

Digital Logic

Pocket Data Book

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Little Logic

Series	Supply Voltage V _{CC} (V)	Operating Free-air Temperature T _a (°C)
SN74AUC1G/2G/3G	0.8~2.7	-40~85
SN74LVC1G/2G/3G	1.65~5.5	-40~85
SN74AHC1G	2.0~5.5	-40~85
SN74AHC1GxxH	2.0~5.5	-40~85
SN74AHC2GxxH	2.0~5.5	-40~85
SN74AHCT1G	4.5~5.5	-40~85

GATE/OCTAL/Widebus™/Widebus+

Series	Supply Voltage V _{CC} (V)	Operating Free-air Temperature T _a (°C)
SN74ABT	4.5~5.5	-40~85
SN74BCT SN74F SN74ALS SN74AS	4.5~5.5	0~70
SN74LS SN74S SN74xx(STD)	4.75~5.25	0~70
SN74AC SN74AC11 SN74AHC	2.0~5.5	-40~85
SN74HC	2.0~6.0	-40~85
SN74LV	2.0~5.5	-40~85
SN74LVC	2.0~3.6	-40~85
SN74LVT	2.7~3.6	-40~85
SN74ALVC	1.65~3.6	-40~85
SN74ALVT	2.3~3.6	-40~85
SN74AVC	1.4~3.6	-40~85

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Production processing does not necessarily include testing of all parameters.

See www.ti.com/sc/logic for the most current data sheets.

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16271	12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER WITH 3-STATE OUTPUTS	554
16282	18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS	556
16334	16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	558
16344	1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS	560
16373	16-BIT TRANSPARENT LATCHES WITH 3-STATE OUTPUTS	562
16374	16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS	564
16409	9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER WITH 3-STATE OUTPUTS	566
16460	4-TO-1 MULTIPLEXED/DEMULPLEXED TRANSCEIVERS WITH 3-STATE OUTPUTS	568
16470	16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS	570
16500	18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS	572
16501	18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS	574
16524	18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS	576
16525	18-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS	578
16540	16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	580
16541	16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	581
16543	16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS	582
16600	18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	584
16601	18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	586
16620	16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	588
16623	16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	590

TTL CMOS SN74 BiCMOS		Page
Device	Function	
16640	16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	591
16646	16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS	592
16651	16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS	594
16652	16-BIT BUS TRANSCEIVERS AND REGISTERS WITH 3-STATE OUTPUTS	596
16657	16-BIT TRANSCEIVERS WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS	598
16721	20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS	600
16722	22-BIT FLIP-FLOP WITH 3-STATE OUTPUTS	601
16820	10-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH DUAL OUTPUTS	602
16821	20-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS	603
16823	18-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH DUAL OUTPUTS	604
16825	18-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	605
16827	20-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	606
16831	1-TO-4 ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS	607
16832	1-TO-4 ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS	608
16833	DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS	610
16834	16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	612
16835	3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	613
16841	20-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS	614
16843	18-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS	615
16853	DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS	616
16861	20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	618
16863	18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	619
16901	18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS	620
16903	3.3-V 12-BIT UNIVERSAL BUS DRIVER WITH PARITY CHECKER AND DUAL 3-STATE OUTPUTS	622
16952	16-BIT REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS	624
25244	25Ω OCTAL BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	626
25245	25Ω OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	627
25642	25-Ω OCTAL BUS TRANSCEIVER	628
29821	10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS	629
29825	8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS	630
29827	10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS	631
29828	10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS	632
29841	10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS	633

TTL CMOS SN74 BiCMOS		Page
Device	Function	
29843	9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS	634
29854	8-BIT TO 9-BIT PARITY BUS TRANSCEIVER	636
29863	9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	638
29864	9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	639
32240	32-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS	640
32244	36-BIT BUFFER/DRIVER WITH 3-STATE OUTPUTS	642
32245	36-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS	644
32316	16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS	646
32318	18-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS	648
32373	32-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS	650
32374	32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS	652
32501	36-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	654
32543	36-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	656
40103	8-STAGE SYNCHRONOUS DOWN COUNTERS	658
162240	3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	659
162241	3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	660
162244	16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	661
162245	16-BIT TRANSCEIVER WITH 3-STATE OUTPUTS	662
162260	12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS	664
162268	12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS	666
162280	16-BIT TO 32-BIT REGISTERED BUS EXCHANGER WITH BYTE MASKS AND 3-STATE OUTPUTS	668
162282	18-BIT TO 36-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS	670
162334	16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	672
162344	1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS	674
162373	3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS	676
162374	3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS	677
162460	4-TO-1 MULTIPLEXED/DEMULPLEXED REGISTERED TRANSCEIVERS WITH 3-STATE OUTPUTS	678
162500	18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS	680
162501	18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS	682
162525	16-BIT REGISTERED BUS TRANSCEIVER WITH 3-STATE OUTPUTS	684
162541	3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	686
162601	18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS	688
162721	3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS	690
162820	3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS	691
162823	18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS	692

TTL CMOS SN74 BiCMOS		Page
Device	Function	
162825	18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	693
162827	20-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS	694
162830	1-BIT TO 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS	695
162831	1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS	696
162832	1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS	697
162834	18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	698
162835	18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	699
162836	20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS	700
162841	20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS	701
164245	16-BIT TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS	702
322374	3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS	703

FUNCTION

1G / 2G / 3G

LITTLE LOGIC GATE (AND/NAND/OR/NOR/EX-OR)

Description	No. of Input	Circuit	Input	Output	Type	Technology																		
						CMOS		BICMOS					Advanced CMOS											
						HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC				
POSITIVE-AND	2	1			1G08																			
		2			2G08																			*
POSITIVE-NAND	2	1			1G00																			○
		2			2G00																			*
POSITIVE- OR	2	1			1G32																			○
		2			2G32																			○
POSITIVE- NOR	2	1			1G02																			○
		2			2G02																			○
EXCLUSIVE-OR	2	1			1G86																			*
		2			2G86																			*

Explanatory notes [Input] SCH : Schmitt-Trigger Inputs

[Output] BUF : Buffered Output OC : Open-Collector Output 3S : 3-State Output

Status ○ : Product available in technology indicated * : New product planned in technology indicated × : Discontinued

LITTLE LOGIC GATE (INVERTER/NONINVERTER)

Description	No. of Input	Circuit	Input	Output	Type	Technology																				
						CMOS		BICMOS					Advanced CMOS													
						HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC						
INVERTING	1	1			1G04																			○		
				UBF	1GU04																				○	
				OC	1G06																					○
				SCH	1G14																					○
					2G04																					*
		2		UBF	2GU04																					*
				OC	2G06																					*
				SCH	2G14																					*
					2G04																					*
					3G04																					*
		3		UBF	3GU04																					*
				OC	3G06																					*
				SCH	2G14																					*
				SCH	3G14																					*
																										*
NON-INVERTING	1	1		OC	1G07																			○		
				SCH	1G17																				○	
					1G86																				○	
		2		OC	2G07																				*	
				SCH	2G17																				*	
					2G34																				*	
		3			2G66																				*	
				OC	3G07																				*	
				SCH	3G17																				*	
				2G34																					*	
				3G34																					*	

Explanatory notes [Input] SCH : Schmitt-Trigger Inputs

[Output] BUF : Buffered Output OC : Open-Collector Output 3S : 3-State Output

Status ○ : Product available in technology indicated * : New product planned in technology indicated × : Discontinued

LITTLE LOGIC BUFFER/DRIVER

Description	Circuit	Output	Type	Technology																
				CMOS		BiCMOS				Advanced CMOS										
				HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC		
NON-INVERTING	1	3S	1G125																	
		3S	1G126																	
	2	3S	2G125																	*
		3S	2G126																	*
		3S	2G241																	*
INVERTING	1	3S	1G240																*	

Explanatory notes Output 3S : 3-State Output R3S : Series Resistor and 3-State output OC : Open-Collector Output
Status ○ : Product available in technology indicated * : New product planned in technology indicated × : Discontinued

LITTLE LOGIC D-TYPE FLIP-FLOP

Trigger	Circuit	PRE · CLR	Output	Q · /Q	Type	Technology														
						CMOS		BiCMOS				Advanced CMOS								
						HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC
POS	1		2S	Q	1G79															*
			2S	/Q	1G80															*
		B	2S	B	2G74															*

Explanatory notes [Trigger] POS : POSITIVE EDGE, NEG : NEGATIVE EDGE
[PRE · CLR] B : Preset and Clear, C : Clear only
[Output] 2S : Totem pole Output 3S : 3-State Output
[Q·/Q] B : Q-/Q-Output Q : Q-Output /Q : /Q-Output
Status ○ : Product available in technology indicated * : New product planned in technology indicated × : Discontinued

LITTLE LOGIC Data Selectors/Multiplexers

No. of Input/Output	Output	Circuit	Type	Technology																
				CMOS		BiCMOS				Advanced CMOS										
				HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AUC		
2/1	2S	1	20157																	*

Explanatory notes [Output] 2S : Totem Pole Output 3S : 3-State Output OC : Open-Collector Output
Status ○ : Product available in technology indicated * : New product planned in technology indicated × : Discontinued

LITTLE LOGIC ANALOG SWITCH

Description	Type	Technology														
		CMOS		BICMOS					Advanced CMOS							
		HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	AJVC
SINGLE ANALOG SWITCH	1G66												○			○
One of Two Noninverting Demultiplexer with 3-State Deselected Output	1G18												○			
SINGLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS	2G53												○			*
DUAL ANALOG SWITCH	2G66												○			*

Status ○ : Product available in technology indicated * : New product planned in technology indicated × : Discontinued

PIN ASSIGNMENTS

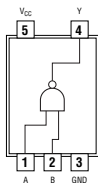
1G / 2G / 3G

Pin Assinments

1G00

SINGLE 2-INPUT POSITIVE-NAND GATE

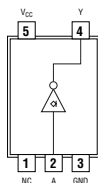
$$Y = \overline{AB}$$



See page 27

1G06

SINGLE INVERTER BUFFER/DRIVER
WITH OPEN-DRAIN OUTPUT



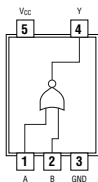
NC – No internal connection

See page 29

1G02

SINGLE 2-INPUT POSITIVE-NOR GATE

$$Y = \overline{A + B}$$

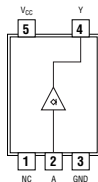


NC – No internal connection

See page 27

1G07

SINGLE BUFFER/DRIVER
WITH OPEN-DRAIN OUTPUT

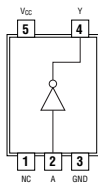


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1G04

SINGLE INVERTER GATE

$$Y = \overline{A}$$



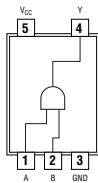
NC – No internal connection

See page 28

1G08

SINGLE 2-INPUT POSITIVE-AND GATE

$$Y = AB$$

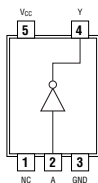


See page 30

1GU04

SINGLE INVERTER

$$Y = \overline{A}$$



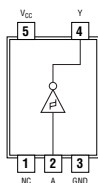
NC – No internal connection

See page 28

1G14

SINGLE SCHMITT-TRIGGER INVERTER GATE

$$Y = \overline{A}$$



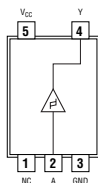
NC – No internal connection

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Pin Assignments

1G17

SINGLE SCHMITT-TRIGGER BUFFER

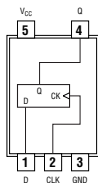


NC – No internal connection

See page 31

1G79

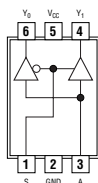
SINGLE POSITIVE-EDGE-TRIGGERED
D-TYPE FLIP-FLOP



See page 33

1G18

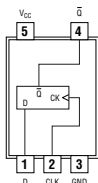
1-OF-2 NONINVERTING DEMULTIPLEXER
WITH 3-STATE DESELECTED OUTPUT



See page 31

1G80

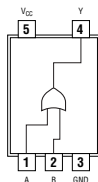
SINGLE POSITIVE-EDGE-TRIGGERED
D-TYPE FLIP-FLOP



See page 33

1G32

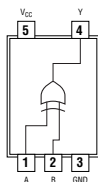
SINGLE 2-INPUT POSITIVE-OR GATE
 $Y = A + B$



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1G86

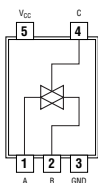
SINGLE 2-INPUT EXCLUSIVE-OR GATE
 $Y = A \oplus B = \bar{A}B + A\bar{B}$



See page 34

1G66

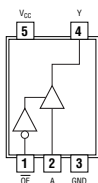
SINGLE ABILATERAL ANALOG SWITCH



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1G125

SINGLE BUS BUFFER GATE
WITH 3-STATE OUTPUT
 $Y = A$



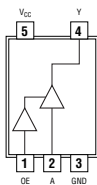
See page 34

Pin Assinments

1G126

SINGLE BUS BUFFER GATE
WITH 3-STATE OUTPUT

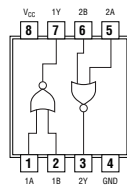
$$Y = A$$



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2G02

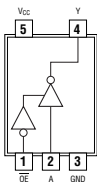
DUAL 2-INPUT POSITIVE-NOR GATE



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1G240

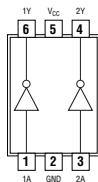
SINGLE BUFFER/DRIVER WITH 3-STATE OUTPUT



See page 35

2G04

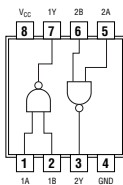
DUAL INVERTER GATE



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2G00

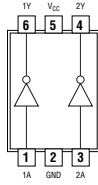
DUAL 2-INPUT POSITIVE-NAND GATE



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2GU04

DUAL INVERTER GATE

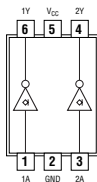


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Pin Assignments

2G06

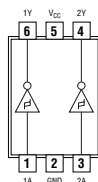
DUAL INVERTER BUFFER/DRIVER
WITH OPEN-DRAIN OUTPUTS



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2G14

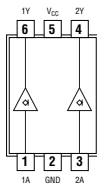
DUAL SCHMITT-TRIGGER INVERTER



See page 39

2G07

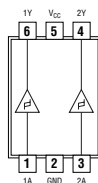
DUAL BUFFER/DRIVER
WITH OPEN-DRAIN OUTPUTS



See page 38

2G17

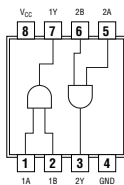
DUAL SCHMITT-TRIGGER BUFFER



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2G08

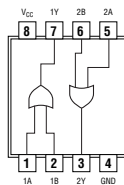
DUAL 2-INPUT POSITIVE-AND GATE



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2G32

DUAL 2-INPUT POSITIVE-OR GATE

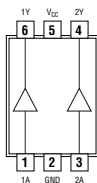


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Pin Assinments

2G34

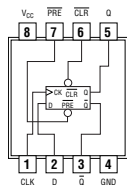
DUAL BUFFER GATE



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2G74

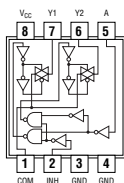
SINGLE POSITIVE-EDGE-TRIGGERED
D-TYPE FLIP-FLOP WITH CLEAR AND PRESET



See page 42

2G53

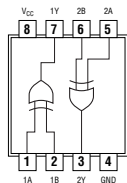
DUAL ANALOG MULTIPLEXER/DEMULTIPLEXER



See page 41

2G86

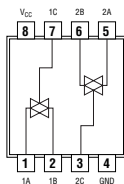
DUAL 2-INPUT EXCLUSIVE-OR GATE



See page 43

2G66

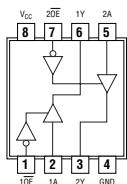
DUAL BILATERAL ANALOG SWITCH



See page 42

2G125

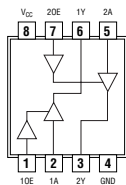
DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS



See page 43

2G126

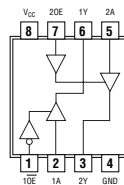
DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS



See page 44

2G241

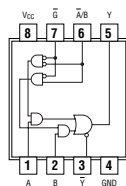
DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS



See page 45

2G157

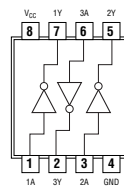
SINGLE 2-LINE TO 1-LINE DATA
SELECTOR/MULTIPLEXER



See page 44

3G04

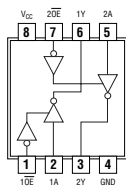
TRIPLE INVERTER GATE



See page 46

2G240

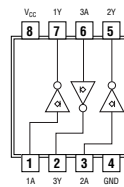
DUAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 45

3G06

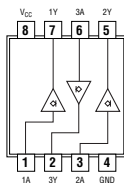
TRIPLE INVERTER BUFFER/DRIVER
WITH OPEN-DRAIN OUTPUTS



See page 46

3G07

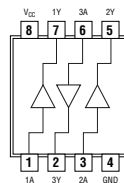
TRIPLE BUFFER/DRIVER
WITH OPEN-DRAIN OUTPUTS



See page 47

3G34

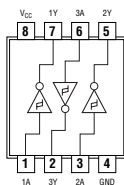
TRIPLE BUFFER GATE



See page 48

3G14

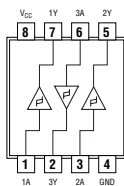
TRIPLE SCHMITT-TRIGGER INVERTER



See page 47

3G17

TRIPLE SCHMITT-TRIGGER BUFFER



See page 48

**FUNCTION
AND
ELECTRICAL
CHARACTERISTICS**

1G / 2G / 3G

1G00

SINGLE 2-INPUT POSITIVE-NAND GATE

$$\bullet Y = \overline{AB}$$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
I _{OL}	MAX	8	8	32	24	8	4	9	8	mA

FUNCTION TABLE

INPUT		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t _{PLH}	A or B	Y	MAX	8.5	9	4	4.7	5.5	8	2	2.2
t _{PHL}				8.5	9	4	4.7	5.5	8	2	2.2

UNIT:ns

1G02

SINGLE 2-INPUT POSITIVE-NOR GATE

$$\bullet Y = \overline{A + B}$$

Logic Diagram (positive logic)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
I _{OL}	MAX	8	8	32	24	8	4	9	8	mA

FUNCTION TABLE

INPUT		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t _{PLH}	A or B	Y	MAX	8.5	8.5	4	4.5	5.5	8	2.1	2.4
t _{PHL}				8.5	8.5	4	4.5	5.5	8	2.1	2.4

UNIT:ns

1G04

SINGLE INVERTER GATE

$$\bullet Y = \bar{A}$$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
I _{DH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
I _{OL}	MAX	8	8	32	24	8	4	9	8	mA

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t _{PLH}	A	Y	MAX	8.5	8.5	3.7	4.2	5.2	7.5	1.9	2.2
t _{PHL}				8.5	8.5	3.7	4.2	5.2	7.5	1.9	2.2

UNIT:ns

1GU04

SINGLE INVERTER

$$\bullet Y = \bar{A}$$

● Unbuffered Output

● Supply Voltage Range : 2V ~ 5.5V

Logic Diagram



FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
I _{DH}	MAX	-8	-32	-24	-8	-4	-9	-8	mA
I _{OL}	MAX	8	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t _{PLH}	A	Y	MAX	8	3	3.7	4	5	2.1	2.4
t _{PHL}				8	3	3.7	4	5	2.1	2.4

UNIT:ns

1G06

SINGLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	V _L 5V	V _L 3.3V	V _L 2.5V	V _L 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
V _O	MAX	5.5	5.5	5.5	5.5	2.7	2.7	V
I _{OL}	MAX	32	24	8	4	9	8	mA

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	V _L 5V	V _L 3.3V	V _L 2.5V	V _L 1.8V	AUC 2.5V	AUC 1.8V
t _{PLH}	A	Y	MAX	3	4	4	5.6	1.8	2.5
t _{PHL}				3	4	4	5.6	1.8	2.5

UNIT:ns

1G07

SINGLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	V _L 5V	V _L 3.3V	V _L 2.5V	V _L 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	5.5	5.5	5.5	5.5	2.7	2.7	V
I _{OL}	MAX	32	24	8	4	9	8	mA

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	V _L 5V	V _L 3.3V	V _L 2.5V	V _L 1.8V	AUC 2.5V	AUC 1.8V
t _{PLH}	A	Y	MAX	3.5	4.2	5.5	8.3	1.8	2.5
t _{PHL}				3.5	4.2	5.5	8.3	1.8	2.5

UNIT:ns

1G08

SINGLE 2-INPUT POSITIVE-AND GATE

● $Y = AB$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
I _{OL}	MAX	8	8	32	24	8	4	9	8	mA

FUNCTION TABLE

INPUT		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t _{PLH}	A or B	Y	MAX	9	9	4	4.5	5.5	8	2	2.4
t _{PHL}				9	9	4	4.5	5.5	8	2	2.4

UNIT:ns

1G14

SINGLE SCHMITT-TRIGGER INVERTER GATE

● $Y = \bar{A}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
I _{OL}	MAX	8	8	32	24	8	4	9	8	mA

FUNCTION TABLE

INPUT	OUTPUT
A	Y
H	L
L	H

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t _{PLH}	A	Y	MAX	12	9	5	5.5	6.5	11	2.5	2.5
t _{PHL}				12	9	5	5.5	6.5	11	2.5	2.5

UNIT:ns

1G17

SINGLE SCHMITT-TRIGGER BUFFER

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	VLC 5V	VLC 3.3V	VLC 2.5V	VLC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I _{OL}	MAX	32	24	8	4	9	8	mA

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

SWITCHING CHARACTERISTICS

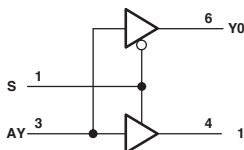
PARAMETER	INPUT	OUTPUT	MAX or MIN	VLC 5V	VLC 3.3V	VLC 2.5V	VLC 1.8V	AUC 2.5V	AUC 1.8V
t _{PLH}	A	Y	MAX	5	5.5	6.5	11	2.5	2.4
t _{PHL}				5	5.5	6.5	11	2.5	2.4

UNIT:ns

1G18

1-OF-2 NONINVERTING DEMULTIPLEXER WITH 3-STATE Deselected OUTPUT

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT	
S	A	Y0	Y1
L	L	L	Z
L	H	H	Z
H	L	Z	L
H	H	Z	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	VLC 5V	VLC 3.3V	VLC 2.5V	VLC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	VLC 5V	VLC 3.3V	VLC 2.5V	VLC 1.8V
t _{PLH}	A	Y	MAX	3.2	4.2	5	9.3
t _{PHL}				3.2	4.2	5	9.3
t _{PZL}	S	Y	MAX	3.4	4.6	5.6	10.2
t _{PZH}				3.4	4.6	5.6	10.2
t _{PLZ}	S	Y	MAX	3.3	4.9	5.3	12.7
t _{PHZ}				3.3	4.9	5.3	12.7

UNIT:ns

1G32

SINGLE 2-INPUT POSITIVE-OR GATE

● $Y = A + B$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC		LVC		LVC		AUC		UNIT
		AHCT	AHCT	5V	3.3V	2.5V	1.8V	2.5V	1.8V	
I _{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
I _{DH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
I _{OL}	MAX	8	8	32	24	8	4	9	8	mA

FUNCTION TABLE

INPUT		OUTPUT Y
A	B	
H	X	H
X	H	H
L	L	L

SWITCHING CHARACTERISTICS

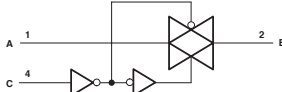
PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC		LVC		LVC		AUC		UNIT
				AHCT	AHCT	5V	3.3V	2.5V	1.8V	2.5V	1.8V	
t _{PLH}	A or B	Y	MAX	8.5	9	4	4.5	5.5	8	2.1	2.4	
t _{PHL}				8.5	9	4	4.5	5.5	8	2.1	2.4	

UNIT:ns

1G66

SINGLE ABILATERAL ANALOG SWITCH

Logic Diagram



FUNCTION TABLE

CONTROL INPUT (C)	SWITCH
L	OFF
H	ON

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC	AUC	UNIT
I _{CC}	MAX	0.01	0.01	mA

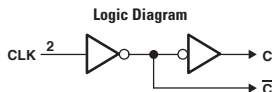
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC		LVC		AUC		UNIT
				5V	3.3V	2.5V	1.8V	2.5V	1.8V	
t _{PLH}	A or B	B or A	MAX	0.6	0.8	1.2	2	0.1	0.2	
t _{PHL}				0.6	0.8	1.2	2	0.1	0.2	
t _{PZH}	C	B or A	MAX	4.2	5	6.5	12	1	1.1	
t _{PZL}				4.2	5	6.5	12	1	1.1	
t _{PHZ}	C	B or A	MAX	5	6.5	6.9	10	2.2	2.9	
t _{PLZ}				5	6.5	6.9	10	2.2	2.9	

UNIT:ns

1G79

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	V _{CC} 5V	V _{CC} 3.3V	V _{CC} 2.5V	V _{CC} 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

FUNCTION TABLE

INPUT		OUTPUT
CLK	D	Q
↑	H	H
↑	L	L
L	X	Q ₀

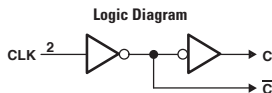
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	V _{CC} 5V	V _{CC} 3.3V	V _{CC} 2.5V	V _{CC} 1.8V
f _{max}			MIN	160	160	160	160
t _w	CLK high or low		MIN	2.5	2.5	2.5	2.5
t _{su}	Before CLK ↑, Data high		MIN	1.2	1.3	1.4	2.2
	Before CLK ↑, Data low			1.2	1.3	1.4	2.6
t _h	Data after CLK ↑		MIN	0.5	1.0	0.4	0.3
t _{PLH}	CLK	Q	MAX	4.5	5.2	7	9.9
t _{PHL}				4.5	5.2	7	9.9

UNIT f_{max} : MHz other : ns

1G80

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP



FUNCTION TABLE

INPUT		OUTPUT
CLK	D	Q
↑	H	L
↑	L	H
L	X	Q ₀

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	V _{CC} 5V	V _{CC} 3.3V	V _{CC} 2.5V	V _{CC} 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	V _{CC} 5V	V _{CC} 3.3V	V _{CC} 2.5V	V _{CC} 1.8V
f _{max}			MIN	160	160	160	160
t _w	CLK high or low		MIN	2.5	2.5	2.5	2.5
t _{su}	Before CLK ↑, Data high		MIN	1.1	1.3	1.5	2.3
	Before CLK ↑, Data low			1.1	1.3	1.5	2.5
t _h	Data after CLK ↑		MIN	0.4	0.9	0.2	0
t _{PLH}	CLK	Q	MAX	4.5	5.2	7	9.9
t _{PHL}				4.5	5.2	7	9.9

UNIT f_{max} : MHz other : ns

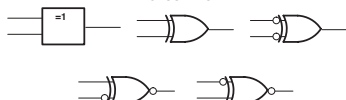
1G86

SINGLE 2-INPUT EXCLUSIVE-OR GATE

$$\bullet Y = A \oplus B = \bar{A}B + A\bar{B}$$

Logic Diagram

EXCLUSIVE OR



An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I _{DH}	MAX	-8	-8	-32	-24	-8	-4	mA
I _{OL}	MAX	8	8	32	24	8	4	mA

FUNCTION TABLE

INPUT		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t _{PLH}	A or B	Y	MAX	10	9	4	5	5.5	9.9
t _{PHL}				10	9	4	5	5.5	9.9

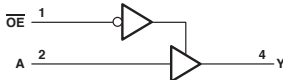
UNIT:ns

1G125

SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

$$\bullet Y = A$$

Logic Diagram



FUNCTION TABLE

INPUT		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
I _{DH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
I _{OL}	MAX	8	8	32	24	8	4	9	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t _{PLH}	A	Y	MAX	8.5	8.5	4	4.5	5.5	8	1.7	2.5
t _{PHL}				8.5	8.5	4	4.5	5.5	8	1.7	2.5
t _{PZH}	\overline{OE}	Y	MAX	8	8	5	5.3	6.5	9.4	1.9	2.6
t _{PZL}				8	8	5	5.3	6.5	9.4	1.9	2.6
t _{PHZ}	\overline{OE}	Y	MAX	10	10	4.2	5	5	9.2	1.7	3.1
t _{PLZ}				10	10	4.2	5	5	9.2	1.7	3.1

UNIT:ns

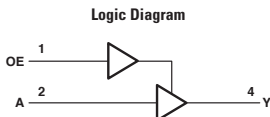
1G126

SINGLE BUS BUFFER GATE WITH 3-STATE OUTPUT

● Y = A

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-8	-8	-32	-24	-8	-4	-9	-8	mA
I _{OL}	MAX	8	8	32	24	8	4	9	8	mA



FUNCTION TABLE

INPUT		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t _{PLH}	A	Y	MAX	8.5	8.5	4	4.5	5.5	8	1.7	2.5
				8.5	8.5	4	4.5	5.5	8	1.7	2.5
t _{PHL}	OE	Y	MAX	8	8	5	5.3	6.6	9.4	1.9	2.5
				8	8	5	5.3	6.6	9.4	1.9	2.5
t _{PHZ}	OE	Y	MAX	10	10	4.2	5.5	5.5	9.8	1.7	3.1
				10	10	4.2	5.5	5.5	9.8	1.7	3.1

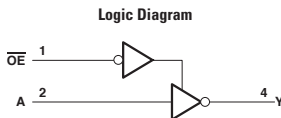
UNIT:ns

1G240

SINGLE BUFFER/DRIVER WITH 3-STATE OUTPUT

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	-9	-8	mA
I _{OL}	MAX	32	24	8	4	9	8	mA



FUNCTION TABLE

INPUT		OUTPUT
OE	A	Y
L	H	L
L	L	H
H	X	Z

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	AUC 2.5V	AUC 1.8V
t _{PLH}	A	Y	MAX	4	4.5	5.5	8	1.7	2.5
				4	4.5	5.5	8	1.7	2.5
t _{PHL}	OE	Y	MAX	5.2	5.4	6.5	9.4	1.9	2.6
				5.2	5.4	6.5	9.4	1.9	2.6
t _{PHZ}	OE	Y	MAX	4.1	5.2	4.9	9.4	1.7	3.1
				4.1	5.2	4.9	9.4	1.7	3.1

UNIT:ns

2G00

DUAL 2-INPUT POSITIVE-NAND GATE

RECOMMENDED OPERATING CONDITIONS

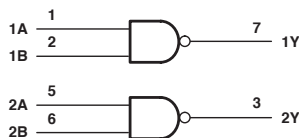
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t _{PLH}	A or B	Y	MAX	3.3	4.3	4.8	8.6
t _{PHL}				3.3	4.3	4.8	8.6

UNIT:ns

Logic Diagram



FUNCTION TABLE (each gate)

INPUT		OUTPUT
A	B	Y
H	H	L
L	X	L
X	L	L

2G02

DUAL 2-INPUT POSITIVE-NOR GATE

RECOMMENDED OPERATING CONDITIONS

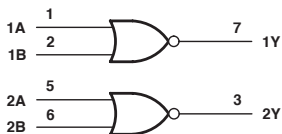
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t _{PLH}	A or B	Y	MAX	4.4	4.9	5.4	8.9
t _{PHL}				4.4	4.9	5.4	8.9

UNIT:ns

Logic Diagram



FUNCTION TABLE (each gate)

INPUT		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

2G04

DUAL INVERTER GATE

RECOMMENDED OPERATING CONDITIONS

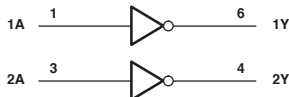
PARAMETER	MAX or MIN	VLC 5V	VLC 3.3V	VLC 2.5V	VLC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{DH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	VLC 5V	VLC 3.3V	VLC 2.5V	VLC 1.8V
t _{PLH}	A	Y	MAX	3.2	4.1	4.4	8
t _{PHL}				3.2	4.1	4.4	8

UNIT:ns

Logic Diagram



FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
H	L
L	H

2GU04

DUAL INVERTER GATE

RECOMMENDED OPERATING CONDITIONS

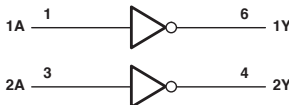
PARAMETER	MAX or MIN	VLC 5V	VLC 3.3V	VLC 2.5V	VLC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{DH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	VLC 5V	VLC 3.3V	VLC 2.5V	VLC 1.8V
t _{PLH}	A	Y	MAX	3	3.7	4	5.5
t _{PHL}				3	3.7	4	5.5

UNIT:ns

Logic Diagram



FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
H	L
L	H

2G06

DUAL INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

RECOMMENDED OPERATING CONDITIONS

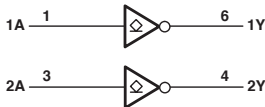
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
V ₀	MAX	5.5	5.5	5.5	5.5	V
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t _{PLH}	A	Y	MAX	2.9	3.4	3.9	7.2
t _{PHL}				2.9	3.4	3.9	7.2

UNIT:ns

Logic Diagram



FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
H	L
L	H

2G07

DUAL BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

RECOMMENDED OPERATING CONDITIONS

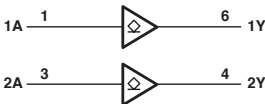
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
V ₀	MAX	5.5	5.5	5.5	5.5	V
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t _{PLH}	A	Y	MAX	2.9	3.7	4.4	8.6
t _{PHL}				2.9	3.7	4.4	8.6

UNIT:ns

Logic Diagram



FUNCTION TABLE (each buffer/driver)

INPUT A	OUTPUT Y
H	H
L	L

2G08

DUAL 2-INPUT POSITIVE-AND GATE

RECOMMENDED OPERATING CONDITIONS

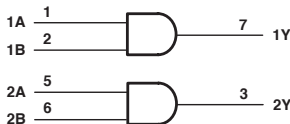
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t _{PLH}	A or B	Y	MAX	3.8	4.7	5.1	9
t _{PHL}				3.8	4.7	5.1	9

UNIT:ns

Logic Diagram



FUNCTION TABLE (each gate)

INPUT		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

2G14

DUAL SCHMITT-TRIGGER INVERTER

RECOMMENDED OPERATING CONDITIONS

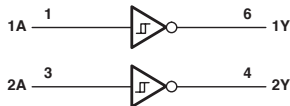
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t _{PLH}	A	Y	MAX	4.3	5.4	5.7	9.5
t _{PHL}				4.3	5.4	5.7	9.5

UNIT:ns

Logic Diagram



FUNCTION TABLE (each inverter)

INPUT	OUTPUT
A	Y
H	L
L	H

2G17

DUAL SCHMITT-TRIGGER BUFFER

RECOMMENDED OPERATING CONDITIONS

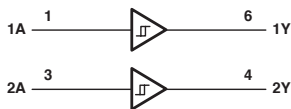
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A	Y	MAX	4.3	5.4	5.7	9.3
t_{PHL}				4.3	5.4	5.7	9.3

UNIT:ns

Logic Diagram



FUNCTION TABLE

(each inverter)

INPUT A	OUTPUT Y
H	H
L	L

2G32

DUAL 2-INPUT POSITIVE-OR GATE

RECOMMENDED OPERATING CONDITIONS

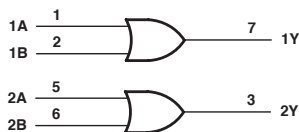
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I_{CC}	MAX	0.01	0.01	0.01	0.01	mA
I_{OH}	MAX	-32	-24	-8	-4	mA
I_{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t_{PLH}	A or B	Y	MAX	3.2	3.8	4.4	8
t_{PHL}				3.2	3.8	4.4	8

UNIT:ns

Logic Diagram



FUNCTION TABLE

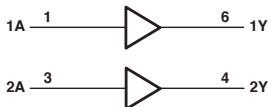
(each gate)

INPUT		OUTPUT Y
A	B	Y
H	X	H
X	H	H
L	L	L

2G34

DUAL BUFFER GATE

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	V _{CC} 5V	V _{CC} 3.3V	V _{CC} 2.5V	V _{CC} 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

FUNCTION TABLE
(each gate)

INPUT A	OUTPUT Y
H	H
L	L

SWITCHING CHARACTERISTICS

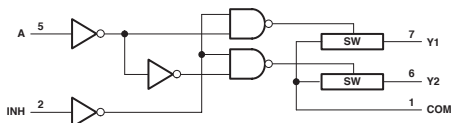
PARAMETER	INPUT	OUTPUT	MAX or MIN	V _{CC} 5V	V _{CC} 3.3V	V _{CC} 2.5V	V _{CC} 1.8V
t _{PLH}	A	Y	MAX	3.2	4.1	4.4	8.6
t _{PHL}				3.2	4.1	4.4	8.6

UNIT:ns

2G53

DUAL ANALOG MULTIPLEXER/DEMULTIPLEXER

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	V _{CC} 5V	UNIT
I _{CC}	MAX	0.01	mA

FUNCTION TABLE

CONTROL INPUT		ON CHANNEL
INH	A	
L	L	Y1
L	H	Y2
H	X	None

SWITCHING CHARACTERISTICS

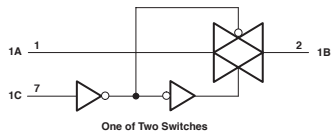
PARAMETER	INPUT	OUTPUT	MAX or MIN	V _{CC} 5V	V _{CC} 3.3V	V _{CC} 2.5V	V _{CC} 1.8V
t _{PLH}	COM or Y	Y or COM	MAX	0.6	0.8	1.2	2
t _{PHL}				0.6	0.8	1.2	2
t _{PZH}	INH	COM or Y	MAX	4.5	5.4	6.1	9
t _{PZL}				4.5	5.4	6.1	9
t _{PHZ}	A	COM or Y	MAX	8	8.1	8.3	10.9
t _{PLZ}				8	8.1	8.3	10.9
t _{PZH}	A	COM or Y	MAX	5.4	5.8	7.2	10.3
t _{PZL}				5.4	5.8	7.2	10.3
t _{PHZ}	A	COM or Y	MAX	5	7.2	7.9	9.4
t _{PLZ}				5	7.2	7.9	9.4

UNIT:ns

2G66

DUAL BILATERAL ANALOG SWITCH

Logic Diagram, each switch



One of Two Switches

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC	UNIT
I _{CC}	MAX	0.01	mA

FUNCTION TABLE
(each section)

CONTROL INPUT (C)	SWITCH
L	OFF
H	ON

SWITCHING CHARACTERISTICS

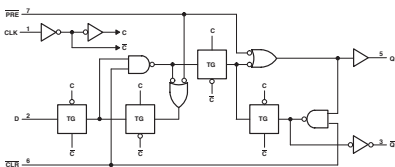
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t _{PLH}	A or B	B or A	MAX	0.6	0.8	1.2	2
t _{PHL}				0.6	0.8	1.2	2
t _{PZH}	C	A or B	MAX	3.9	4.4	5.6	10
t _{PZL}				3.9	4.4	5.6	10
t _{PHZ}	C	A or B	MAX	6.3	7.2	6.9	10.5
t _{PLZ}				6.3	7.2	6.9	10.5

UNIT:ns

2G74

SINGLE POSITIVE-EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH CLEAR AND PRESET

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{DH}	MAX	-32	-16	-8	-4	mA
I _{OL}	MAX	32	16	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
f _{max}			MIN	200	175	175	80
t _w	CLK		MIN	2	2.7	2.7	6.2
	PRE or CLR low			2	2.7	2.7	6.2
t _{su}	Data		MIN	1.1	1.3	1.7	2.9
	PRE or CLR inactive			1	1.2	1.4	1.9
t _h			MIN	0.5	1.2	0.3	0
t _{PLH}	CLK	Q	MAX	4.1	5.9	7.1	13.4
t _{PHL}				4.1	5.9	7.1	13.4
t _{PLH}	CLK	Q̄	MAX	4.4	6.2	7.7	14.4
t _{PHL}				4.4	6.2	7.7	14.4
t _{PLH}	PRE or CLR	Q or Q̄	MAX	4.1	5.9	7	12.9
t _{PHL}				4.1	5.9	7	12.9

UNIT:ns

FUNCTION TABLE

INPUT				OUTPUT	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H†	H†
H	H	↑	H	L	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	Q̄ ₀

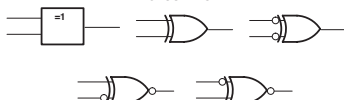
† This configuration is nonstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

2G86

DUAL 2-INPUT EXCLUSIVE-OR GATE

Logic Diagram

EXCLUSIVE OR



An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	V _{CC} 5V	V _{CC} 3.3V	V _{CC} 2.5V	V _{CC} 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

FUNCTION TABLE

(each gate)

INPUT		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

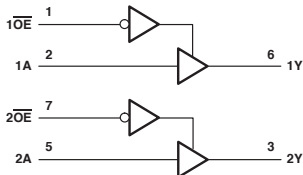
RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	V _{CC} 5V	V _{CC} 3.3V	V _{CC} 2.5V	V _{CC} 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

2G125

DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	V _{CC} 5V	V _{CC} 3.3V	V _{CC} 2.5V	V _{CC} 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

FUNCTION TABLE

(each buffer)

INPUT		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	V _{CC} 5V	V _{CC} 3.3V	V _{CC} 2.5V	V _{CC} 1.8V
t _{PLH}	A	Y	MAX	3.7	4.3	4.8	9.1
t _{PHL}				3.7	4.3	4.8	9.1
t _{PZH}	\overline{OE}	Y	MAX	3.8	4.7	5.6	9.9
t _{PZL}				3.8	4.7	5.6	9.9
t _{PHZ}	\overline{OE}	Y	MAX	3.4	4.6	5.8	11.6
t _{PLZ}				3.4	4.6	5.8	11.6

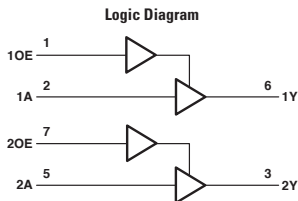
UNIT: ns

2G126

DUAL BUS BUFFER GATE WITH 3-STATE OUTPUTS

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	V _L 5V	V _L 3.3V	V _L 2.5V	V _L 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{DH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA



FUNCTION TABLE (each buffer)

INPUT		OUTPUT
OE	A	Y
H	H	H
H	L	L
L	X	Z

SWITCHING CHARACTERISTICS

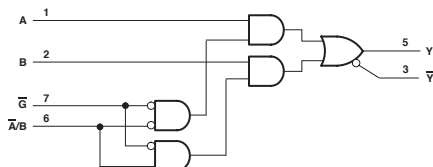
PARAMETER	INPUT	OUTPUT	MAX or MIN	V _L 5V	V _L 3.3V	V _L 2.5V	V _L 1.8V
t _{PLH}	A	Y	MAX	3.2	4	4.9	9.8
t _{PHL}				3.2	4	4.9	9.8
t _{PZH}	OE	Y	MAX	3.1	4.1	5	10
t _{PZL}				3.1	4.1	5	10
t _{PHZ}	OE	Y	MAX	3.3	4.4	5.7	12.6
t _{PLZ}				3.3	4.4	5.7	12.6

UNIT:ns

2G157

SINGLE 2-LINE TO 1-LINE DATA SELECTOR/MULTIPLEXER

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	V _L 5V	V _L 3.3V	V _L 2.5V	V _L 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{DH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

FUNCTION TABLE

INPUT				OUTPUT	
G	A/B	A	B	Y	Y-bar
H	X	X	X	L	L
L	L	L	X	L	H
L	L	H	X	H	L
L	H	X	L	L	H
L	H	X	H	H	L

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	V _L 5V	V _L 3.3V	V _L 2.5V	V _L 1.8V
t _{PLH}	A or B	Y or Y-bar	MAX	4	6	8	14
t _{PHL}				4	6	8	14
t _{PLH}	A/B	Y or Y-bar	MAX	4	6	9	16
t _{PHL}				4	6	9	16
t _{PLH}	G	Y or Y-bar	MAX	4	6	8	14
t _{PHL}				4	6	8	14

UNIT:ns

2G240

DUAL BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

RECOMMENDED OPERATING CONDITIONS

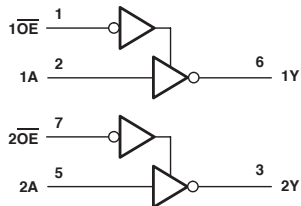
PARAMETER	MAX or MIN	VLC 5V	VLC 3.3V	VLC 2.5V	VLC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	VLC 5V	VLC 3.3V	VLC 2.5V	VLC 1.8V
t _{PLH}	A	Y	MAX	4	4.6	5.5	11.3
				4	4.6	5.5	11.3
t _{PHL}	A	Y	MAX	5	5.4	6.6	11.7
				5	5.4	6.6	11.7
t _{PLZ}	OE	Y	MAX	4.2	5.5	5.7	12.8
				4.2	5.5	5.7	12.8
t _{PHZ}	OE	Y	MAX	4.2	5.5	5.7	12.8
				4.2	5.5	5.7	12.8

UNIT:ns

Logic Diagram



FUNCTION TABLE (each buffer)

INPUT		OUTPUT
OE	A	Y
L	H	L
L	L	H
H	X	Z

2G241

DUAL BUFFER/DRIVER WITH 3-STATE OUTPUTS

RECOMMENDED OPERATING CONDITIONS

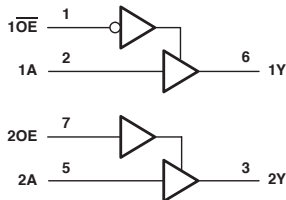
PARAMETER	MAX or MIN	VLC 5V	VLC 3.3V	VLC 2.5V	VLC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	VLC 5V	VLC 3.3V	VLC 2.5V	VLC 1.8V
t _{PLH}	A	Y	MAX	3.7	4.3	4.8	8.8
				3.7	4.3	4.8	8.8
t _{PHL}	A	Y	MAX	3.8	4.7	5.6	9.9
				3.8	4.7	5.6	9.9
t _{PLZ}	OE	Y	MAX	3.4	4.4	5.8	11.6
				3.4	4.4	5.8	11.6
t _{PHZ}	OE	Y	MAX	3.3	4.1	4.7	8.8
				3.3	4.1	4.7	8.8
t _{PLZ}	OE	Y	MAX	3.3	4.2	5.2	12.5
				3.3	4.2	5.2	12.5
t _{PHZ}	OE	Y	MAX	3.3	4.2	5.2	12.5
				3.3	4.2	5.2	12.5

UNIT:ns

Logic Diagram



FUNCTION TABLE

INPUT		OUTPUT
1OE	1A	1Y
L	H	H
L	L	L
H	X	Z

INPUT		OUTPUT
2OE	2A	2Y
H	H	H
H	L	L
L	X	Z

3G04

TRIPLE INVERTER GATE

RECOMMENDED OPERATING CONDITIONS

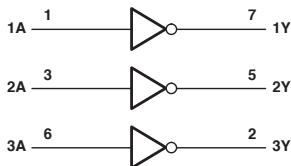
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{DH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t _{PLH}	A	Y	MAX	3.2	4.1	4.4	7.9
t _{PHL}				3.2	4.1	4.4	7.9

UNIT:ns

Logic Diagram



FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
H	L
L	H

3G06

TRIPLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

RECOMMENDED OPERATING CONDITIONS

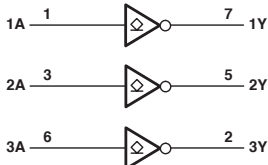
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
V _O	MAX	5.5	5.5	5.5	5.5	V
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t _{PLH}	A	Y	MAX	2.9	3.4	3.9	7.2
t _{PHL}				2.9	3.4	3.9	7.2

UNIT:ns

Logic Diagram



FUNCTION TABLE (each inverter)

INPUT A	OUTPUT Y
H	L
L	H

3G07

TRIPLE BUFFER/DRIVER WITH OPEN-DRAIN OUTPUTS

RECOMMENDED OPERATING CONDITIONS

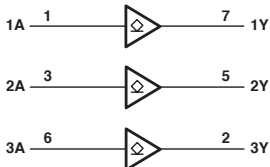
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
V _O	MAX	5.5	5.5	5.5	5.5	V
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t _{PLH}	A	Y	MAX	2.9	3.7	4.3	7.8
t _{PHL}				2.9	3.7	4.3	7.8

UNIT:ns

Logic Diagram



FUNCTION TABLE

(each buffer/driver)

INPUT A	OUTPUT Y
H	H
L	L

3G14

TRIPLE SCHMITT-TRIGGER INVERTER

RECOMMENDED OPERATING CONDITIONS

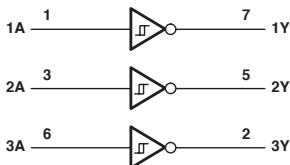
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{OH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t _{PLH}	A	Y	MAX	4.3	5.4	5.7	9.2
t _{PHL}				4.3	5.4	5.7	9.2

UNIT:ns

Logic Diagram



FUNCTION TABLE

(each inverter)

INPUT A	OUTPUT Y
H	L
L	H

3G17

TRIPLE SCHMITT-TRIGGER BUFFER

RECOMMENDED OPERATING CONDITIONS

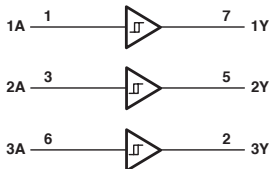
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{DH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t _{PLH}	A	Y	MAX	TBD	TBD	TBD	TBD
t _{PHL}				TBD	TBD	TBD	TBD

UNIT:ns

Logic Diagram



FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

3G34

TRIPLE BUFFER GATE

RECOMMENDED OPERATING CONDITIONS

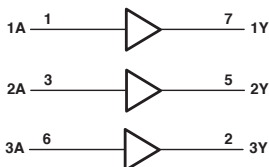
PARAMETER	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V	UNIT
I _{CC}	MAX	0.01	0.01	0.01	0.01	mA
I _{DH}	MAX	-32	-24	-8	-4	mA
I _{OL}	MAX	32	24	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 5V	LVC 3.3V	LVC 2.5V	LVC 1.8V
t _{PLH}	A	Y	MAX	3.2	4.1	4.4	7.9
t _{PHL}				3.2	4.1	4.4	7.9

UNIT:ns

Logic Diagram



FUNCTION TABLE

(each gate)

INPUT A	OUTPUT Y
H	H
L	L

FUNCTION

BUFFER/DRIVER(NON-INVERTING)

Description	No. of Output	Output	Device	Technology																			
				Bipolar					CMOS				BiCMOS				Advanced CMOS						
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
NON-INVERTING	4	3S	125	X	OA																		
		3S	126	X	OA																		
	6	3S	365	X	OA																		
		3S	367	X	OA																		
	8	3S	241			OC	OA																
		3S	244			OC/OC1	OA																
		3S	455																				
		3S	465			X																	
		3S	467	X		X																	
		3S	541																				
		3S	566																				
		3S	747			X																	
		OC	757																				
		OC	760																				
		3S	1241																				
		3S	1244				OA																
		R3S	2241																				
		R3S	2244						X														
		R3S	2541																				
		3S	25241																				
		3S	25244																				
		OC	25757																				
		OC	25760																				
		3S	827																				
	10	R3S	2827																				
		3S	29827																				
	11	R3S	5400																				
		3S	5402																				
	12	R3S	16903																				
		3S	16241																				
	16	3S	16244																				
		3S	16541																				
		R3S	162241																				
		R3S	162244																				
	18	R3S	162541																				
		3S	16825																				
		R3S	162825																				
		3S	16835																				
	20	R3S	162835																				
		3S	16827																				
3S		162827																					
32	3S	32244																					

Explanatory notes [Output] 3S : 3-State Output R3S : Series Resistor and 3-State Output OC : Open-Collector Output

Status ○ : Product available in technology indicated * : New product planned in technology indicated

X : Discontinued ■ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCTxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

BUFFER/DRIVER(INVERTING,INVERTING AND NON-INVERTING,ADDRESS DRIVERS)

Description	No. of Output	Output	Device	Technology																					
				Bipolar						CMOS		BICMOS				Advanced CMOS									
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AMC	AHCT	LV	LVC	ALVC	AVC		
INVERTING	6	3S	366	X	X	X				X/O	/O														
		3S	365	X	OA						O/O	/O													
		3S	436			X																			
		3S	437	X						X															
		3S	231				X	X																	
		3S	240		O			OA/OA	OA	O	O/O	O/O	O/-	OA	OA/H		O/O/O	O/O/O	O	O	OA	OA	OA	OA	OA
	3S	456										O/-													
	3S	466	X	X		X							X/-												
	3S	465	X	X		X																			
	3S	540	O			O/O	1		X	O/O	O/O	OA/-	O	HO			-H/O	-H/O	O	O	OA	OA			
	3S	655															X/H-	X/H-			OA	OA			
	3S	746				X																			
	OC	756		X	O	X						O/-													
	OC	763				X																			
	3S	1240				X							O/-	OA											
	R3S	2240				X																			
	R3S	2540				X																			
	3S	25240											X/-												
	OC	29756											X/-												
	3S	626															X/H-	X/H-				OA			
	R3S	2828											X/-												
	3S	29628										X/B/-													
	R3S	3401																							
	R3S	5403																							
	3S	16240												OA	O/H	H	X	O	O	O		H	OA	H	HO
	3S	16540												OA	O/H	O		X	O	O		H	OA	X	
	R3S	162240													O/H	O									X
	R3S	162540																							X
	3S	16628																X							X
	32	3S	32240													O			X						X
	INVERTING AND NON-INVERTING	8	3S	230				X	X																
			OC	762					X																
ADDRESS DRIVERS	1-2	3S	16830																					H*	
		R3S	162830																					H	
	1-4	3S	16344																						H
		3S	16831																						H
		3S	16832																						H
		R3S	162344																						H
		R3S	162831																						O/H
R3S	162832																						H		

Explanatory notes [Output] 3S : 3-State Output R3S : Series Resistor and 3-State Output OC : Open-Collector Output

Status ○ : Product available in technology indicated * : New product planned in technology indicated

X : Discontinued ■ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCTxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

BUS TRANSCEIVER(NON-INVERTING)

Description	No. of Output	Output	Device	Technology																			
				Bipolar				CMOS				BiCMOS				Advanced CMOS							
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC
NON- INVERTING	4	3S	226			X																	
		3S	440	X																			
		OC	441	X																			
		3S	442	X																			
		3S	443	X																			
		3S	444	X																			
		OC	448	X																			
		3S	449	X																			
3S	243				OA	X	X	-I/O	-I/O														
3S	1243																						
NON- INVERTING	8	3S	245			OA/A1		O	O/O	O/O	O/O	O/O	OB/ HO	OB/ H OA/ R	O/O/O	O/O/O	O	O	OA	OA/H OA/Z	O/HO		
		3S	470												X/I/-	X/I/-							
		3S	472												X/I/-	X/I/-							
		3S	474												X/I/-	X/I/-							
		3S	543												X/I/-	X/I/-							
		OC	615			X					O		OA	HO							OA		
		OC	621		X		OA/A1	X	X														
		3S	623			OA	X	X		O/O	O/O	O/O	O			X/I/O	O/I/O						
		3SIOC	639		X		OA	X															
		OC	641			OA/A1																	
		3S	645			OA/A1	O			O/O	O/O												
		3S	646		OA	O				O/O	O/O	O/O	O/O	OA	HO	X/I/O	X/I/O					OA	
		OC	647		X	X																	
		3S	652		OA	O				O/O	O/O	O/O	O/O	OA	HO	X/I/O	O/I/O					OA	
		3SIOC	654		X	O																	
		3S	657						O							X/I/-	X/I/-						
		3S	659							X/I/-	X/I/-	X/I/-											
		3S	665							X/I/-	X/I/-	X/I/-											
		3S	852					X								X/I/-	X/I/-						
		3S	856					X								X/I/-	X/I/-						
		3S	877					X								X/I/-	X/I/-						
		3S	899												X/I/-								
		3S	1245				OA																
		3S	1645				OA																
		3S	2245													O/O/R/O	HO					OA	
		3S	2623				X																
		3S	2645				X																
		3S	2952											X/I/-	OA	HO						OA	
		3S	26345											X/I/-	OH								
		3S	25543											X/I/-									
		3S	25621											X/I/-									
		3S	25623											X/I/-									
		3S	25641											X/I/-									
		3S	25646											X/I/-									
		3S	25647											X/I/-									
		3S	25652											X/I/-									
		3S	25654											X/I/-									
		3S	3245												X							OA OA/ C/OA	
		3SIOC	533											O			X/I/-	X/I/-					
		3SIOC	853											O			X/I/-	X/I/-					
		3SIOC	29833				X							X/I/-									
		3SIOC	29853				X							X/I/-									
9	3S	863													X/I/-	X/I/-				OA			
		29853			O							O/B/-											
9X4	3S	16409																			HO/ HO		
		861														X/I/-	X/I/-				OA		
10	3S	29861			X							X/B/-											

Explanatory notes [No. of Output] +P: With Parity Bit

[Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output

OC: Open-Collector Output 3SIOC: 3-State Output / Open-Collector Output

Status ○: Product available in technology indicated *: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

BUS TRANSCEIVER (NON-INVERTING)

Description	No. of Output	Output	Device	Technology																			
				Bipolar				CMOS				BiCMOS				Advanced CMOS							
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LY	LVC	ALVC	AVC
NON-INVERTING	12/24	3S	16268																		X		
		3S	16289																			○	
		3S	16270																			H○/HR○/A	
		3S	16271																			H○	
		3S	16272																			X	
		3S	162268																			H○	
	16/32	3S	162269																			H○	
		3S	162280																				
	16	3S	16245									○/A/ H○	○/B/ H○/A	H○	○	○	○	*	○	○/A/ HR○/A/ Z○/A	H○/○ HR○	○	
		3S	16334																			○/H○	
		3S	16470									○						X				○	
		3S	16543									○	H○	*	X	X	○	○		○/H○/A	H○	○	
		3S	16623									○	H○	*	X	X	○	○		H○/A	H○	○	
		3S	16646									○	H○	*	X	X	○	○		H○/A	H○	○	
		3S	16652									○	H○	*	X	X	○	○		H○/A	H○	○	
		3S	16952									○	H○	*	X	X	○	○		H○/A	H○	○	
		R3S	162245									○/H○	○/A/ H○	H○							R○		
		R3S	164245																			○	○/H○
		R3S	162334																			○/H○	H○
		16X3	3S	32316									H○										
	16X3	3S	32318									H○											
	16-2P	3S	16687									○											
		3S	16833									○							X				
	18	3S	16853									○							X				
		3S	16472																X				
		3S	16474																X				
		3S	16500									○/B	H○										
		3S	16501									○	H○										
		3S	16525									○											
		3S	16600									○											
		3S	16601									○							H○				
		3S	16834									○											○
		3S	16863									○											H○
		3S	16901									○											H○
		R3S	162500									○											
		R3S	162501									○											
		R3S	162525									○											H○
		R3S	162600									○											
		R3S	162601									○											H○/HR○/X
		R3S	162634									○											○
		3S	16282																				H○
	18/36	R3S	162282																			H○/○	
	20	3S	16636																			H○/○	
		3S	16861																			H○/○	
	32	R3S	162636																			○/H○	
		3S	32543								H○											○/H○	
	36	3S	32952								X											○/H○	
		3S	32245								H○	H○										○/○/A	
	36	3S	32500								X											○/H○	
		3S	32501								H○											H○	

Explanatory notes [No. of Output] +P: With Parity Bit

[Output] 3S: 3-State Output R3S: Series Resistor and 3-State Output

OC: Open-Collector Output 3SOC: 3-State Output / Open-Collector Output

Status ○: Product available in technology indicated *: New product planned in technology indicated

X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC1xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT1xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

BUS TRANSCEIVER(INVERTING NON-INVERTING/INVERTING)

Description	No. of Output	Output	Device	Technology																				
				Bipolar				CMOS			BiCMOS				Advanced CMOS									
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	
INVERTING	4	3S	242		X																			
		3S	446		X																			
		3S	1242				X																	
		R3S	2242					X																
		3S	544						X						X/-		X/-							
		3S	471												X/-		X/-							
	3S	473												X/-		X/-								
	3S	475												X/-		X/-								
	OC	614					X																	
	3S	620			X		A	X	X	X/-	X/-	X/-	0		X/-		X/-							
	OC	622			X		X	X	X	X/-	X/-	X/-	0		X/-		X/-							
	3SOC	638			X		A/A1		A															
	3S	640			0/1		0/1		0	0/0	X/0	0/	0			X/-		X/-						
	OC	642			0/1		A/A1		X				X/-											
	3S	648			0		A		0	X/-	X/-	X/-			X/-		X/-							
	OC	649			X		X			X/-	X/-	X/-			X/-		X/-							
	3S	651			X		A	X		X/-	X/-	X/-	0		X/-		X/-							
	3SOC	653			X		0			X/-	X/-													
	3S	658								X/-	X/-													
	3S	664								X/-	X/-													
	3S	1640					X																	
	3S	2820					X																	
	3S	2640						X			X/-													
	3S	2953									X/-													
	3S	25620									X/-													
	3S	25622									X/-													
	3S	25640									X/-													
	3S	25642									0/													
	3S	25645									X/-													
	3S	25649									X/-													
	3S	25651									X/-													
	3S	25653									X/-													
	3SOC	334													X/-		X/-							
	3SOC	854													X/-		X/-							
	3SOC	29834					X				X/-													
	3SOC	29854					0				0/													
	3S	854													X/-		X/-							
	3S	29664					X				0/B/-				X/-		X/-							
	3S	862													X/-		X/-							
	3S	29962					X				X/B/-				X/-		X/-							
	3S	16471																						
	3S	16544																						
	3S	16820														X		X						
	3S	16640													0	X		X						
	3S	16648																X						
	3S	16651																0						
	3S	16862																		X				
	3S	16953																		X				
	3S	16475																				H/0		
	3S	16524																						
	3S	16964																	X					
	NON-INVERTING/INVERTING	8	3S	643		X		X	X	X/-	X/-					X/-		X/-						
			OC	644		X		X	X															
			OC	758				X	X															
			OC	759				X	X															
			3S	7340					X	X	X/-													

Explanatory notes [No. of Output] +P: With Parity Bit

[Output] 3S : 3-State Output R3S : Series Resistor and 3-State Output

OC : Open-Collector Output 3SOC : 3-State Output / Open-Collector Output

Status 0 : Product available in technology indicated * : New product planned in technology indicated

X : Discontinued █ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCTxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

SHIFT REGISTER

Input Type	Output Type	No. of Bit	CLR	Shift	Output	Device	Technology																		
							Bipolar					CMOS			BICMOS				Advanced CMOS						
							TTL	LS	S	ALS	AS	E	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC
S/P	S/P	4		R	2S	178	X																		
					2S	179	X																		
					2S	195	X	X		X			X/I/O												
					2S	95	X	X		X															
		5	C	R	2S	295	X	C																	
					3S	395	X	A																	
					2S	194	X	A		X			X/I/O	-I/O				X/I/-	X/I/-						
					2S	96	X	X		X															
		8	C	R	3S	322	X																		
					2S	196	X					X/-													
					3S	298	X	O	X	O	X	X/O	-I/O	X/-			X/I/-	X/I/-							
					3S	323	X		O	X	O	X/O	-I/O	X/-			X/I/-	X/I/-							
		C	B	2S	199	X																			

S/P	S	8		R	2S	165	X	A	O		X	O	-I/O											
				R	2S	166	X	A	O		X	O	-I/O										A	A

S	S/P	8	C	R	2S	184	X	O	A		O	-I/O					-I/-	-I/-					A
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S	P	10	C		2S	896											X/I/-	X/I/-						
---	---	----	---	--	----	-----	--	--	--	--	--	--	--	--	--	--	-------	-------	--	--	--	--	--	--

S	S	8		R	2S	91	X	X																
---	---	---	--	---	----	----	---	---	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--	--

P	S				4	C	R	2S	84	X														
---	---	--	--	--	---	---	---	----	----	---	--	--	--	--	--	--	--	--	--	--	--	--	--	--

					16		R	3S	674	O														
--	--	--	--	--	----	--	---	----	-----	---	--	--	--	--	--	--	--	--	--	--	--	--	--	--

SHIFT REGISTER WITH LATCH

Input Type	Output Type	No. of Bit	CLR	Shift	Output	Device	Technology																				
							Bipolar					CMOS			BICMOS				Advanced CMOS								
							TTL	LS	S	ALS	AS	E	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	
S/P	S/P	4	C	B	3S	671	X																				
					3S	672	X																				
		8	C	R	2S	595	O																				
					OC	596	X																				
					OC	596	O																				
					2S	594	O																				
16	C	B	3S	673	O																						

S/P	S	8	C	R	2S	597	O																	
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Explanatory notes [Input/Output Type] S: Serial P: Parallel S/P: Alternative Serial/Parallel

[CLR] C: With Clear

[Shift] R: Right-Shift B: Alternative Shift Right/Left

[Output] 2S: Totem-Pole Output 3S: 3-State Output

Status O: Product available in technology indicated * : New product planned in technology indicated

X: Discontinued ■ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCTxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

REGISTER(ETC)

Description	Device	Technology																				
		Bipolar				CMOS			BiCMOS			Advanced CMOS										
		TTL	LS	S	ALS	AB	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	
REGISTER FILES 8WX2B	172	X																				
REGISTER FILES 4WX4B	170	X	X																			
REGISTER FILES 4WX4B	670							-/0	-/0													
REGISTER FILES 16WX5B	870													X/J-L	X/J-L							
REGISTER FILES 16WX5B	856													X/J-L	X/J-L							
REGISTER FILES 16WX5B	871																					
REGISTER FILES 32WX4B	859				X	X								X/J-L	X/J-L							
MUX WITH STRAGE	298	X					CA	X/-														
MUX WITH STRAGE	398	X																				
4BIT BUS-BUFFER REGISTER	173	X	CA					X/J-	-/0													
8BIT STORAGE REGISTER	396	X																				
	818													X/J-L	X/J-L							
8BIT DIAGNOSTICS/PIPELINE REGISTER	819													X/J-L	X/J-L							
	28818				X					X/-												

Status ○ : Product available in technology indicated * : New product planned in technology indicated
 X : Discontinued ■ : Not recommended for new designs
 HC : SN74HCxx / CD74HCxx
 HCT : SN74HCTxx / CD74HCTxx
 BCT : SN74BCTxx / SN64BCTxx
 AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
 ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

MONOSTABLE MULTIVIBRATOR

Circuit	CLR	Retrigger	Device	Technology																		
				Bipolar				CMOS			BiCMOS			Advanced CMOS								
				TTL	LS	S	ALS	AB	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC
1			121																			
	C	R	122	X																		
	C	R	422	X																		
2	C	R	123						-/0	-/0						CA	CA	CA				
	C		221						-/0	-/0												
	C	R	423						-/0	-/0												
	C	R	4538						-/0	-/0												

Explanatory notes [CLR] C : With Clear
 [Retrigger] R : With Retrigger

Status ○ : Product available in technology indicated * : New product planned in technology indicated
 X : Discontinued ■ : Not recommended for new designs
 HC : SN74HCxx / CD74HCxx
 HCT : SN74HCTxx / CD74HCTxx
 BCT : SN74BCTxx / SN64BCTxx
 AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
 ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

RATE MULTIPLIER/FREQUENCY DIVIDERS

Description	Device	Technology																				
		Bipolar				CMOS			BiCMOS			Advanced CMOS										
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AMC	AMCT	LV	LVC	ALVC	AVC	
FREQUENCY DIVIDERS	56	X	X																			
FREQUENCY DIVIDERS	57	X	X																			
6BIT BINARY RATE MULTIPLIER	97	○																				
DECADE RATE MULTIPLIER	167	X																				
PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMERS	292	○																				
	294	○																				

Status ○ : Product available in technology indicated * : New product planned in technology indicated

X : Discontinued ■ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCTxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

DATA SELECTOR/MULTIPLEXER

No. of Input/output	Output	Circuit	ETC	Device	Technology																				
					Bipolar				CMOS			BiCMOS			Advanced CMOS										
					TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AMC	AMCT	LV	LVC	ALVC	AVC	
16/1	2S	1		150	○												X/H/-	X/H/-							
	3S	1		250							○/A						X/H/-	X/H/-							
	3S	1		650							X														
	3S	1		851							X														
	2S	1		4067							X/○														
8/1	2S	1		151	X/A	○	○	○	○	○	B	○/○	○/○				X/H/-	X/H/-							
	2S	1		152								X/-													
	3S	1		251	X	○	X	○	○	○	B	○/○	○/○				X/H/-	X/H/-							
	3S	1		354	X							X/○	○/○												
	3S	1		356	X							X/○	○/○												
	3S	1		4051								○/○	○/○									○/A			
	3S	1		4351							○/○	○/○													
	OC	1		355	X																				
	OC	1		357	X																				
4/1	2S	2		352	X	X	X	X	X	X	X/-						X/H/-	X/H/-							
	3S	2		153	X	○	X	○	○	○	X/A	○	○/○	○/○			X/H/-	X/H/-							
	3S	2		253	X	○	X	○	○	○	X/A	○	○/○	○/○			X/H/-	X/H/-							
	3S	2		353	X	X	X	X	X	X	X/-						X/H/-	X/H/-							
	3S	2		4052								○/○	○/○									○/A			
	3S	2		4352							○/○	○/○													
	3S	4		16460									H	○										X	
	3S	4		162460									H	○											
2/1	2S	1		157	X	○	○	○/A	○	○/A	○/○	○/○					X/H/-	X/H/-	○	○	○/A	○/A			
	2S	1		158	○	X	○	○	○	○	X/A	○/○	○/○				X/H/-	X/H/-	○	○	○/A	○/A			-
	2S	4	S	399																					
	3S	1		257				○/B	○/A	○	○/○	○/○					○/H/-	○/H/-					○/A		
	3S	1		259	○/B	X	○/A	○	○	○	○/○	○/○					X/H/-	X/H/-							-
	3S	4		4053								○/○	○/○												
	3S	6	U	657								○/○	○/○										○/A		
	3S	6	S	604	X							X													
	OC	6	S	605	X																				
	3S	6	S	606	X																				
	OC	6	S	607	X																				
16	3S	16	AD	16254																	X				

Explanatory notes [Output] 2S : Totem pole Output 3S : 3-State Output OC : Open-Collector Output

[ETC] S : Storage Register

Status ○ : Product available in technology indicated * : New product planned in technology indicated

X : Discontinued ■ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCTxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

DECODER/DEMULTIPLEXER

No. of Input/output	Output	Circuit	ETC	Device	Technology																	
					Bipolar					CMOS		BiCMOS		Advanced CMOS								
					TTL	LS	S	ALS	AS	E	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC
4/16	2S	1	AD	4514							X/O	-/O										
	2S	1	AD	4515							X/O	-/O										
	3S	1		154							X/O	-/O			X/H	X/H						
4/10	2S	1	BD	42	X/A	O					O/O	-/O										
	2S	1	BD	43	X																	
	2S	1	BD	44	X																	
3/8	2S	1		238							X/O	-/O			X/H/O	X/H/O						
	2S	1		138	O	O	O	O	O		O/O	-/O			X/H/O	X/H/O	O	O	O	O		
	2S	1	AD	237							X/O	-/O			X/H/O	X/H/O						
	2S	1	AD	137	X		O/A	X	X	X/O	X/O											
	2S	1	AD	131				O/A	X	X	X/O	X/O										
2/4	2S	2		139	O/A	O/A	O	X	X	O/O	O/O				X/H/O	O/H/O	O	O	O/A	O/A		
	2S	2		239							X/O	-/O			X/H	X/H						
	2S	2		155	X	O/A									X/H	X/H						
	OC	2		156	X	O		O														

Explanatory notes [Output] 2S: Totem pole Output 3S: 3-State Output OC: Open-Collector Output
[ETC] AD: Address Latch BD: BCD TO DECIMAL

Status O: Product available in technology indicated * : New product planned in technology indicate
X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74ACT1xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

CODE CONVERTER PRIORITY ENCODER/REGISTER

Description	Device	Technology																				
		Bipolar					CMOS		BiCMOS		Advanced CMOS											
		TTL	LS	S	ALS	AS	E	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	
CODE CONVERTER	184	X																				
CODE CONVERTER	185	X	X																			
10-4 PRIORITY ENCODER	147	X	X					-/O	-/O													
8-3 PRIORITY ENCODER	148	X					X	O/O														
8-3 PRIORITY ENCODER	348	O										X										
4BIT CASCADABLE PRIORITY REGISTER	278	X																				

Status O: Product available in technology indicated * : New product planned in technology indicate
X: Discontinued ■: Not recommended for new designs

HC: SN74HCxx / CD74HCxx

HCT: SN74HCTxx / CD74HCTxx

BCT: SN74BCTxx / SN64BCTxx

AC: 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT: 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

Display Decoder/Driver

Function	V _{OH} (V)	Device	Technology																				
			Bipolar			CMOS			BiCMOS			Advanced CMOS											
			TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	
D	30	45	○																				
D	60	141	×																				
D	15	145	○	○																			
D	7	445	○	×																			
7	30	46	×																				
7	15	47	○	○																			
7	5.5	48	×	×																			
7	5.5	49	×																				
7	30	246	×																				
7	15	247	×	○																			
7	7	347																					
7	7	447																					
7	5.5	248	×																				
7	5.5	249	×																				
B	7	142	×																				
B	7	143	×																				
B	7	144	×																				

Explanatory notes [Function] D : BCD TO DECIMAL, 7 : BCD TO 7-SEGMENT, B : COUNTER/LATCH/DECODER/DRIVER
[V_{OH}] Off-Stage Output Voltage(V)

Status ○ : Product available in technology indicated * : New product planned in technology indicated

× : Discontinued ■ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCTxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

COMPARATOR

No. of Bit	Input	P=Q	P<Q	P>Q	P<Q	Output	Device	Technology																				
								Bipolar			CMOS			BiCMOS			Advanced CMOS											
								TTL	LS	S	ALS	AS	L	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	
4	S	Y	N	Y	Y	ZS	85	×	○	○				×A/-	-/○													
6	S	N	Y	N	N	ZS	29806				×																	
8	20	Y	N	N	N	OC	518				○			×														
8	20	N	Y	N	N	ZS	520				○			×														
8	20	N	Y	N	N	OC	522				○																	
8	20	N	Y	Y	N	ZS	682				○			○/-														
8	20	N	Y	Y	N	OC	683				×																	
8	S	Y	N	N	N	OC	519																					
8	S	N	Y	N	N	ZS	521				×			×														
8	S	N	Y	Y	N	ZS	684				○			○/-														
8	S	N	Y	Y	N	OC	685				×																	
8	S	N	Y	Y	N	ZS	686				×																	
8	S	N	Y	Y	N	OC	687				×																	
8	S	N	Y	N	N	ZS	686				○			○/○	-/○													
8	S	N	Y	N	N	OC	689				×																	
8	S	Y	N	Y	Y	ZS	860																					
8	S	N	N	Y	Y	ZS	865																					
8	LP	N	N	Y	Y	ZS	865							○														
8	LPQ	Y	N	Y	Y	OC	866							×A														
9	-	N	Y	N	N	ZS	29809				×																	

Explanatory notes [Input] S : Standard 20 : 20-kW Pullup Resistors LP : P-Port Latch LPQ : L,P-port Latch
[Output] ZS : Totem Pole Output, OC : Open-Collector Output

Status ○ : Product available in technology indicated * : New product planned in technology indicated

× : Discontinued ■ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCTxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

ADDRESS COMPARATOR / FUSE-PROGRAMMABLE IDENTITY COMPARTOR

Description	No. of Bit	ETC	Device	Technology																		
				Bipolar				CMOS				BICMOS				Advanced CMOS						
				TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC
A	16-4	OE	677				X/A			X					X/-/	X/-/						
A	16-4	L	676				X			X					X/-/	X/-/						
A	12-4	OE	679				○			X												
A	12-4	L	680				X			X												
F	16		526				X															
F	12		528				X															
F	8		527				X															

Explanatory notes [Function] A : Address Comparator F : Fuse-Programmable Identity Comparators

[ETC] OE : Output-With Enable L : Output-With Latch

Status ○ : Product available in technology indicated * : New product planned in technology indicated

X : Discontinued ■ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCTxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

PARITY GENERATOR / CHECKER

No. of Bit	Device	Technology																				
		Bipolar				CMOS				BICMOS				Advanced CMOS								
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	
8	180	X							X													
9	280		○	○	○	○	○	○	X/○	-/○				X/-/○	X/-/○							
9	286								○	X				X/-/	○/-/							

Status ○ : Product available in technology indicated * : New product planned in technology indicated

X : Discontinued ■ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCTxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

VOLTAGE CONTROLLED OSCILLATOR(VCO)

Circuit	Fmax (MHz)	COMPL' 2 OUT	ENABLE	RANGE INPUT	Rest	PLL	Device	Technology															
								Bipolar				CMOS				BICMOS				Advanced CMOS			
								TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT
1	20	Y	Y	Y			624																
	20	Y	Y	Y	Y		626																
	24				Y	Y	7046																
2	20						627	X															
	20						629	○															
	20	Y		Y			625	X															
	20	Y	Y				626	X															
	60		Y	Y			124		○														
24					Y	Y	4046																

Status ○ : Product available in technology indicated * : New product planned in technology indicated

X : Discontinued ■ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCTxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

ACCUMULATORS, ARITHMETIC LOGIC UNIT(ALU), LOOK-AHEAD CARRY GENERATOR

Description	Device	Technology																				
		Bipolar				CMOS			BiCMOS			Advanced CMOS										
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	
4BIT PARALLEL BINARY ACCUMULATORS	281		X		X																	
4BIT PARALLEL BINARY ACCUMULATORS	681	X	X																			
4BIT ALU/FUNCTION GENERATORS	181	X	○				▲							X/J-/-	X/J-/-							
4BIT ALU/FUNCTION GENERATORS	381	X	X				▲															
4BIT ALU/FUNCTION GENERATORS	881						X▲															
4BIT ALU WITH RIPPLE CARRY	382	X						X						X/J-/-	X/J-/-							
LOOK AHEAD CARRY GENERATORS	264							X														
LOOK AHEAD CARRY GENERATORS	182	X		○				X														
LOOK AHEAD CARRY GENERATORS	282	X						X														
LOOK AHEAD CARRY GENERATORS	882						X▲							X/J-/-	X/J-/-							
QUAD SERIAL ADDER/SUBTRACTOR	385	X																				

Status ○ : Product available in technology indicated * : New product planned in technology indicated

X : Discontinued ■ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCTxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

ADDER

Description	Device	Technology																				
		Bipolar				CMOS			BiCMOS			Advanced CMOS										
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	
4BIT BINARY FULL ADDER	83	X	X																			
4BIT BINARY FULL ADDER	283	X	○				○	-/○	-/○					-/○	-/○							
DUAL CARRY SAVE FULL ADDER	183	X																				
GATED FULL ADDER	80	X																				
2BIT BINARY FULL ADDER	82	X																				

Status ○ : Product available in technology indicated * : New product planned in technology indicated

X : Discontinued ■ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCTxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

MULTIPLIER

Description	Device	Technology																				
		Bipolar				CMOS			BiCMOS			Advanced CMOS										
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	AVC	
2-4 PARALLEL BINARY MULTIPLIERS	261	X																				
4-4 PARALLEL BINARY MULTIPLIERS	284	X																				
4-4 PARALLEL BINARY MULTIPLIERS	285	X																				
2'S COMPLEMENT MULTIPLIERS	384	X																				

Status ○ : Product available in technology indicated * : New product planned in technology indicated

X : Discontinued ■ : Not recommended for new designs

HC : SN74HCxx / CD74HCxx

HCT : SN74HCTxx / CD74HCTxx

BCT : SN74BCTxx / SN64BCTxx

AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx

ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

MEMORY

Description	Device	Technology																			
		Bipolar				CMOS				BiCMOS				Advanced CMOS							
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	ANC
MEMORY REFRESH CONTROLLERS	600	X																			
MEMORY REFRESH CONTROLLERS	601	X																			
MEMORY REFRESH CONTROLLERS	603	X																			
MEMORY CYCLE CONTROLLER	608	X																			
MEMORY MAPPERS	612	X																			
MEMMORY MAPPERS	613	X																			
MEMMORY MAPPERS WITH LATCH	610	X																			
MEMMORY MAPPERS WITH LATCH	611	X																			
MULTI-MODE LATCH	412		X																		
3-8 MEMORY DECIDER	2414																				

Status ○ : Product available in technology indicated * : New product planned in technology indicate
 X : Discontinued ■ : Not recommended for new designs
 HC : SN74HCxx / CD74HCxx
 HCT : SN74HCTxx / CD74HCTxx
 BCT : SN74BCTxx / SN64BCTxx
 AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
 ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

CLOCK GENERATOR CIRCUIT

Description	Device	Technology																			
		Bipolar				CMOS				BiCMOS				Advanced CMOS							
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	ANC
QUAD COMPLEMENTARY-OUTPUT LOGIC	265	X																			
DUAL PULSE SYNCHRONIZERS/DRIVERS	120	X																			
CRYSTAL-CONTROLLED OSCILLATORS	320		X																		
CRYSTAL-CONTROLLED OSCILLATORS	321		X																		
DIGITAL PHASE-LOCK LOOP	297																				

Status ○ : Product available in technology indicated * : New product planned in technology indicate
 X : Discontinued ■ : Not recommended for new designs
 HC : SN74HCxx / CD74HCxx
 HCT : SN74HCTxx / CD74HCTxx
 BCT : SN74BCTxx / SN64BCTxx
 AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
 ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

SWITCH , SHIFTER , ERROR DETECTION CORRECTION CIRCUIT , HARD DISK DRIVER

Description	Device	Technology																			
		Bipolar				CMOS				BiCMOS				Advanced CMOS							
		TTL	LS	S	ALS	AS	F	HC	HCT	BCT	ABT	LVT	ALVT	AC	ACT	AHC	AHCT	LV	LVC	ALVC	ANC
QUAD BILATERAL SWITCHES	4016																				
QUAD BILATERAL SWITCHES	4066																				
ANALOG SWITCHES WITH LEVEL TRANSLATION	4316																				
4BIT SHIFTERS	350		X																		
8BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	636		X																		
8BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	637		X																		
8BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	616				X																
16BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	617		X																		
16BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	630		X																		
16BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	631		X																		
32BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	632				X	X															
32BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	633				X	X															
32BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	634				X	X															
32BIT PARALLEL ERROR DETECTION CORRECTION CIRCUIT	635				X	X															
HARD DISK DRIVER	1250				X																

Status ○ : Product available in technology indicated * : New product planned in technology indicate
 X : Discontinued ■ : Not recommended for new designs
 HC : SN74HCxx / CD74HCxx
 HCT : SN74HCTxx / CD74HCTxx
 BCT : SN74BCTxx / SN64BCTxx
 AC : 74AC11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACxx / CD74ACxx
 ACT : 74ACT11xxx (Product available in reduced-noise advanced CMOS: 11000 Series) / SN74ACTxx / CD74ACTxx

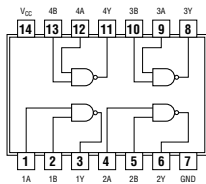
PIN ASSIGNMENTS

Pin Assignments

00

QUADRUPLE 2-INPUT POSITIVE-NAND GATES

positive logic:
 $Y = \overline{A \cdot B}$

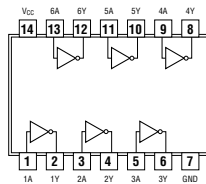


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04

HEX INVERTERS

positive logic:
 $Y = \overline{A}$

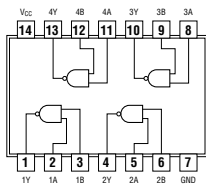


See page 143

01

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:
 $Y = \overline{A \cdot B}$

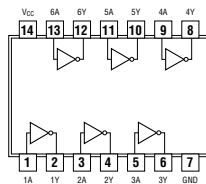


See page 140

U04

HEX INVERTERS

positive logic:
 $Y = \overline{A}$

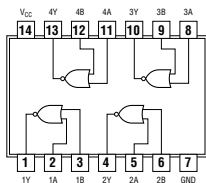


See page 144

02

QUADRUPLE 2-INPUT POSITIVE-NOR GATES

positive logic:
 $Y = \overline{A + B}$

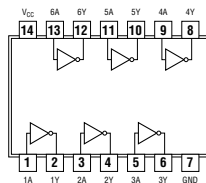


See page 141

05

HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:
 $Y = \overline{A}$

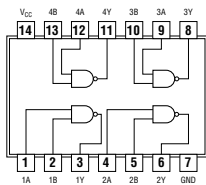


See page 144

03

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:
 $Y = \overline{A \cdot B}$

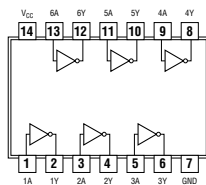


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06

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:
 $Y = \overline{A}$



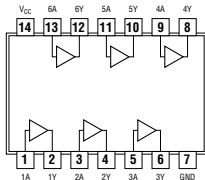
See page 145

Pin Assignments

07

HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:
 $Y = \bar{A}$

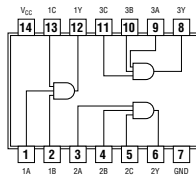


See page 145

11

TRIPLE 3-INPUT POSITIVE-AND GATES

positive logic:
 $Y = A \cdot B \cdot C$

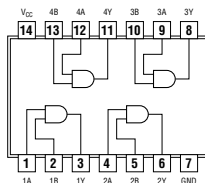


See page 149

08

QUADRUPLE 2-INPUT POSITIVE-AND GATES

positive logic:
 $Y = A \cdot B$

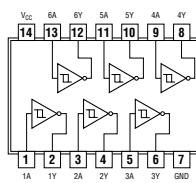


See page 146

14

HEX SCHMITT-TRIGGER INVERTERS

positive logic:
 $Y = \bar{A}$

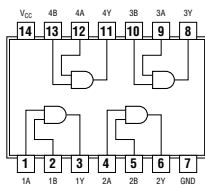


See page 150

09

QUADRUPLE 2-INPUT POSITIVE-AND GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:
 $Y = A \cdot B$

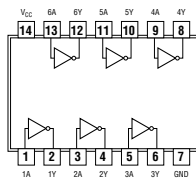


See page 147

16

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:
 $Y = \bar{A}$

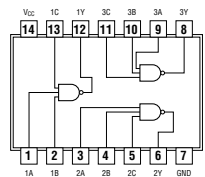


See page 151

10

TRIPLE 3-INPUT POSITIVE-NAND GATES

positive logic:
 $Y = \bar{A} \cdot \bar{B} \cdot \bar{C}$

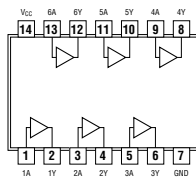


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17

HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

positive logic:
 $Y = A$



See page 151

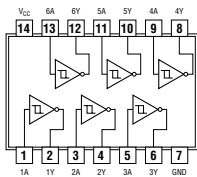
Pin Assignments

19

HEX SCHMITT-TRIGGER INVERTERS

positive logic:

$Y = A$



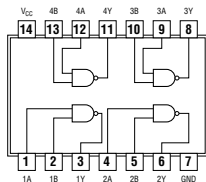
See page 152

26

QUADRUPLE 2-INPUT HIGH-VOLTAGE INTERFACE POSITIVE-NAND GATES

positive logic:

$Y = AB$



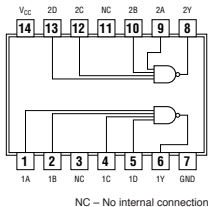
See page 155

20

DUAL 4-INPUT POSITIVE-NAND GATES

positive logic:

$Y = A \cdot B \cdot C \cdot D$



See page 153

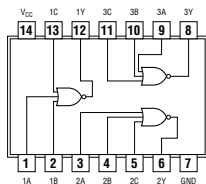
NC - No internal connection

27

TRIPLE 3-INPUT POSITIVE-NOR GATES

positive logic:

$Y = A + B + C$



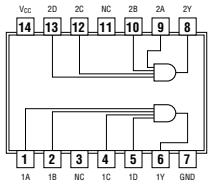
See page 155

21

DUAL 4-INPUT POSITIVE-AND GATES

positive logic:

$Y = A \cdot B \cdot C \cdot D$



See page 154

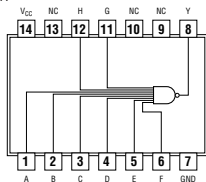
NC - No internal connection

30

8-INPUT POSITIVE-NAND GATES

positive logic:

$Y = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H$



See page 156

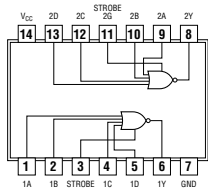
NC - No internal connection

25

DUAL 4-INPUT POSITIVE-NOR GATES WITH STROBE

positive logic:

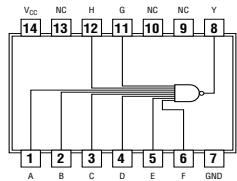
$Y = G(\bar{A} + B + C + D)$



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31

DELAY ELEMENTS



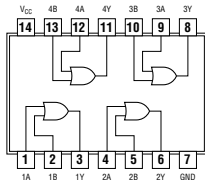
See page 156

NC - No internal connection

32

QUADRUPLE 2-INPUT POSITIVE OR GATES

positive logic:
 $Y = A + B$

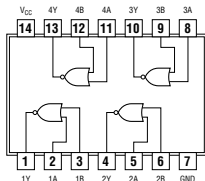


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33

QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:
 $Y = \overline{A + B}$

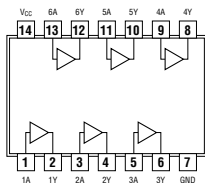


See page 158

35

HEX NONINVERTERS WITH OPEN-COLLECTOR OUTPUTS

positive logic:
 $Y = A$

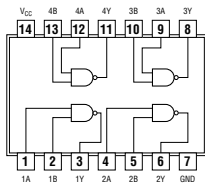


See page 158

37

QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS

positive logic:
 $Y = \overline{A \cdot B}$

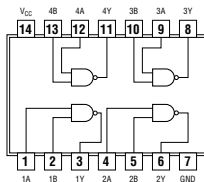


See page 159

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QUADRUPLE 2-INPUT POSITIVE-NAND BUFFERS WITH OPEN-COLLECTOR OUTPUTS

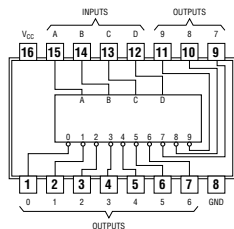
positive logic:
 $Y = \overline{A \cdot B}$



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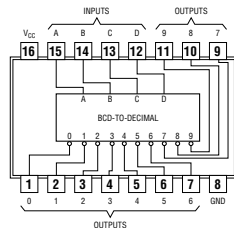
4-LINE-TO-10-LINE DECODERS



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45

BCD-TO-DECIMAL DECODER/DRIVER

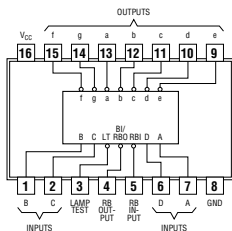


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Pin Assignments

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BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS



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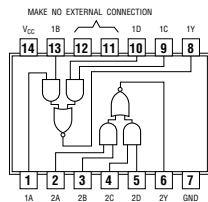
51

AND-OR-INVERT GATES

'S1, 'S51 DUAL 2-WIDE 2-INPUT

positive logic:

$$Y = AB + CD$$



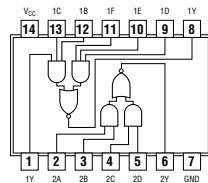
AND-OR-INVERT GATES

'LS51 2-WIDE 3-INPUT, 2-WIDE 2-INPUT

positive logic:

$$1Y = (1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)$$

$$2Y = (2A \cdot 2B) + (2C \cdot 2D)$$



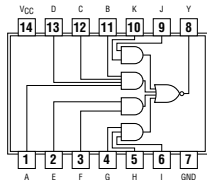
See page 166

64

4-2-3-2 INPUT AND-OR INVERT GATE

positive logic:

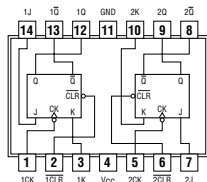
$$Y = ABCD + EF + GHI + JK$$



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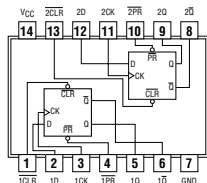
DUAL J-K FLIP-FLOPS WITH CLEAR



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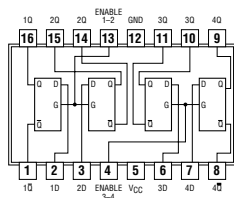
DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR



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75

4-BIT BISTABLE LATCHES

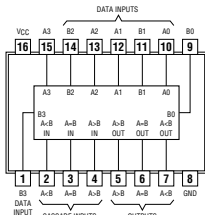


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Pin Assignments

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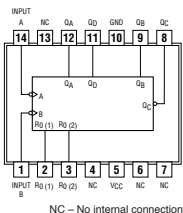
4-BIT MAGNITUDE COMPARATORS



See page 173

93

4-BIT BINARY COUNTERS



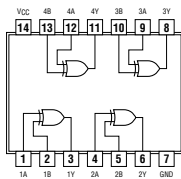
See page 177

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QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

positive logic:

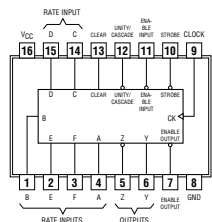
$$Y = A \oplus B \text{ or } Y = \bar{A}B + A\bar{B}$$



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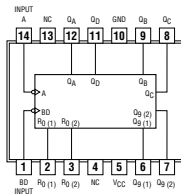
SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIER



See page 178

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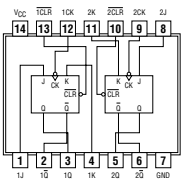
DECADE COUNTER



See page 175

107

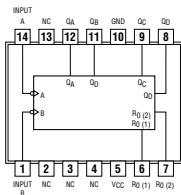
DUAL J-K FLIP-FLOPS WITH CLEAR



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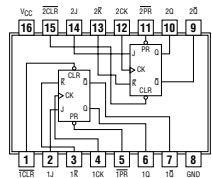
DIVIDE-BY-TWELVE COUNTERS



See page 176

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DUAL J-K POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

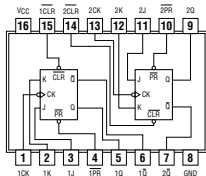


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Pin Assignments

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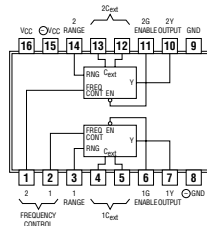
DUAL J-K NEGATIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR



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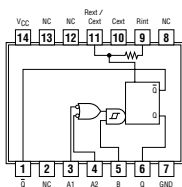
DUAL VOLTAGE-CONTROLLED OSCILLATORS WITH ENABLE INPUTS



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MONOSTABLE MULTIVIBRATOR



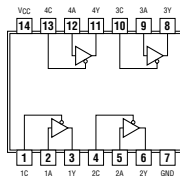
NC - No internal connection

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QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

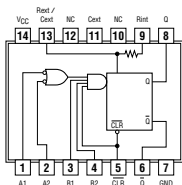
positive logic:
 $Y = A$



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RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR



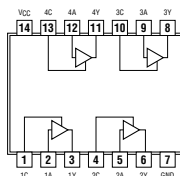
NC - No internal connection

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QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

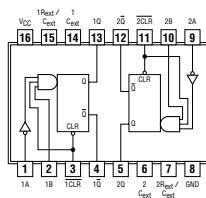
positive logic:
 $Y = A$



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DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

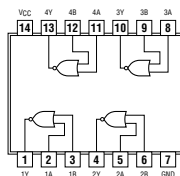


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SN54128...75-Ω LINE DRIVER
SN74128...50-Ω LINE DRIVER

positive logic:
 $Y = A + B$



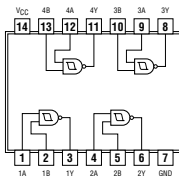
See page 192

Pin Assignments

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QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

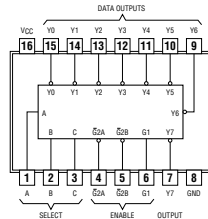
positive logic:
 $Y = A \cdot B$



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3-TO-8-LINE DECODERS/DEMULPLEXERS



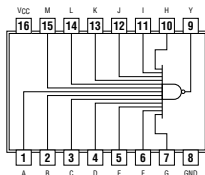
See page 196

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13-INPUT POSITIVE-NAND GATES

positive logic:

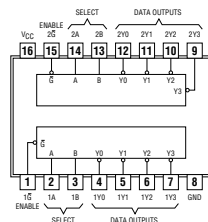
$$Y = A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M$$



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DUAL 2-TO-4-LINE DECODERS/DEMULPLEXERS



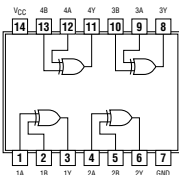
See page 198

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QUAD 2-INPUT EXCLUSIVE-OR GATES WITH OPEN COLLECTOR OUTPUTS

positive logic:

$$Y = A \oplus B = \bar{A}B + A\bar{B}$$



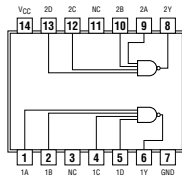
See page 193

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DUAL 4-INPUT POSITIVE-NAND 50-Ω LINE DRIVERS

positive logic:

$$Y = ABCD$$

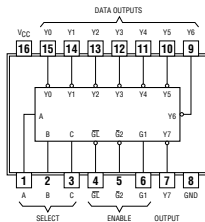


NC - No internal connection

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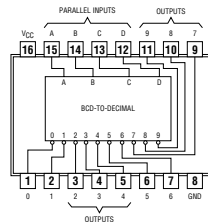
3-TO 8-LINE DECODERS/DEMULPLEXERS WITH ADDRESS LATCHES



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BCD-TO-DECIMAL DECODERS/DRIVERS FOR LAMPS, RELAYS, MOS

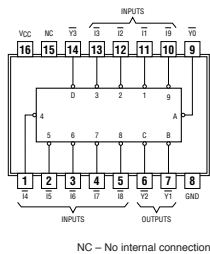


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Pin Assignments

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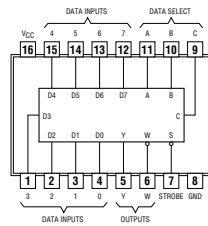
10-TO-4 LINE PRIORITY ENCODER



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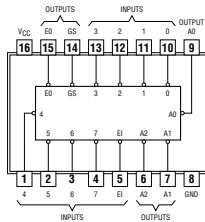
8-TO-1 LINE DATA SELECTORS/MULTIPLEXERS



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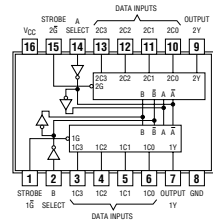
8-TO-3-LINE OCTAL PRIORITY ENCODERS



See page 204

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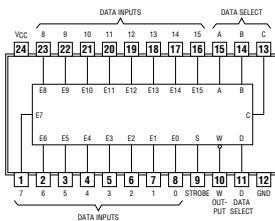
DUAL 4-LINE TO 1-LINE DATA SELECTORS/MULTIPLEXERS



See page 210

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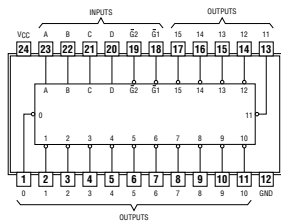
1-OF-16 DATA SELECTOR



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4-LINE TO 16-LINE DECODER/DEMULTIPLEXER



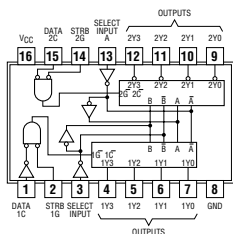
See page 212

Pin Assignments

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DECODERS/DEMULTEPLEXERS

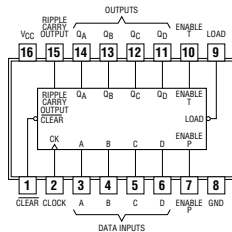


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SYNCHRONOUS 4-BIT BINARY COUNTERS

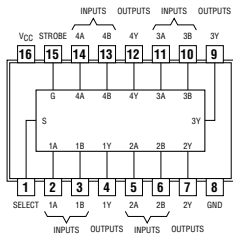


See page 224, 226

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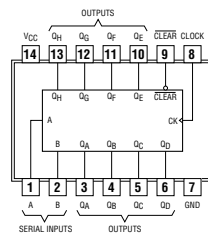
QUAD 2-TO 1-LINE DATA SELECTORS/MULTIPLEXERS



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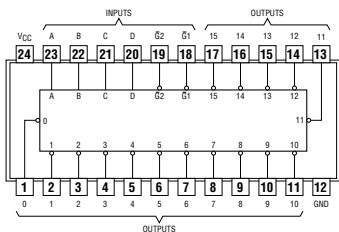
8-BIT PARALLEL OUTPUT SERIAL SHIFT REGISTERS



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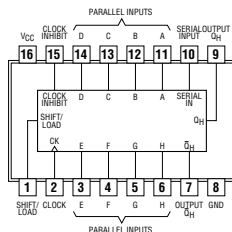
4-TO-16 LINE DECODER/DEMULTEPLEXER



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8-BIT SHFT REGISTERS

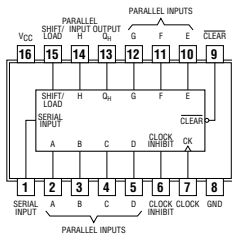


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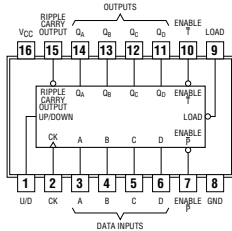
8-BIT SHIFT REGISTERS



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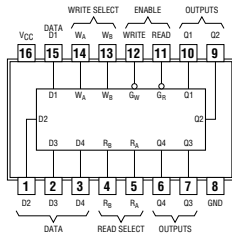
4-BIT UP/DOWN SYNCHRONOUS BINARY COUNTERS



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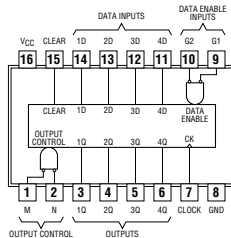
4-BY-4-REGISTER FILES



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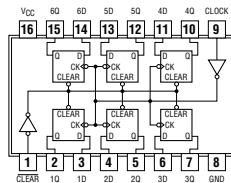
4-BIT D-TYPE REGISTERS



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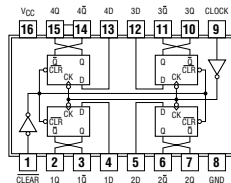
HEX D-TYPE FLIP-FLOPS



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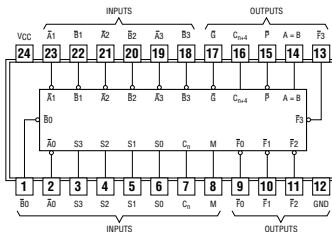
QUAD D-TYPE FLIP-FLOPS



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ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

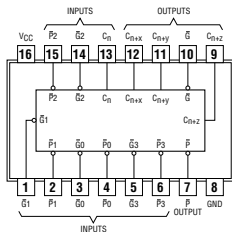


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Pin Assignments

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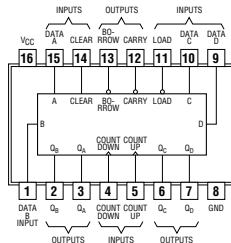
LOOK-AHEAD CARRY GENERATORS



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SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS

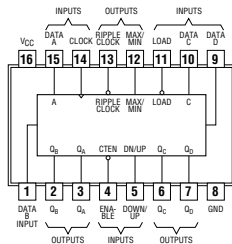


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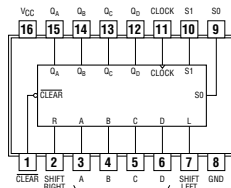
SYNCHRONOUS UP/DOWN DUAL CLOCK COUNTERS



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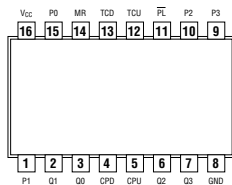
4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS



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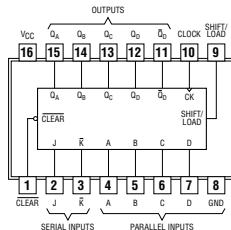
PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN COUNTERS



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4-BIT PARALLEL-ACCESS SHIFT REGISTERS

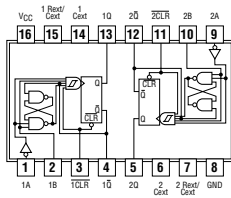


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Pin Assignments

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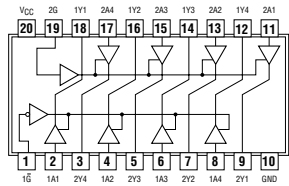
DUAL MONOSTABLE MULTIVIBRATORS



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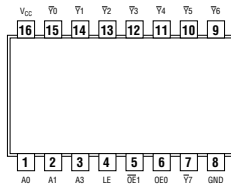
OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS



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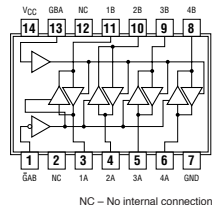
3-TO-8 LINE DECODER DEMULTIPLEXER WITH ADDRESS LATCHES



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QUADRUPLE BUS TRANSCEIVERS

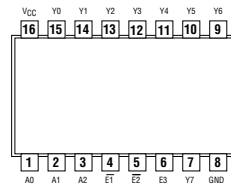


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NC – No internal connection

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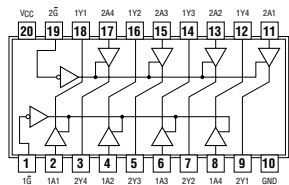
3-TO-8-LINE DECODERS/DEMULTIPLEXERS



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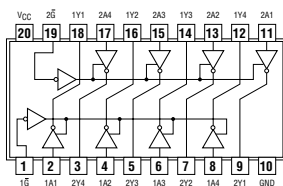
OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS



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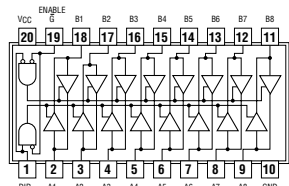
OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS



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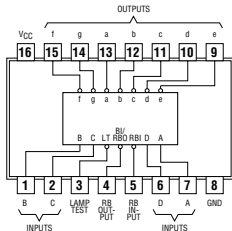
OCTAL BUS TRANSCEIVERS



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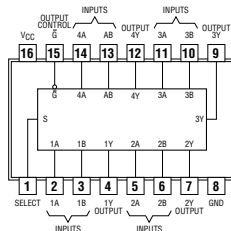
Pin Assignments

247 BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS WITH RIPPLE BLANKING



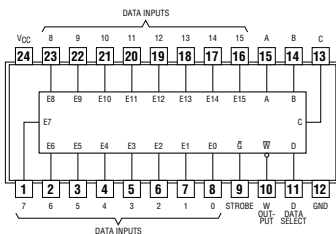
See page 274

257 QUAD DATA SELECTORS/MULTIPLEXERS



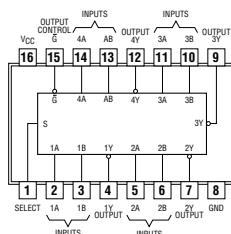
See page 282

250 1-OF-16 DATA GENERATOR/MULTIPLEXER



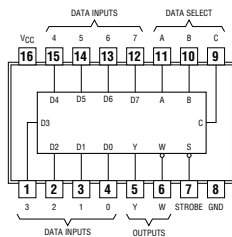
See page 276

258 QUAD DATA SELECTORS/MULTIPLEXERS



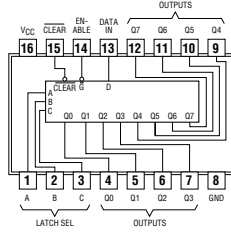
See page 284

251 DATA SELECTORS/MULTIPLEXERS



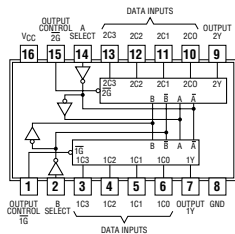
See page 278

259 8-BIT ADDRESSABLE LATCHES



See page 286

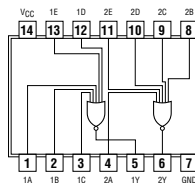
253 DUAL DATA SELECTORS/MULTIPLEXERS



See page 280

260 DUAL 5-INPUT POSITIVE-NOR GATES

positive logic:
 $Y = A + B + C + D + E$



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Pin Assignments

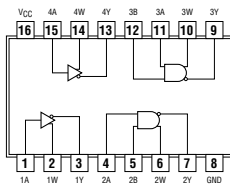
265

QUAD COMPLEMENTARY-OUTPUT ELEMENTS

positive logic:

$$Y = \bar{A}, W = A$$

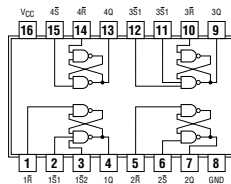
$$Y = AB, W = AB$$



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QUAD S-R LATCHES



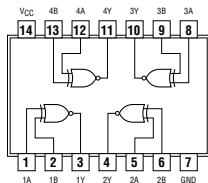
See page 293

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QUAD 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

positive logic:

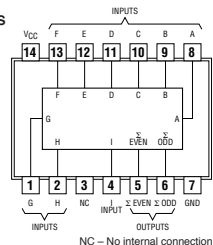
$$Y = A \oplus B$$



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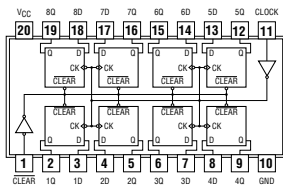
9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS



See page 294

273

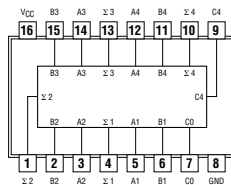
OCTAL D-TYPE FLIP-FLOPS



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283

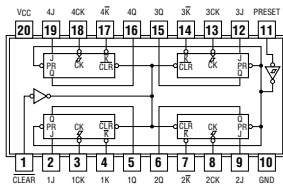
4-BIT BINARY FULL ADDERS



See page 296

276

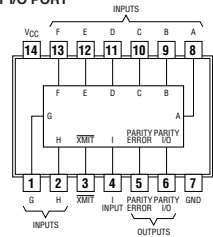
QUAD J-K FLIP-FLOPS



See page 292

286

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS WITH BUS DRIVER PARITY I/O PORT

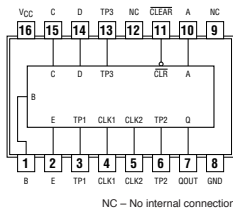


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Pin Assignments

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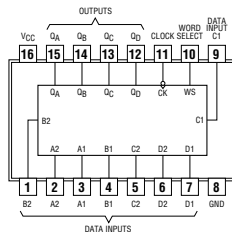
PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMER



See page 300

298

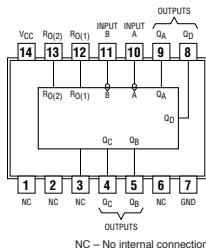
QUAD 2-INPUT MULTIPLEXERS WITH STORAGE



See page 308

293

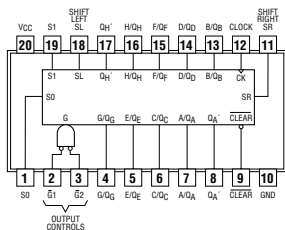
4-BIT BINARY COUNTERS



See page 302

299

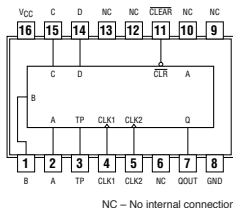
8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTERS



See page 310

294

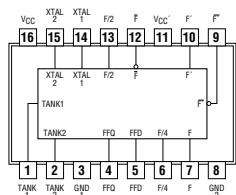
PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMER



See page 304

321

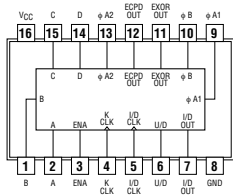
CRYSTAL-CONTROLLED OSCILLATOR



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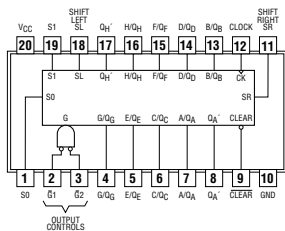
DIGITAL PHASE-LOCKED-LOOP FILTERS



See page 306

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8-BIT BIDIRECTIONAL SHIFT/STORAGE REGISTERS

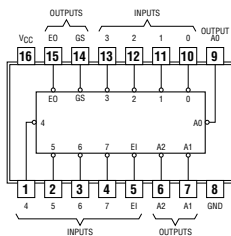


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Pin Assignments

348

8-LINE TO 3-LINE PRIORITY ENCODER

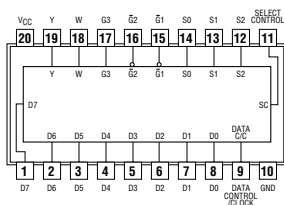


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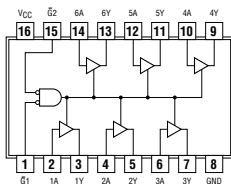
8-INPUT MULTIPLEXERS/REGISTERS 3-STATE



See page 318, 320

365

HEX BUS DRIVERS

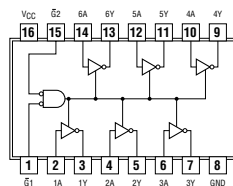


See page 322

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HEX BUS DRIVERS

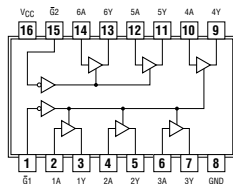
HEX BUFFERS/LINE DRIVERS 3-STATE



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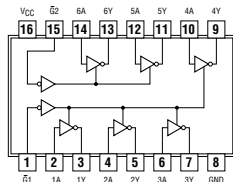
HEX BUS DRIVERS



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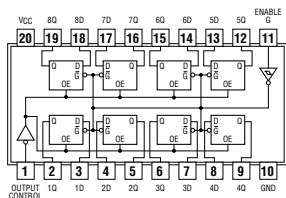
HEX BUS DRIVERS



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OCTAL D-TYPE LATCHES

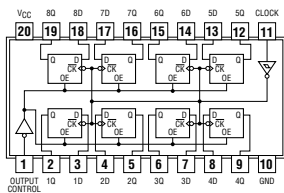


See page 325

Pin Assignments

374

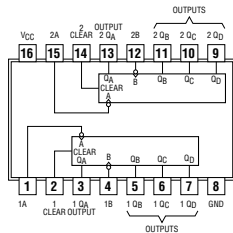
OCTAL D-TYPE FLIP-FLOPS



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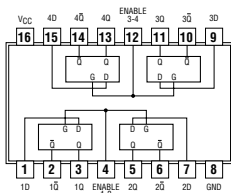
DUAL DECADE COUNTERS



See page 330

375

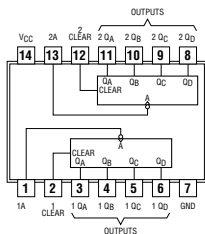
4-BIT BISTABLE LATCHES



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393

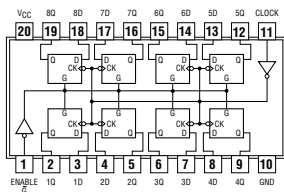
DUAL 4-BIT BINARY COUNTERS



See page 331

377

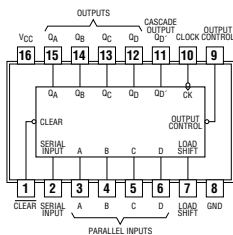
OCTAL D-TYPE FLIP-FLOPS



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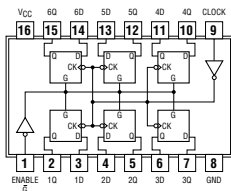
4-BIT UNIVERSAL SHIFT REGISTERS



See page 332

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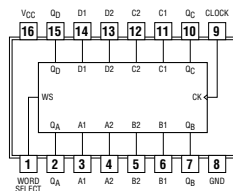
HEX D-TYPE FLIP-FLOPS



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QUAD 2-INPUT MULTIPLEXER WITH STORAGE



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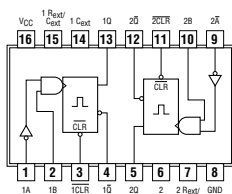
Pin Assignments

423

RE-TRIGGERABLE MONO-STABLE MULTIVIBRATOR

positive logic:

$Y = A$

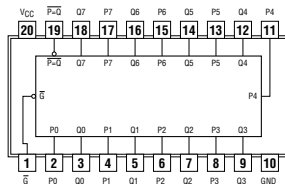


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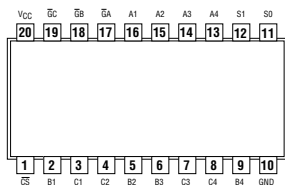
8-BIT IDENTITY COMPARATOR



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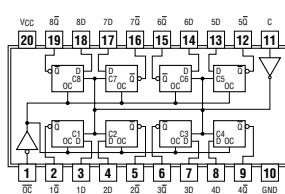
QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS



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533

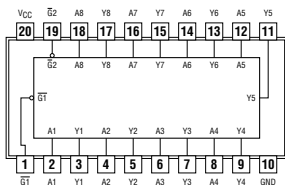
OCTAL D-TYPE TRANSPARENT LATCHES



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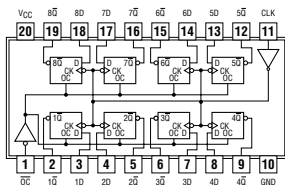
OCTAL BUFFERS WITH 3-STATE OUTPUTS



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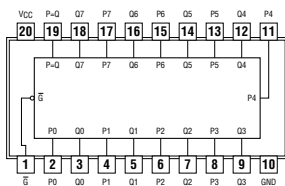
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS



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8-BIT IDENTITY COMPARATOR

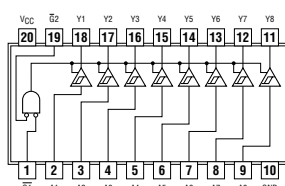


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OCTAL BUFFERS AND LINE DRIVERS

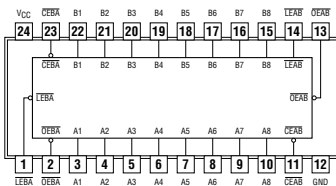


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Pin Assignments

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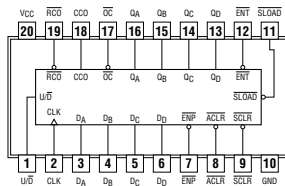
OCTAL REGISTERED TRANSCIEVERS



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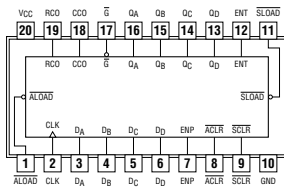
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS



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561

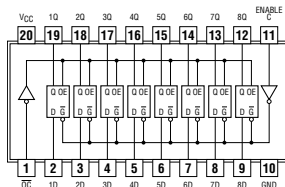
SYNCHRONOUS 4-BIT COUNTER



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573

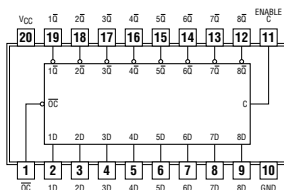
OCTAL D-TYPE TRANSPARENT LATCHES



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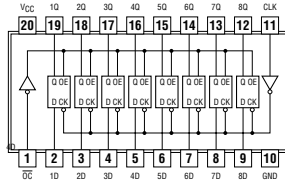
OCTAL D-TYPE TRANSPARENT LATCHES WITH INVERTED OUTPUTS



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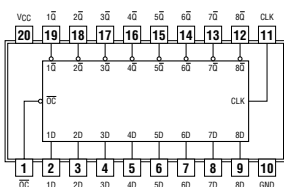
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS



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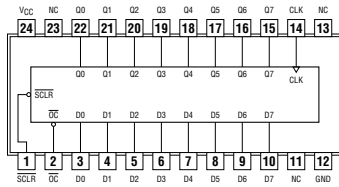
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS



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OCTAL D-TYPES EDGE-TRIGGERED FLIP-FLOPS



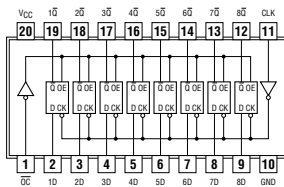
NC - No internal connection

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Pin Assignments

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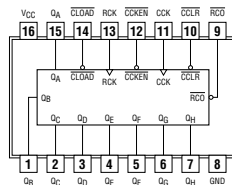
OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS



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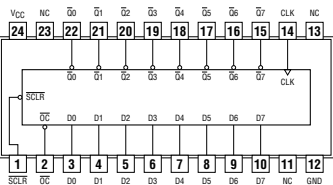
8-BIT BINARY COUNTER WITH INPUT REGISTER



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OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

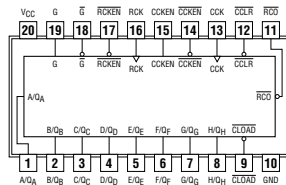


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NC – No internal connection

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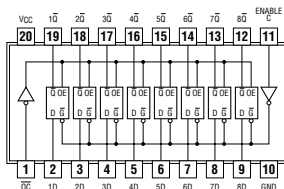
8-BIT BINARY COUNTER WITH INPUT REGISTER



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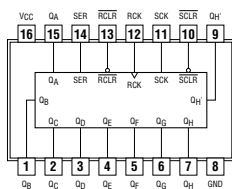
OCTAL D-TYPE TRANSPARENT LATCHES WITH INVERTED OUTPUTS



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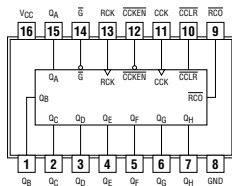
8-BIT SHIFT REGISTER WITH OUTPUT LATCH



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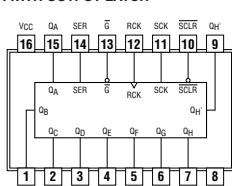
8-BIT BINARY COUNTER WITH OUTPUT REGISTER



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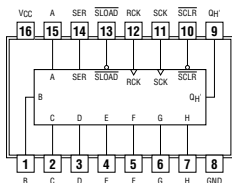
8-BIT SHIFT REGISTER WITH OUTPUT LATCH



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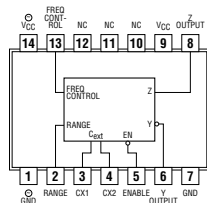
8-BIT SHIFT REGISTER WITH INPUT LATCH



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VOLTAGE-CONTROLLED OSCILLATOR

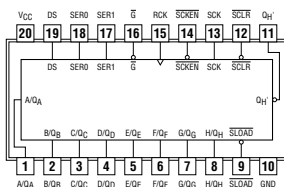


NC – No internal connection

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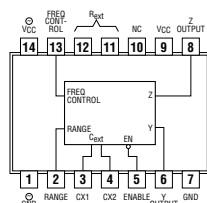
8-BIT SHIFT REGISTERS



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VOLTAGE-CONTROLLED OSCILLATOR



NC – No internal connection

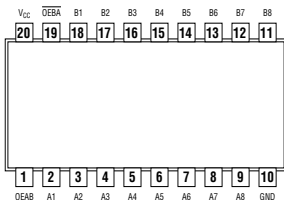
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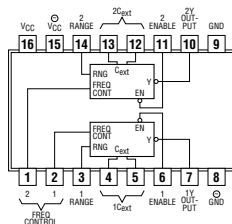
OCTAL BUS TRANSCEIVERS



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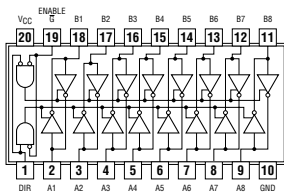
VOLTAGE-CONTROLLED OSCILLATOR



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OCTAL BUS TRANSCEIVERS

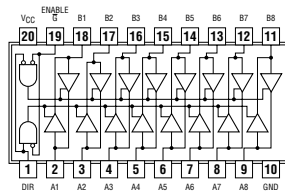


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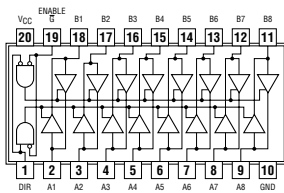
OCTAL BUS TRANSCEIVERS



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OCTAL BUS TRANSCEIVERS



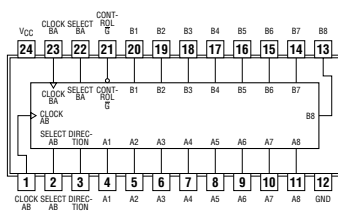
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OCTAL BUS TRANSCEIVERS AND REGISTERS

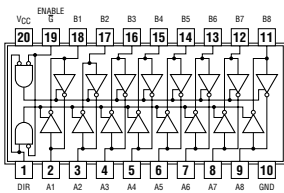


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OCTAL BUS TRANSCEIVERS



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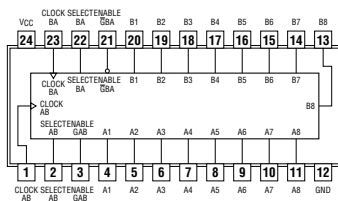
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654

OCTAL BUS TRANSCEIVERS AND REGISTERS

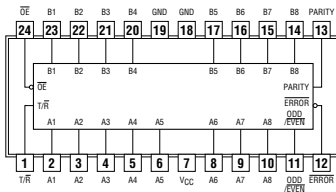


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Pin Assignments

657

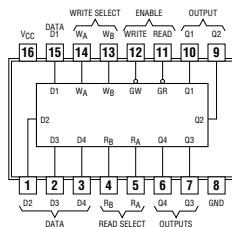
OCTAL BUS TRANSCEIVERS
WITH 8-BIT PARITY GENERATORS/CHECKERS



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670

4-BY-4 REGISTER FILE

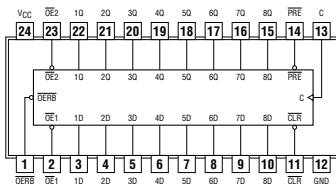


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666

667

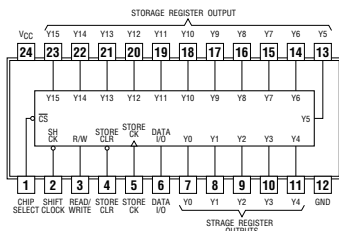
8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES



See page 408, 410

673

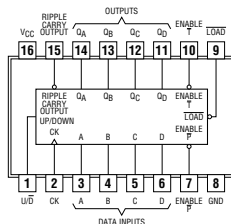
16-BIT SHIFT REGISTER



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669

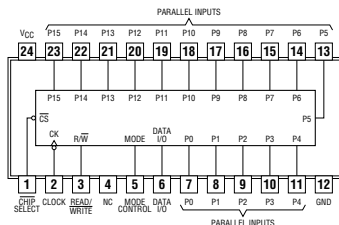
SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTER



See page 412

674

16-BIT SHFT REGISTER



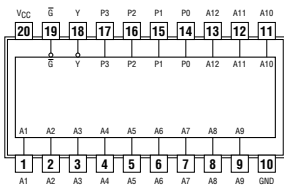
See page 418

NC - No internal connection

Pin Assignments

679

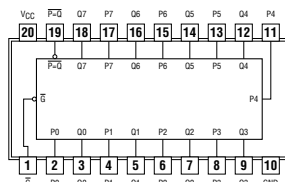
ADDRESS COMPARATOR



See page 420

688

8-BIT IDENTITY COMPARATOR

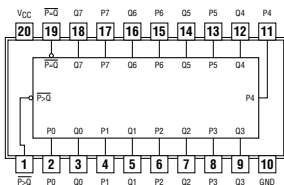


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682

684

8-BIT IDENTITY COMPARATOR

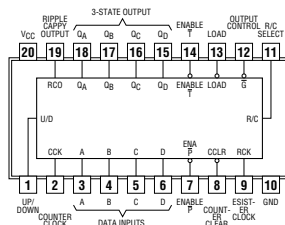


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697

699

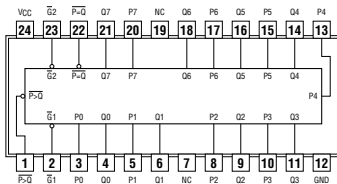
SYNCHRONOUS UP/DOWN COUNTER WITH OUTPUT REGISTER, MULTIPLEXED THREE-STATE OUTPUT



See page 430, 432

686

8-BIT IDENTITY COMPARATOR

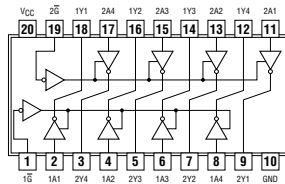


NC – No internal connection

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756

OCTAL BUFFER/LINE DRIVER/LINE RECEIVER WITH OPEN-COLLECTOR OUTPUTS

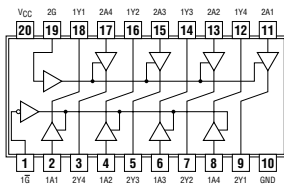


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Pin Assignments

757

**OCTAL BUFFER/LINE DRIVER/LINE RECEIVER
WITH OPEN-COLLECTOR OUTPUTS**

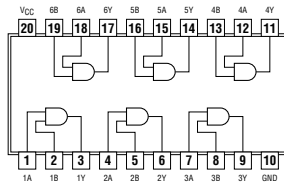


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808

HEX 2-INPUT AND DRIVERS

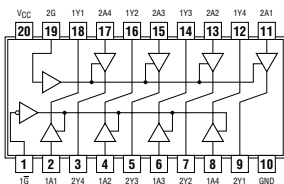
positive logic:
 $Y = A + B$



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760

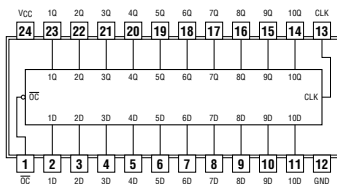
**OCTAL BUFFER/LINE DRIVER/LINE RECEIVER
WITH OPEN-COLLECTOR OUTPUTS**



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821

**10-BIT BUS INTERFACE FLIP FLOPS
WITH 3-STATE OUTPUT**

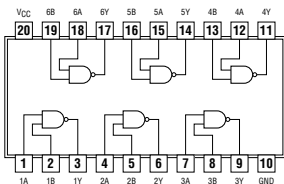


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804

HEX 2-INPUT NAND DRIVERS

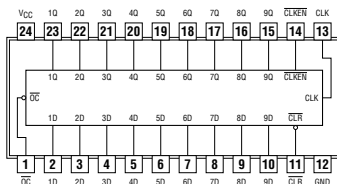
positive logic:
 $A = \overline{A \cdot B}$



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823

**9-BIT BUS INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUT**

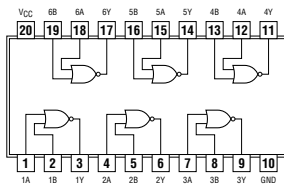


See page 440

805

HEX 2-INPUT NOR DRIVERS

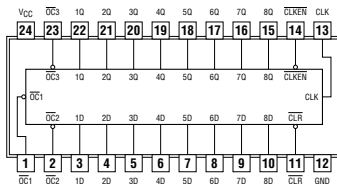
positive logic:
 $Y = \overline{A + B}$



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825

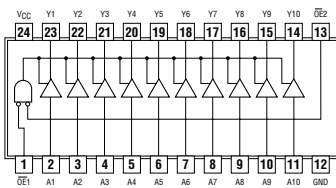
**8-BIT BUS INTERFACE FLIP-FLOP
WITH 3-STATE OUTPUT**



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827

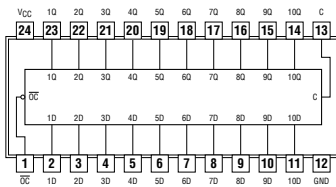
10-BIT BUFFER/BUS DRIVERS



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841

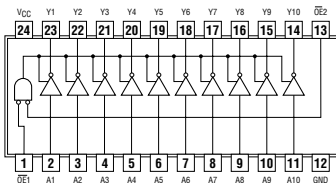
10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



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828

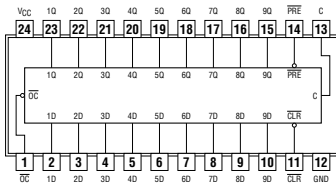
10-BIT BUFFERS/BUS DRIVERS



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843

9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS



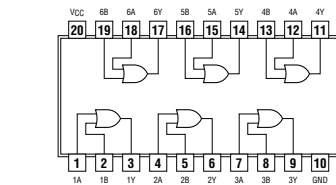
See page 450

832

HEX 2-INPUT OR DRIVERS

positive logic:

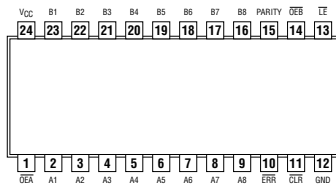
$$Y=A+B$$



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853

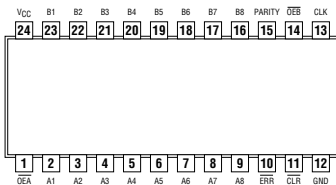
8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS



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833

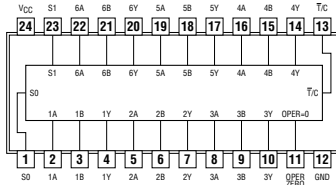
10-BIT TO 9-BIT PARITY BUS TRANSCEIVERS



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857

HEX 2-TO-1 UNIVERSAL MULTIPLEXERS

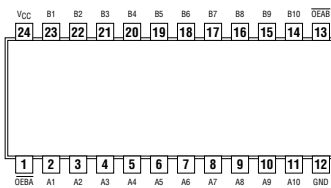


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Pin Assignments

861

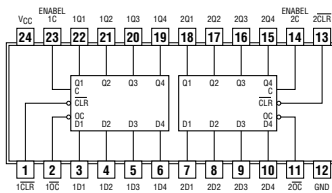
10-BIT TRANSCEIVERS WITH 3-STATE OUTPUTS



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873

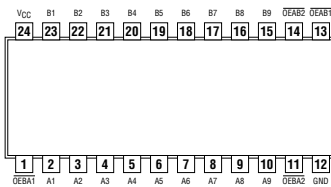
DUAL 4-BIT D-TYPE LATCHES



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863

9-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

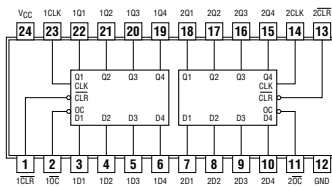


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NC – No internal connection

874

DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS



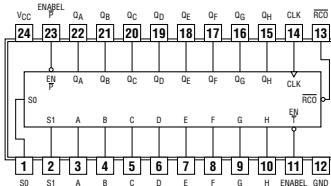
See page 465

NC – No internal connection

867

869

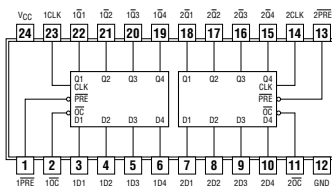
8-BIT SYNCHRONOUS BIDIRECTIONAL COUNTER



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876

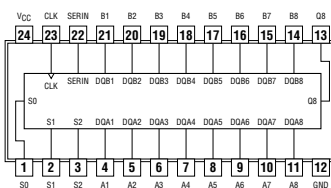
DUAL 4-BIT D-TYPE FLIP-FLOPS



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870

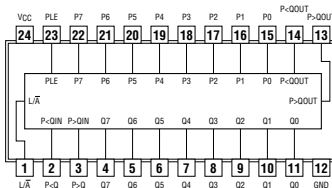
DUAL 16-BY 4-BIT REGISTER FILES



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885

8-BIT MAGNITUDE COMPARATOR

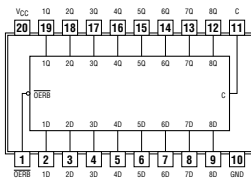


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Pin Assignments

990

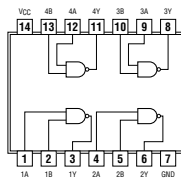
8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES



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1000

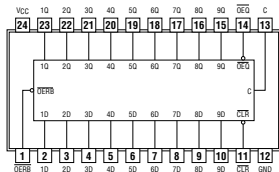
QUAD 2-INPUT NAND BUFFERS/DRIVERS



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992

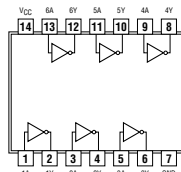
9-BIT D-TYPE TRANSPARENT



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1004

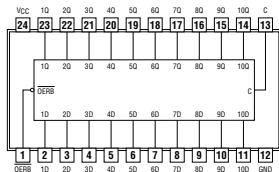
HEX INVERTING DRIVERS



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994

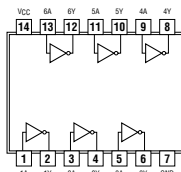
10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES



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1005

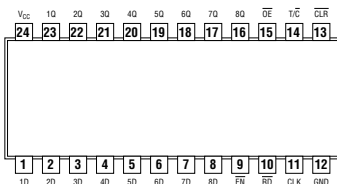
HEX INVERTING BUFFER GATES WITH OPEN-COLLECTOR OUTPUTS



See page 477

996

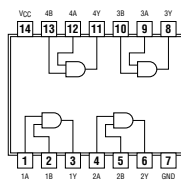
8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES



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1008

QUADRUPLE 2-INPUT POSITIVE-AND BUFFERS/DRIVERS



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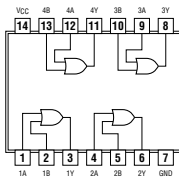
Pin Assignments

1032

QUAD 2-INPUT OR BUFFERS/DRIVERS

positive logic:

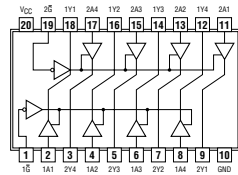
$$Y = A+B$$



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1244

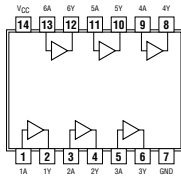
OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS



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1034

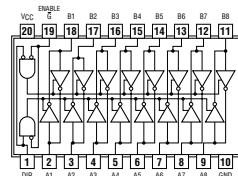
HEX DRIVERS



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1245

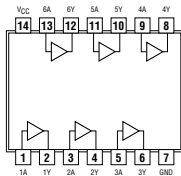
OCTAL BUS TRANSCEIVERS



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1035

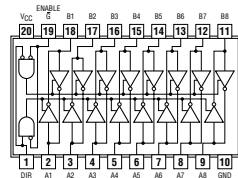
HEX BUFFERS WITH OPEN-COLLECTOR OUTPUTS



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1640

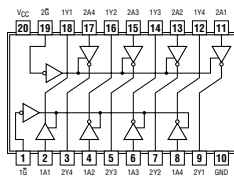
OCTAL BUS TRANSCEIVERS



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1240

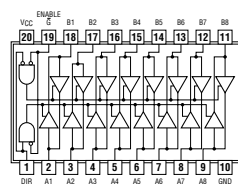
OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS



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1645

OCTAL BUS TRANSCEIVERS

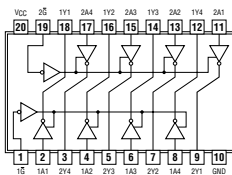


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Pin Assignments

2240

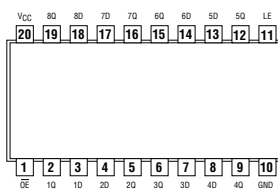
OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS



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2373

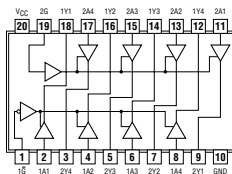
25-Ω OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS



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2241

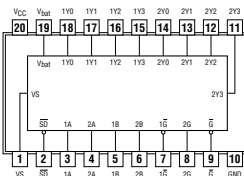
OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS



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2414

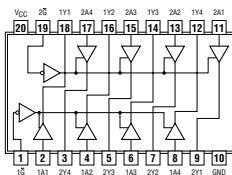
MEMORY DECODER WITH ON-CHIP V_{CC} MONITOR



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2244

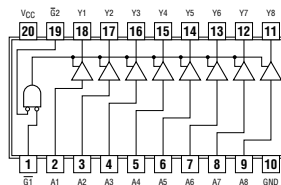
OCTAL BUFFERS AND LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS



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2541

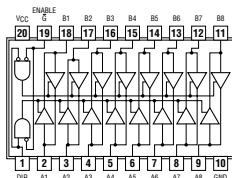
NON-INVERTED 3-STATE OUTPUTS
OCTAL LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS



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2245

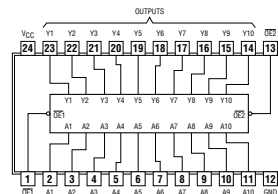
OCTAL TRANSCIVER AND LINE/MOS DRIVERS WITH 3-STATE OUTPUTS



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2827 3-STATE OUTPUTS

2828 3-STATE INVERTING OUTPUTS
BUS/MOS MEMORY DRIVERS

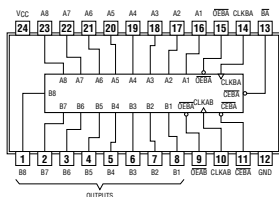


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Pin Assignments

2952

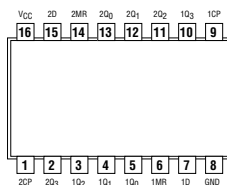
OCTAL BUS TRANSCEIVERS AND REGISTERS



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4015

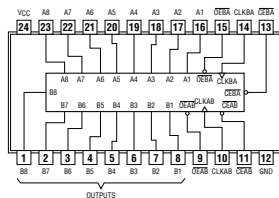
DUAL 4-STAGE STATIC SHIFT REGISTER



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2953

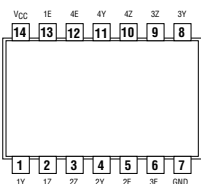
OCTAL BUS TRANSCEIVERS AND REGisters



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4016

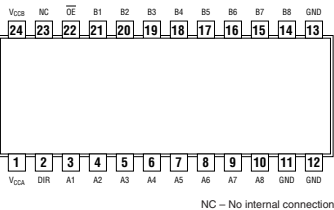
QUAD BILATERAL SWITCH



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3245

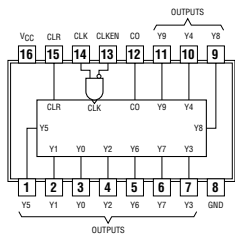
OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS



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4017

DECADE COUNTERS/DIVIDERS

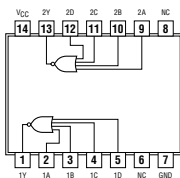


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4002

DUAL 4-INPUT POSITIVE-NOR GATES

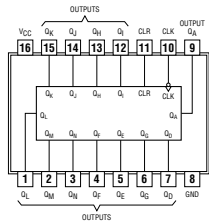
positive logic:
 $Y = \overline{A + B + C + D}$



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4020

14-STAGE BINARY COUNTERS

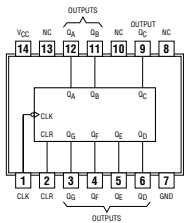


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Pin Assignments

4024

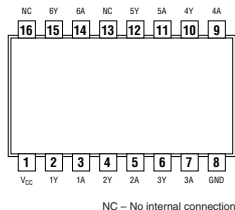
7-STAGE BINARY COUNTERS



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4050

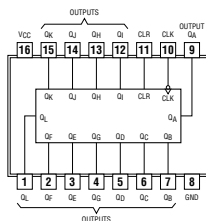
HEX INVERTING BUFFERS NON-INVERTING



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4040

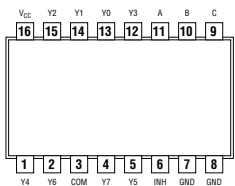
12-STAGE BINARY COUNTERS



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4051

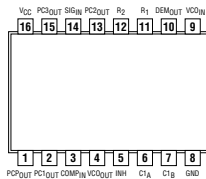
8-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS



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4046

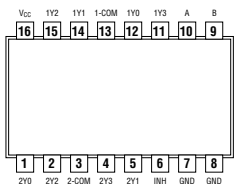
PHASE-LOCKED-LOOP WITH VCO



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4052

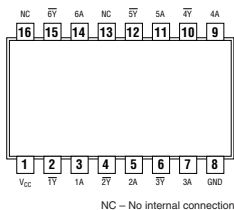
DUAL 4-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS



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4049

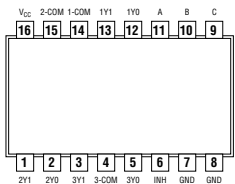
HEX INVERTING BUFFERS



See page 506

4053

TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

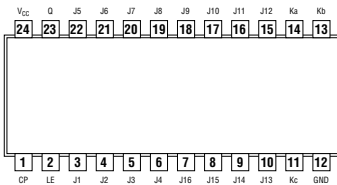


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Pin Assignments

4059

CMOS PROGRAMMABLE DIVIDE-BY-N COUNTER

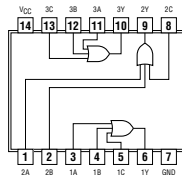


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4075

TRIPLE 3-INPUT OR GATES

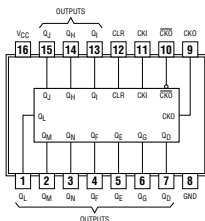
positive logic:
 $Y = A + B + C$



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4060

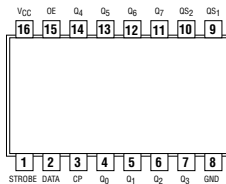
ASYNCHRONOUS 14-STAGE BINARY COUNTERS AND OSCILLATORS



See page 511

4094

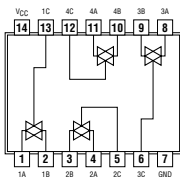
8-STAGE SHIFT AND STORE BUS REGISTER, THREE-STATE



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4066

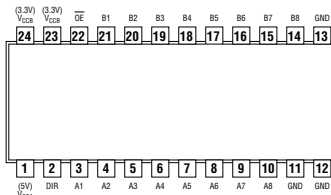
QUADRUPLE BILATERAL SWITCHES



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4245

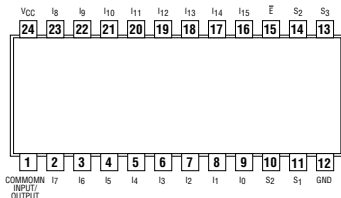
OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS



See page 518

4067

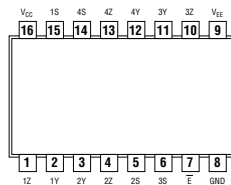
16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER



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4316

QUAD ANALOG SWITCH WITH LEVEL TRANSLATION

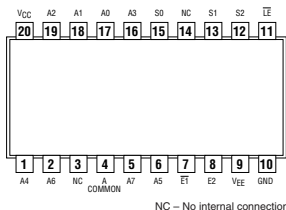


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Pin Assignments

4351

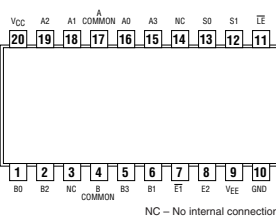
ANALOG MULTIPLEXERS/DEMULPLEXERS WITH LATCH



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4352

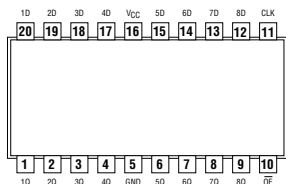
ANALOG MULTIPLEXERS/DEMULPLEXERS WITH LATCH



See page 521

4374

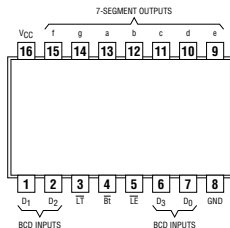
OCTAL EDGE-TRIGGERED D-TYPE DUAL-RANK FLIP-FLOP WITH 3-STAE OUTPUTS



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4511

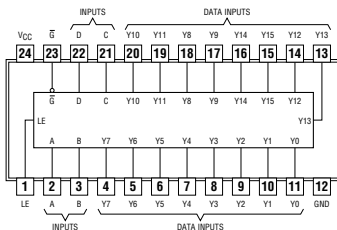
BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS



See page 523

4514

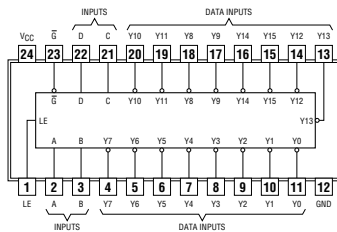
4-LINE TO 16-LINE DECODERS/DEMULPLEXERS WITH LATCHES



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4515

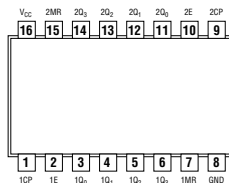
4-LINE TO 16-LINE DECODERS/DEMULPLEXERS WITH LATCHES



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4518

DUAL SYNCHRONOUS COUNTERS

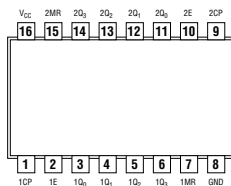


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Pin Assignments

4520

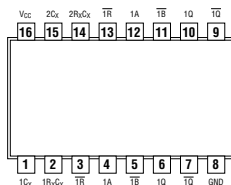
DUAL SYNCHRONOUS COUNTERS



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4538

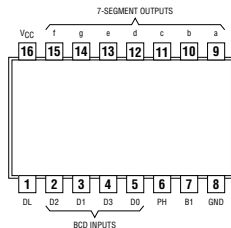
DUAL RETRIGGERABLE
PRECISION MONO STABLE MULTIVIBRATOR



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4543

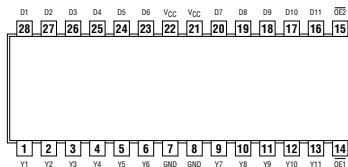
BCD-TO-7 SEGMENT LATCH/DECODER/DRIVERS



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5400

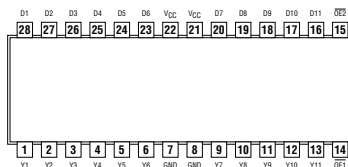
11-BIT LINE/MEMORY DRIVERS
WITH 3-STATE OUTPUTS



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5401

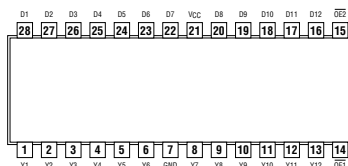
11-BIT LINE/MEMORY DRIVERS
WITH 3-STATE OUTPUTS



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5402

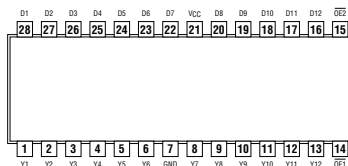
12-BIT LINE/MEMORY DRIVERS
WITH 3-STATE OUTPUTS



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5403

11-BIT LINE/MEMORY DRIVERS
WITH 3-STATE OUTPUTS



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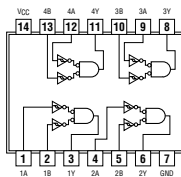
Pin Assignments

7001

QUADRUPLE POSITIVE-AND GATES WITH SCHMITT-TRIGGER INPUTS

positive logic:

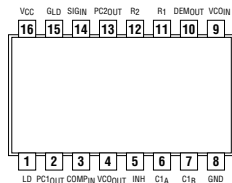
$$Y = A \cdot B$$



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7046

PHASE-LOCKED LOOP WITH VCO AND LOCK DETECTOR



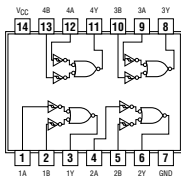
See page 538

7002

QUADRUPLE POSITIVE-NOR GATES WITH SCHMITT-TRIGGER INPUTS

positive logic:

$$Y = \overline{A + B}$$



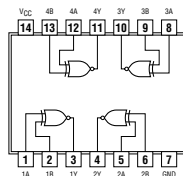
See page 536

7266

QUAD 2-INPUT EXCLUSIVE-NOR GATES

positive logic:

$$Y = A \oplus B$$



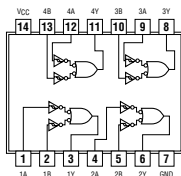
See page 539

7032

QUADRUPLE POSITIVE-OR GATES WITH SCHMITT-TRIGGER INPUTS

positive logic:

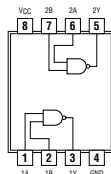
$$Y = A + B$$



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8003

DUAL 2-INPUT POSITIVE-NAND GATES

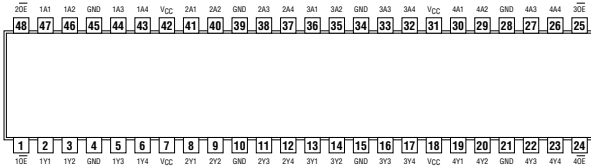


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Pin Assignments

16240

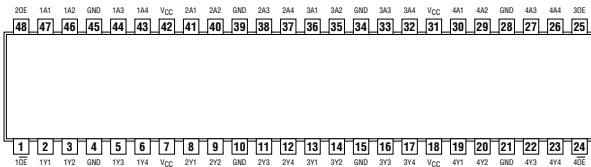
16-BIT BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



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16241

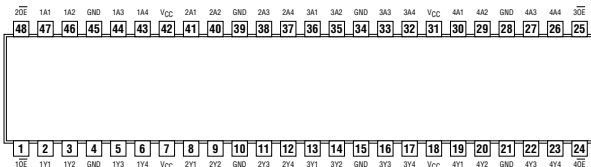
16-BIT BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



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16244

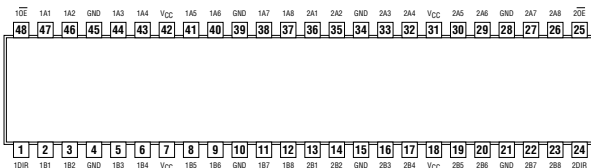
16-BIT BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



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16245

16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

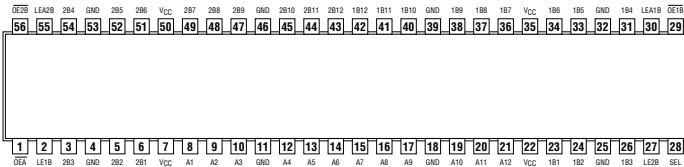


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Pin Assignments

16260

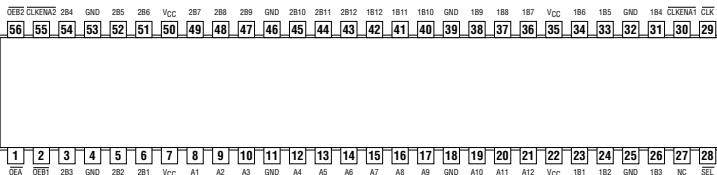
12-BIT TO 24-BIT MULTIPLEXES D-TYPE LATCH
WITH 3-STATE OUTPUTS



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16269

12-BIT TO 24-BIT REGISTERED BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

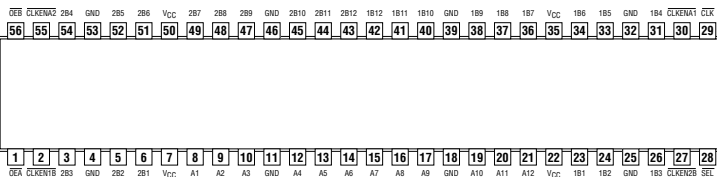


NC – No internal connection

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16270

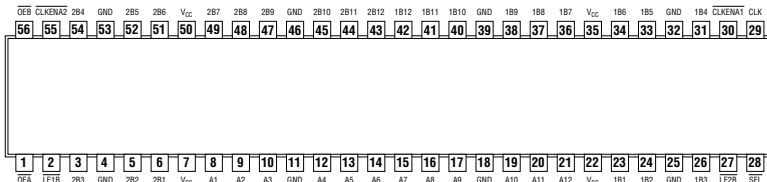
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS



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16271

12-BIT TO 24-BIT MULTIPLEXED BUS EXCHANGER
WITH 3-STATE OUTPUTS

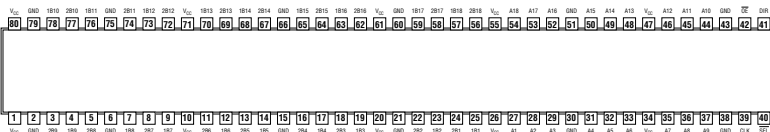


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Pin Assignments

16282

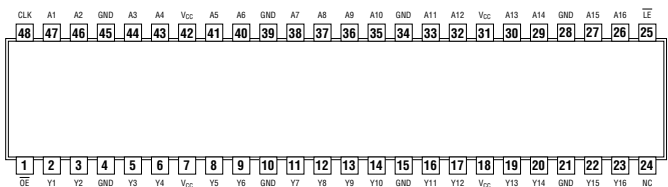
18-BIT TO 36-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS



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16334

16-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS

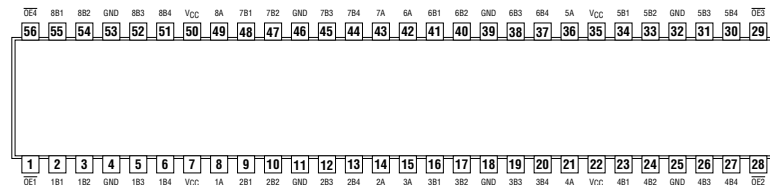


NC – No internal connection

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16344

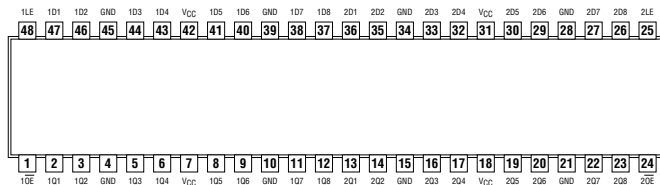
1-BIT TO 4-BIT ADDRESS DRIVER
WITH 3-STATE OUTPUTS



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16373

16-BIT TRANSPARENT LATCHES
WITH 3-STATE OUTPUTS

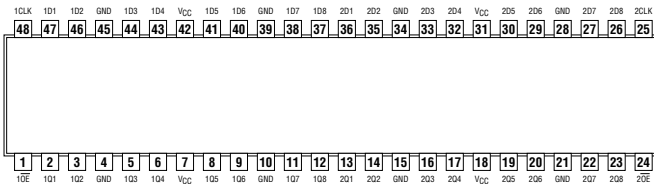


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Pin Assignments

16374

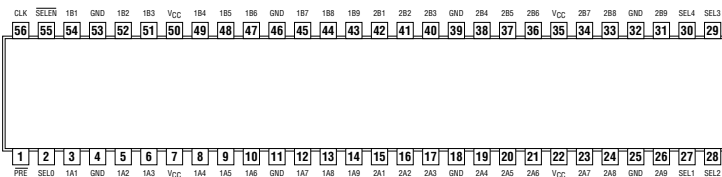
16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS



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16409

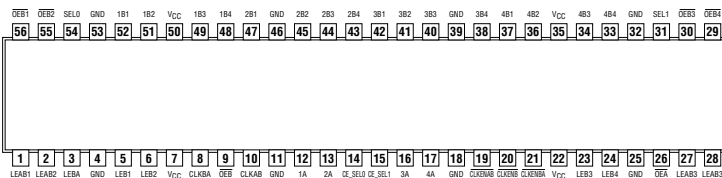
9-BIT, 4-PORT UNIVERSAL BUS EXCHANGER
WITH 3-STATE OUTPUTS



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16460

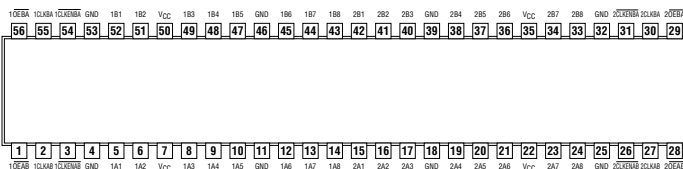
4-TO-1 MULTIPLEXED/DEMULPLEXED TRANSCEIVERS
WITH 3-STATE OUTPUTS



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16470

16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

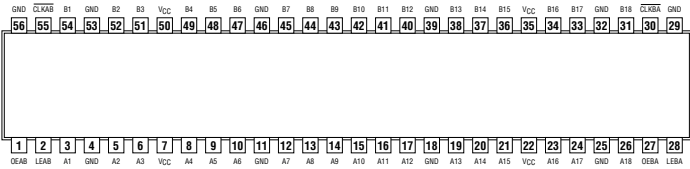


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Pin Assignments

16500

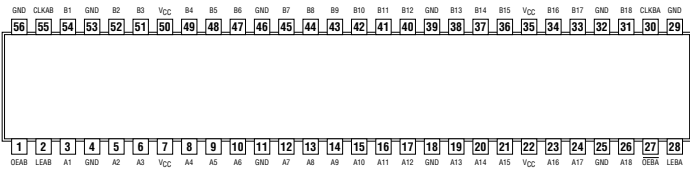
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS



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16501

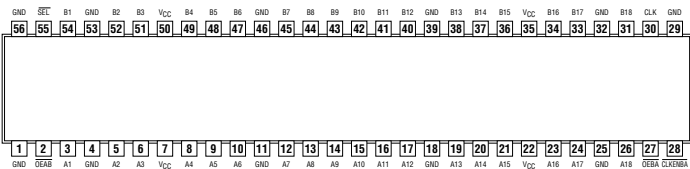
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS



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16524

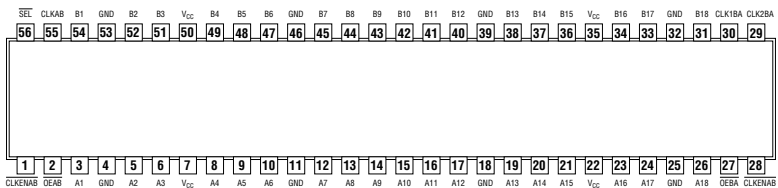
18-BIT REGISTERED BUS TRANSCEIVER
WITH 3-STATE OUTPUTS



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16525

18-BIT REGISTERED BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

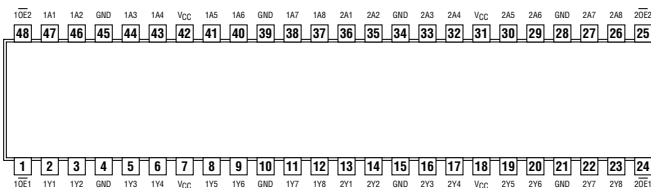


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Pin Assignments

16540

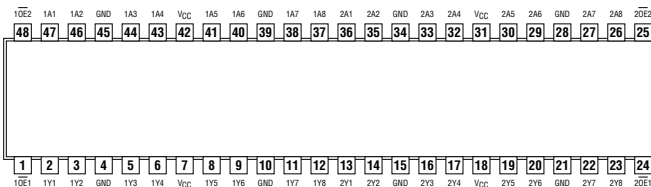
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



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16541

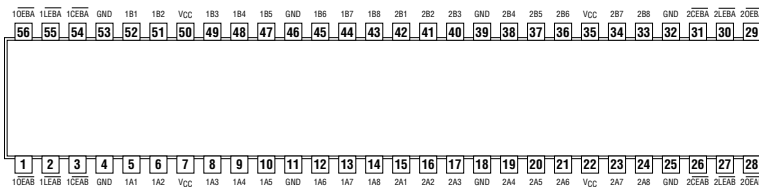
16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



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16543

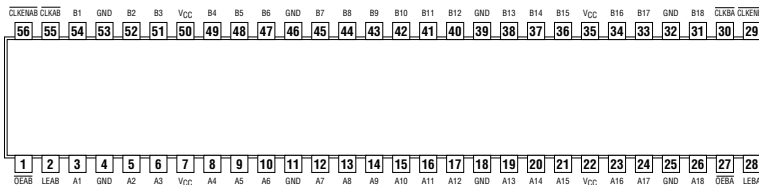
16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS



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16600

18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

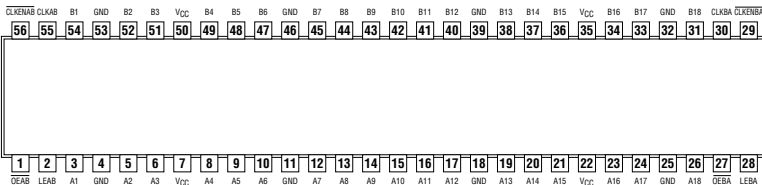


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Pin Assignments

16601

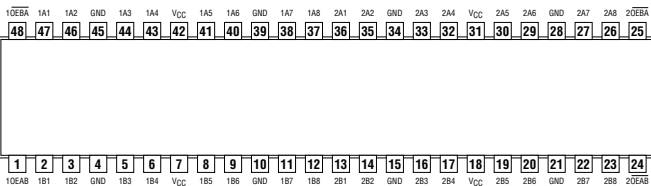
18-BIT UNIVERSAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS



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16620

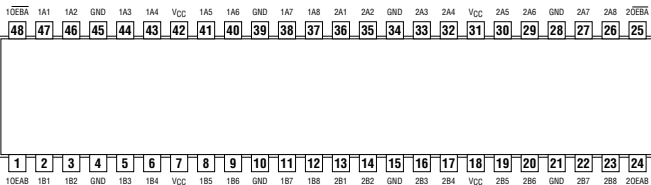
16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS



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16623

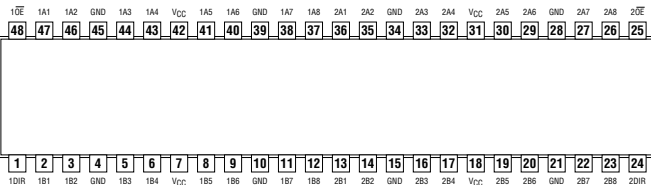
16-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS



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16640

16-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

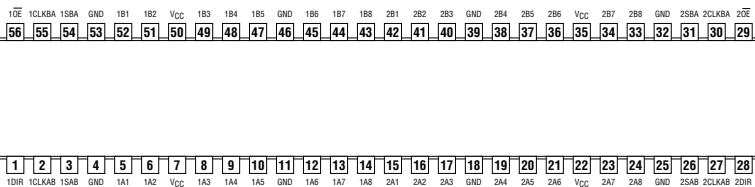


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Pin Assignments

16646

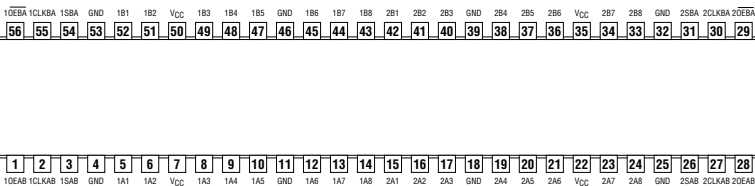
16-BIT BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS



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16651

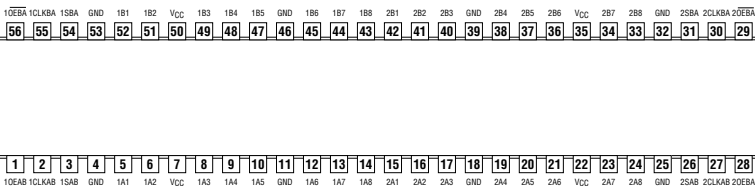
16-BIT BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS



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16652

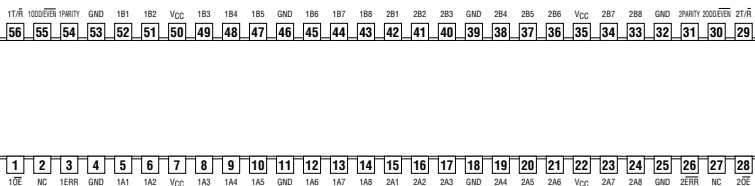
16-BIT BUS TRANSCEIVERS AND REGISTERS
WITH 3-STATE OUTPUTS



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16657

16-BIT TRANSCEIVERS
WITH PARITY GENERATORS/CHECKERS AND 3-STATE OUTPUTS



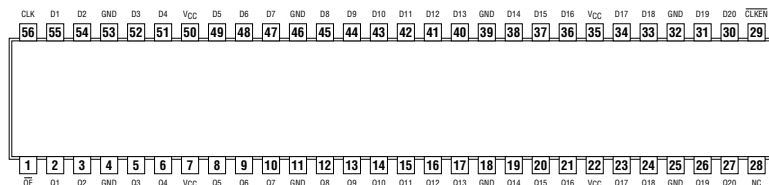
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NC – No internal connection

Pin Assignments

16721

20-BIT FLIP-FLOP
WITH 3-STATE OUTPUTS

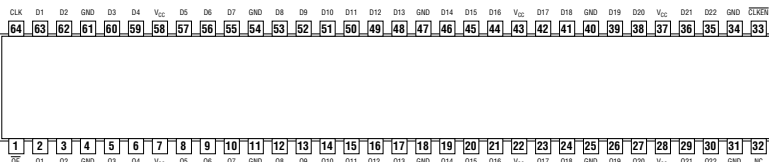


NC – No internal connection

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16722

22-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

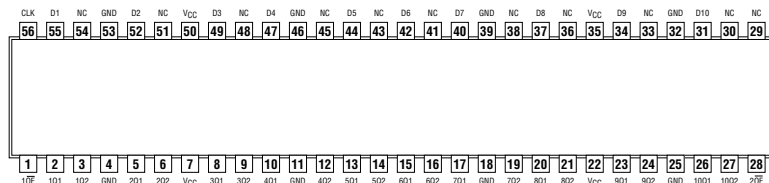


NC – No internal connection

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16820

10-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH DUAL OUTPUTS

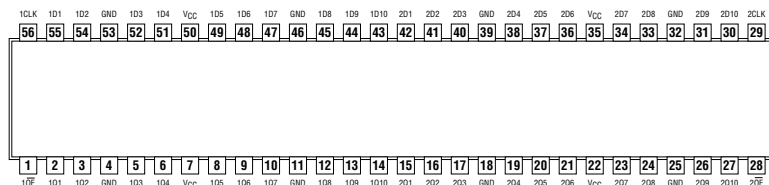


NC – No internal connection

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16821

20-BIT BUS INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS

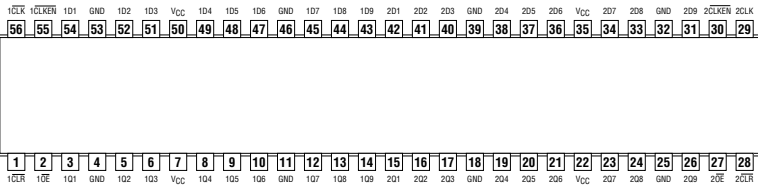


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Pin Assignments

16823

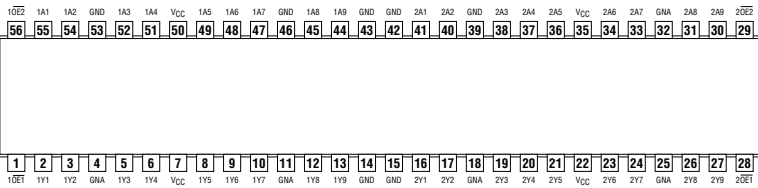
18-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH DUAL OUTPUTS



See page 604

16825

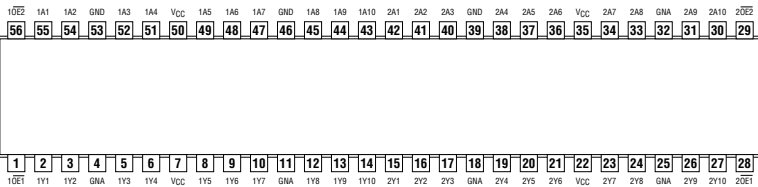
18-BIT BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



See page 605

16827

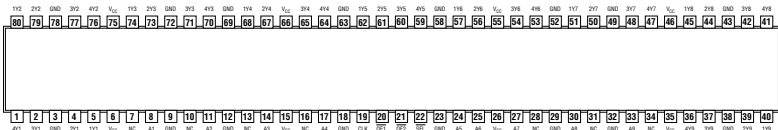
20-BIT BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



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16831

1-TO-4 ADDRESS REGISTER/DRIVER
WITH 3-STATE OUTPUTS



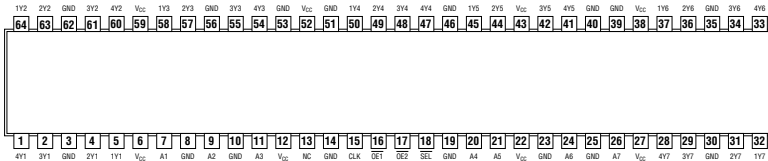
NC – No internal connection

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Pin Assignments

16832

1-TO-4 ADDRESS REGISTER/DRIVER
WITH 3-STATE OUTPUTS

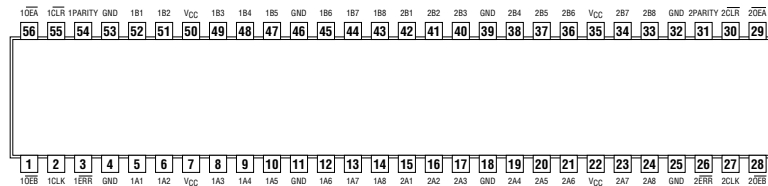


NC – No internal connection

See page 608

16833

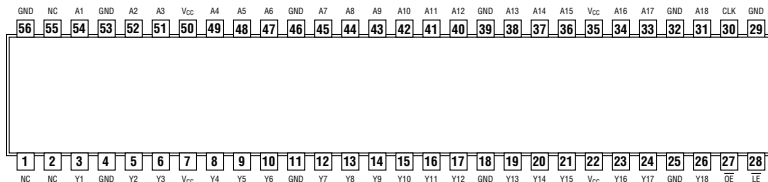
DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS



See page 610

16834

16-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS

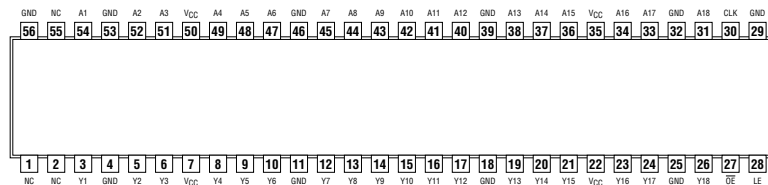


NC – No internal connection

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16835

3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS



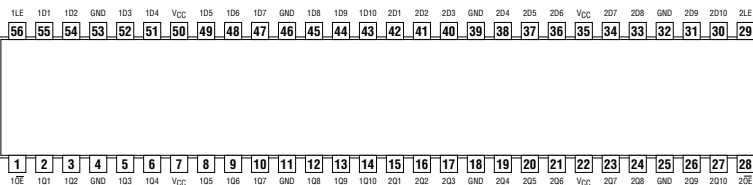
NC – No internal connection

See page 613

Pin Assignments

16841

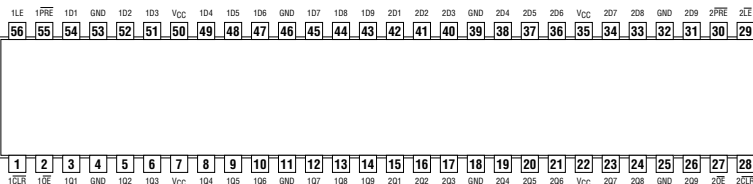
20-BIT BUS INTERFACE D-TYPE LATCHES
WITH 3-STATE OUTPUTS



See page 614

16843

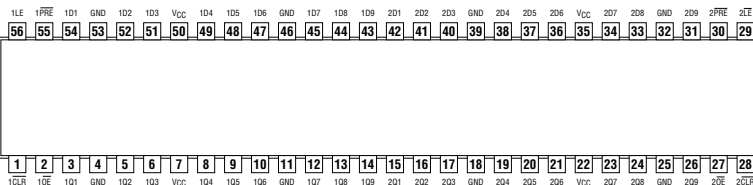
18-BIT BUS INTERFACE D-TYPE LATCHES
WITH 3-STATE OUTPUTS



See page 615

16853

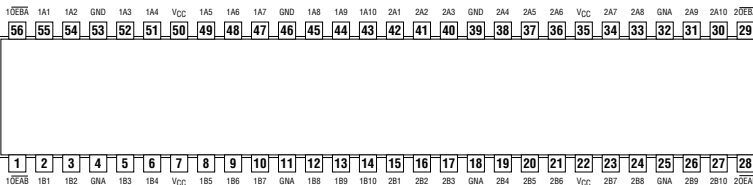
DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS



See page 616

16861

20-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

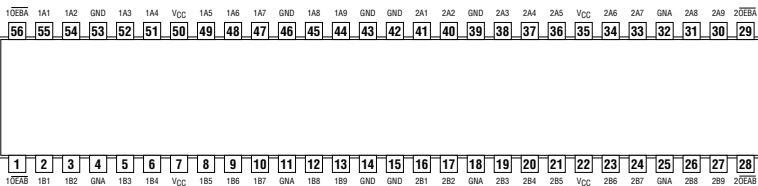


See page 618

Pin Assignments

16863

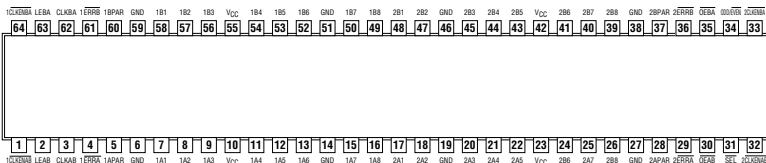
18-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS



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16901

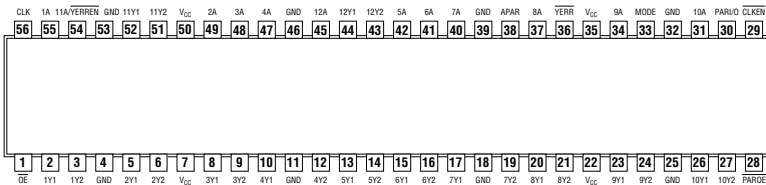
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH PARITY GENERATORS/CHECKERS



See page 620

16903

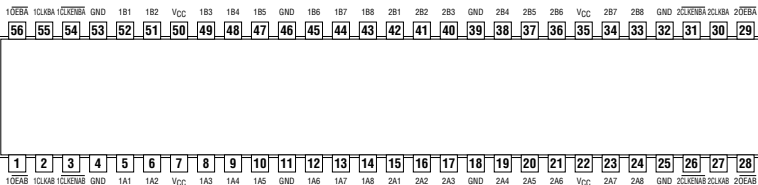
3.3-V 12-BIT UNIVERSAL BUS DRIVER
WITH PARITY CHECKER AND DUAL 3-STATE OUTPUTS



See page 622

16952

16-BIT REGISTERED TRANSCEIVERS
WITH 3-STATE OUTPUTS

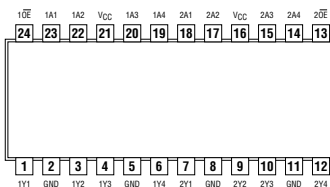


See page 624

Pin Assignments

25244

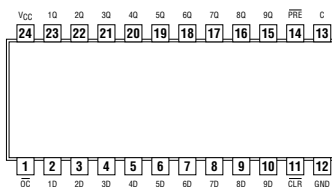
25-Ω OCTAL BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



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29825

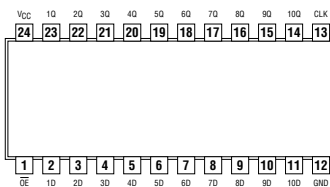
8-BIT BUS-INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS



See page 630

25245

25-Ω OCTAL BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

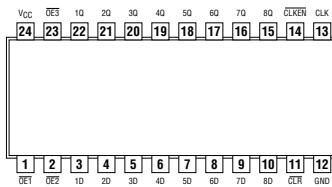


See page 627

29827

29828

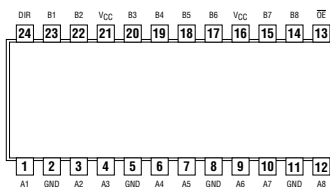
10-BIT BUFFERS AND BUS DRIVERS
WITH 3-STATE OUTPUTS



See page 631, 632

25642

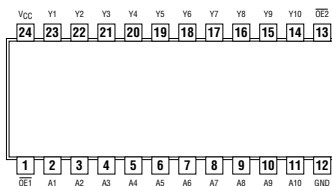
25-Ω OCTAL BUS TRANSCEIVER



See page 628

29841

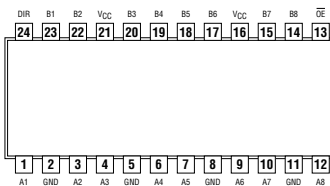
10-BIT BUS INTERFACE D-TYPE LATCHES
WITH 3-STATE OUTPUTS



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29821

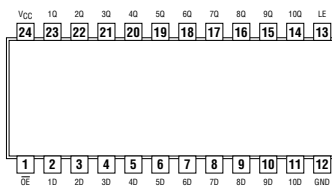
10-BIT BUS-INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS



See page 629

29843

9-BIT BUS INTERFACE D-TYPE LATCHES
WITH 3-STATE OUTPUTS

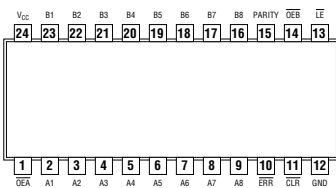


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Pin Assignments

29854

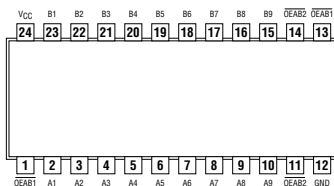
8-BIT TO 9-BIT PARITY BUS TRANSCEIVER



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29864

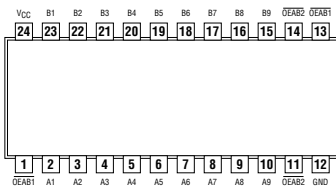
9-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS



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29863

9-BIT BUS TRANSCEIVERS
WITH 3-STATE OUTPUTS

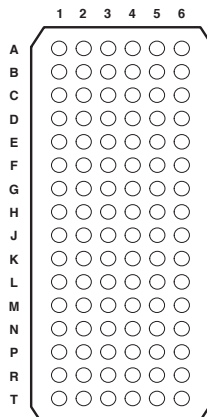


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32240

32-BIT BUFFER/DRIVER

GKE PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1Y2	1Y1	1 \overline{OE}	2 \overline{OE}	1A1	1A2
B	1Y4	1Y3	GND	GND	1A3	1A4
C	2Y2	2Y1	1V _{CC}	1V _{CC}	2A1	2A2
D	2Y2	2Y3	GND	GND	2A3	2A4
E	3Y2	3Y1	GND	GND	3A1	3A2
F	3Y4	3Y3	1V _{CC}	1V _{CC}	3A3	3A4
G	4Y2	4Y1	GND	GND	4A1	4A2
H	4Y3	4Y4	4 \overline{OE}	3 \overline{OE}	4A4	4A3
J	5Y2	5Y1	5 \overline{OE}	6 \overline{OE}	5A1	5A2
K	5Y4	5Y3	GND	GND	5A3	5A4
L	6Y2	6Y1	2V _{CC}	2V _{CC}	6A1	6A2
M	6Y4	6Y3	GND	GND	6A3	6A4
N	7Y2	7Y1	GND	GND	7A1	7A2
P	7Y4	7Y3	2V _{CC}	2V _{CC}	7A3	7A4
R	8Y2	8Y1	GND	GND	8A1	8A2
T	8Y3	8Y4	8 \overline{OE}	7 \overline{OE}	8A4	8A3

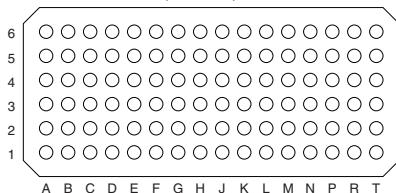
See page 640

Pin Assignments

32244

36-BIT BUFFER/DRIVER
WITH 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)



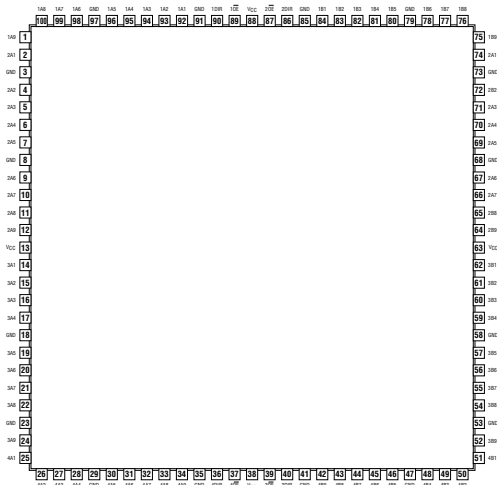
6	1A2	1A4	2A2	2A4	3A2	3A4	4A2	4A3	5A2	5A4	6A2	6A4	7A2	7A4	8A2	8A3
5	1A1	1A3	2A1	2A3	3A1	3A3	4A1	4A4	5A1	5A3	6A1	6A3	7A1	7A3	8A1	8A4
4	2OE	GND	V _{CC}	GND	GND	V _{CC}	GND	3OE	6OE	GND	V _{CC}	GND	GND	V _{CC}	GND	7OE
3	1OE	GND	V _{CC}	GND	GND	V _{CC}	GND	4OE	5DIR	GND	V _{CC}	GND	GND	V _{CC}	GND	8DIR
2	1Y1	1Y3	2Y1	2Y3	3Y1	3Y3	4Y1	4Y4	5Y1	5Y3	6Y1	6Y3	7Y1	7Y3	8Y1	8Y4
1	1Y2	1Y4	2Y2	2Y4	3Y2	3Y4	4Y2	4Y3	5Y2	5Y4	6Y2	6Y4	7Y2	7Y4	8Y2	8Y3
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

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Pin Assignments

32245

36-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

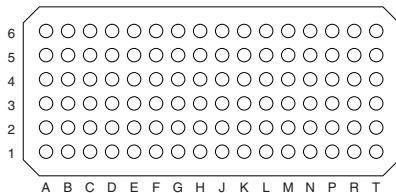


See page 644

32245

36-BIT BUS TRANSCEIVER
WITH 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)



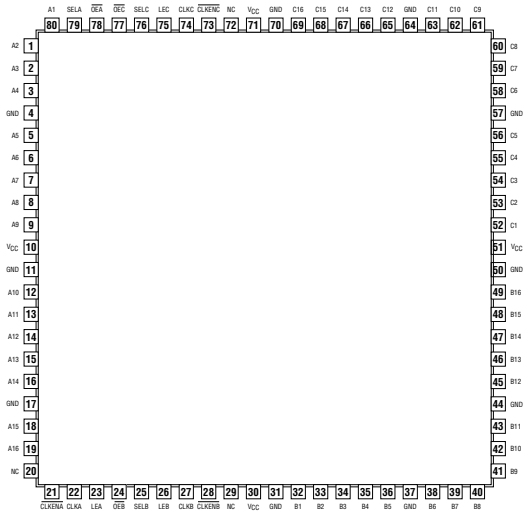
6	1A2	1A4	1A6	1A8	2A2	2A4	2A6	2A7	3A2	3A4	3A6	3A8	4A2	4A4	4A6	4A7
5	1A1	1A3	1A5	1A7	2A1	2A3	2A5	2A8	3A1	3A3	3A5	3A7	4A1	4A3	4A5	4A8
4	1OE	GND	V _{CC}	GND	GND	V _{CC}	GND	2OE	3OE	GND	V _{CC}	GND	GND	V _{CC}	GND	4OE
3	1DIR	GND	V _{CC}	GND	GND	V _{CC}	GND	2DIR	3DIR	GND	V _{CC}	GND	GND	V _{CC}	GND	4DIR
2	1B1	1B3	1B5	1B7	2B1	2B3	2B5	2B8	3B1	3B3	3B5	3B7	4B1	4B3	4B5	4B8
1	1B2	1B4	1B6	1B8	2B2	2B4	2B6	2B7	3B2	3B4	3B6	3B8	4B2	4B4	4B6	4B7
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

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Pin Assignments

32316

16-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS

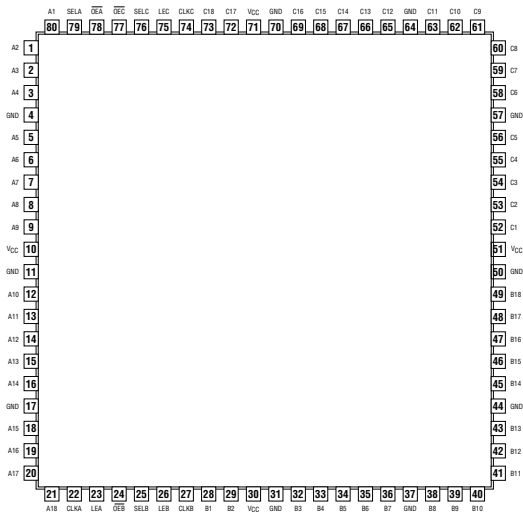


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NC – No internal connection

32318

18-BIT TRI-PORT UNIVERSAL BUS EXCHANGERS



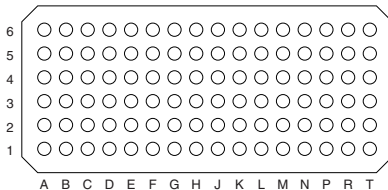
See page 648

Pin Assignments

32373

32-BIT TRANSPARENT D-TYPE LATCH
WITH 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)



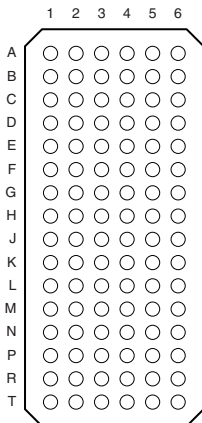
6	1D2	1D4	1D6	1D8	2D2	2D4	2D6	2D7	3D2	3D4	3D6	3D8	4D2	4D4	4D6	4D7
5	1D1	1D3	1D5	1D7	2D1	2D3	2D5	2D8	3D1	3D3	3D5	3D7	4D1	4D3	4D5	4D8
4	1LE	GND	V _{CC}	GND	GND	V _{CC}	GND	2LE	3LE	GND	V _{CC}	GND	GND	V _{CC}	GND	4LE
3	1OE	GND	V _{CC}	GND	GND	V _{CC}	GND	2OE	3OE	GND	V _{CC}	GND	GND	V _{CC}	GND	4OE
2	1Q1	1Q3	1Q5	1Q7	2Q1	2Q3	2Q5	2Q8	3Q1	3Q3	3Q5	3Q7	4Q1	4Q3	4Q5	4Q8
1	1Q2	1Q4	1Q6	1Q8	2Q2	2Q4	2Q6	2Q7	3Q2	3Q4	3Q6	3Q8	4Q2	4Q4	4Q6	4Q7
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T

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32374

32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)



terminal assignments

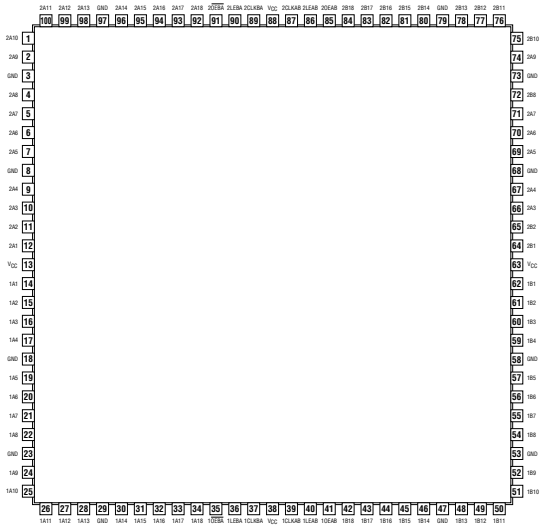
	1	2	3	4	5	6
A	1Q2	1Q1	1OE	1CLK	1D1	1D2
B	1Q4	1Q3	GND	GND	1D3	1D4
C	1Q6	1Q5	V _{CC}	V _{CC}	1D5	1D6
D	1Q8	1Q7	GND	GND	1D7	1D8
E	2Q2	2Q1	GND	GND	2D1	2D2
F	2Q4	2Q3	V _{CC}	V _{CC}	2D3	2D4
G	2Q6	2Q5	GND	GND	2D5	2D6
H	2Q8	2Q7	2OE	2CLK	2D7	2D8
J	3Q2	3Q1	3OE	3CLK	3D1	3D2
K	3Q4	3Q3	GND	GND	3D3	3D4
L	3Q6	3Q5	V _{CC}	V _{CC}	3D5	3D6
M	3Q8	3Q7	GND	GND	3D7	3D8
N	4Q2	4Q1	GND	GND	4D1	4D2
P	4Q4	4Q3	V _{CC}	V _{CC}	4D3	4D4
R	4Q6	4Q5	GND	GND	4D5	4D6
T	4Q7	4Q8	4OE	4CLK	4D8	4D7

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Pin Assignments

32501

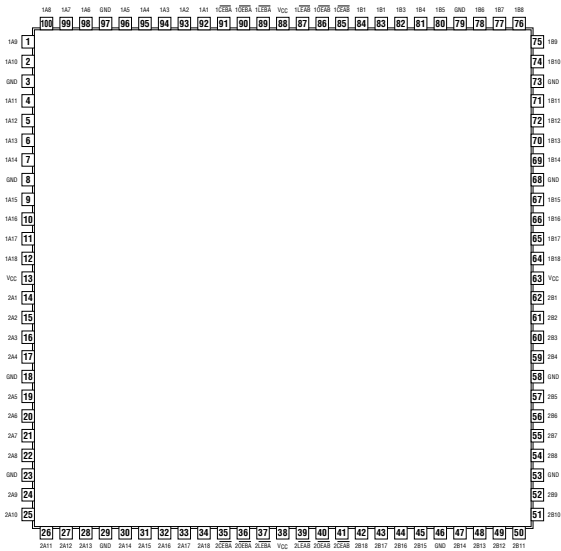
36-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS



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32543

36-BIT REGISTERED BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

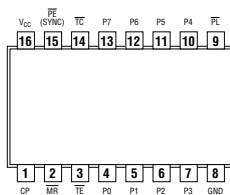


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Pin Assignments

40103

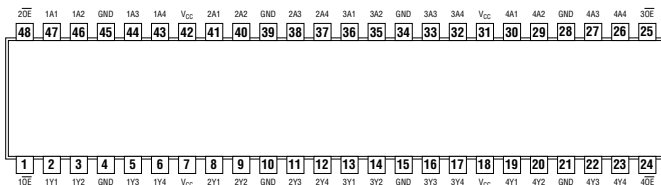
8-STAGE SYNCHRONOUS DOWN COUNTERS



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162240

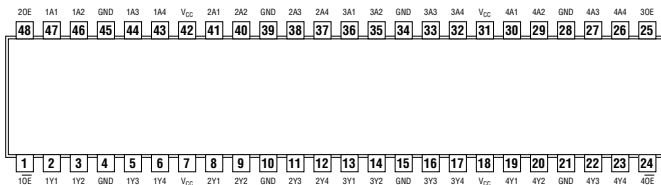
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



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162241

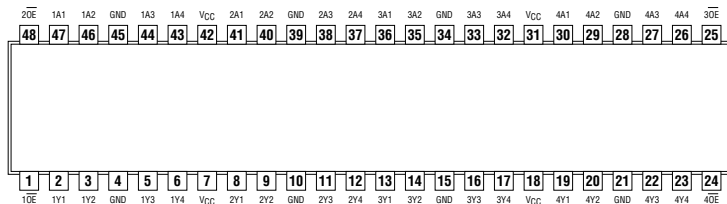
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



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162244

16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

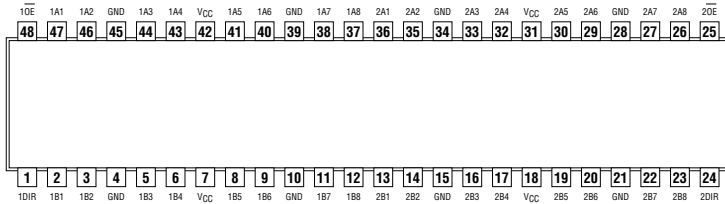


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Pin Assignments

162245

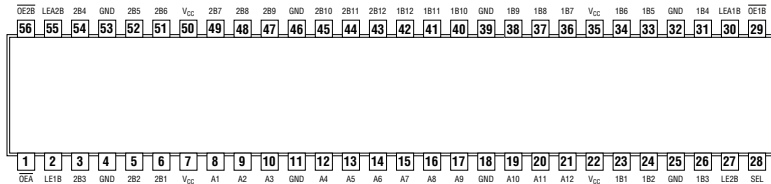
16-BIT TRANSCEIVER
WITH 3-STATE OUTPUTS



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162260

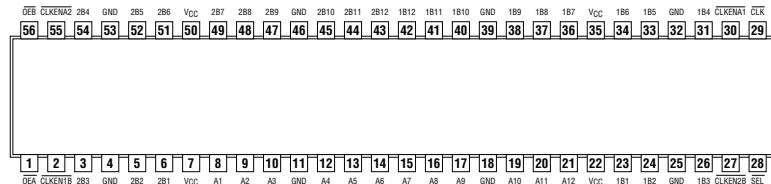
12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH
WITH 3-STATE OUTPUTS



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162268

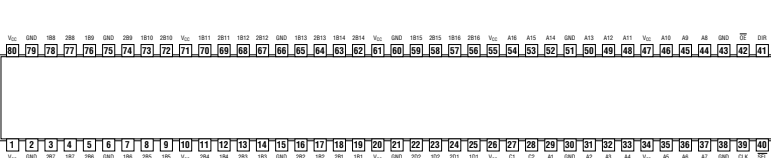
12-BIT TO 24-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS



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162280

16-BIT TO 32-BIT REGISTERED BUS EXCHANGER
WITH BYTE MASKS AND 3-STATE OUTPUTS

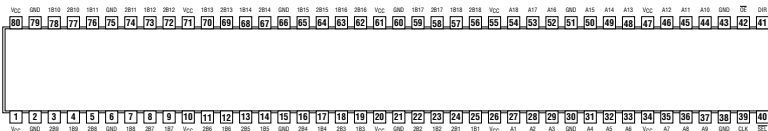


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Pin Assignments

162282

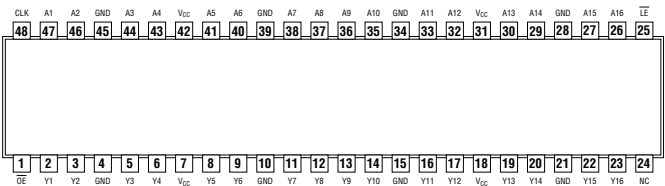
18-BIT TO 36-BIT REGISTERED BUS EXCHANGER
WITH 3-STATE OUTPUTS



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162334

16-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS

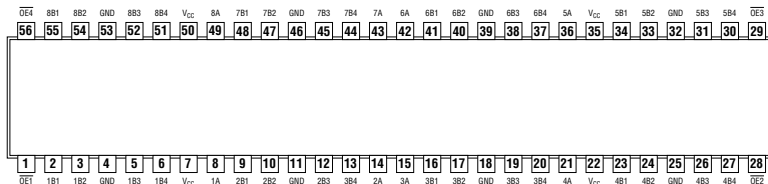


NC – No internal connection

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162344

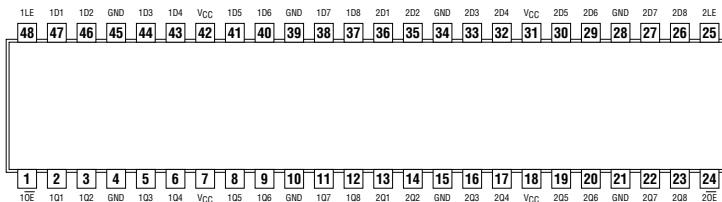
1-BIT TO 4-BIT ADDRESS DRIVER
WITH 3-STATE OUTPUTS



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162373

3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES
WITH 3-STATE OUTPUTS

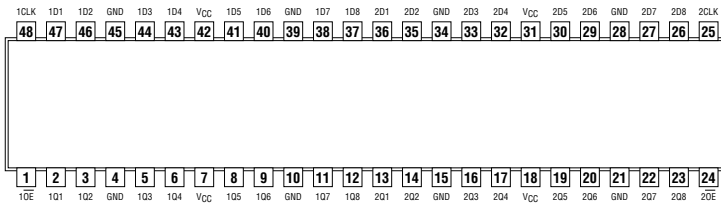


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Pin Assignments

162374

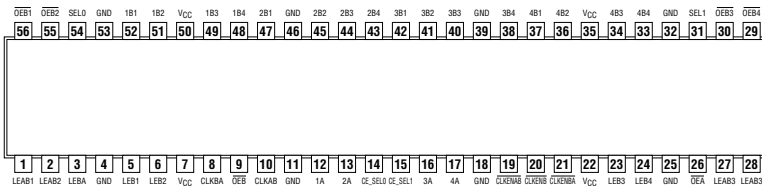
3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS



See page 677

162460

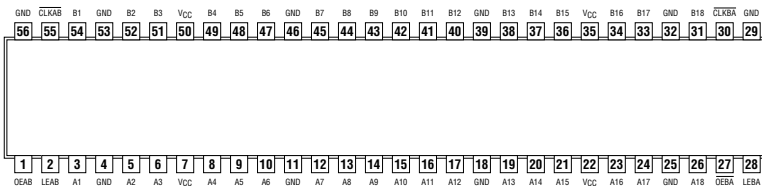
4-TO-1 MULTIPLEXED/DEMULTIPLEXED REGISTERED TRANSCIEVERS
WITH 3-STATE OUTPUTS



See page 678

162500

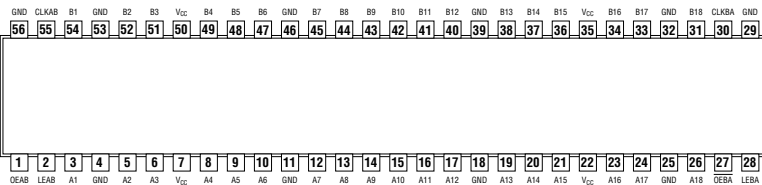
18-BIT UNIVERSAL BUS TRANSCIEVER
WITH 3-STATE OUTPUTS



See page 680

162501

18-BIT UNIVERSAL BUS TRANSCIEVERS
WITH 3-STATE OUTPUTS

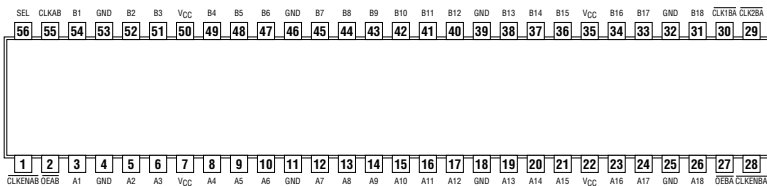


See page 682

Pin Assignments

162525

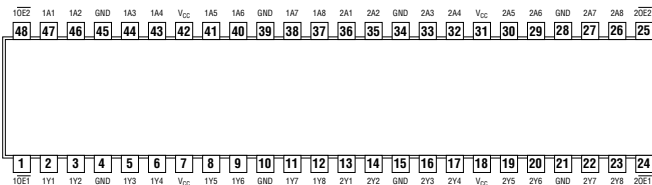
16-BIT REGISTERED BUS TRANSCEIVER
WITH 3-STATE OUTPUTS



See page 684

162541

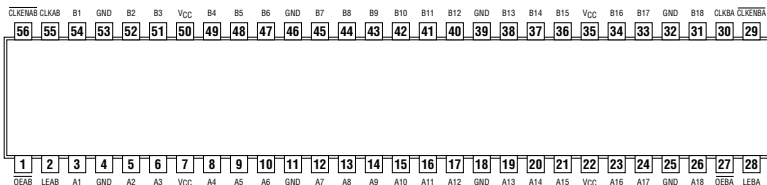
3.3-V ABT 16-BIT BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS



See page 686

162601

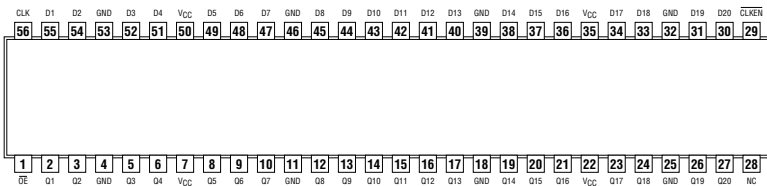
18-BIT UNIVERSAL BUS TRANSCEIVER
WITH 3-STATE OUTPUTS



See page 688

162721

3.3-V 20-BIT FLIP-FLOP
WITH 3-STATE OUTPUTS



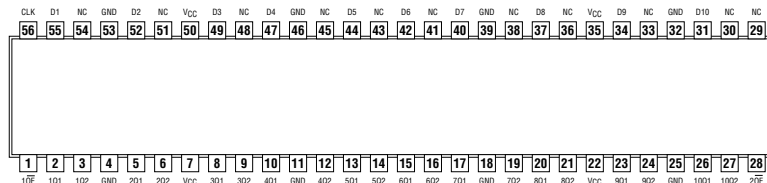
See page 690

NC – No internal connection

Pin Assignments

162820

3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS
AND 3-STATE OUTPUTS

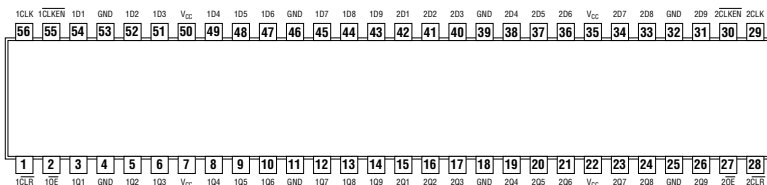


NC – No internal connection

See page 691

162823

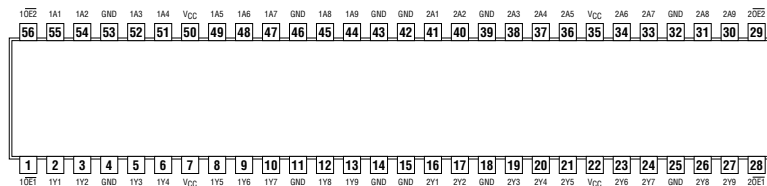
18-BIT BUS-INTERFACE FLIP-FLOPS
WITH 3-STATE OUTPUTS



See page 692

162825

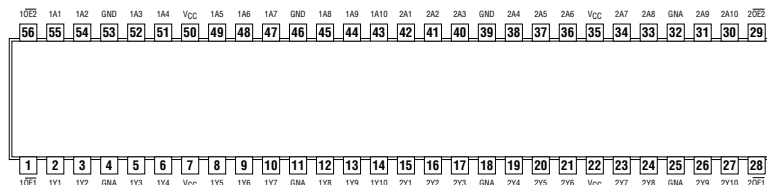
18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS



See page 693

162827

20-BIT BUS BUFFERS/DRIVERS
WITH 3-STATE OUTPUTS

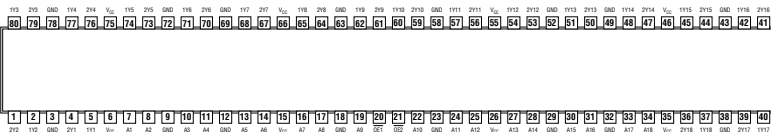


See page 694

Pin Assignments

162830

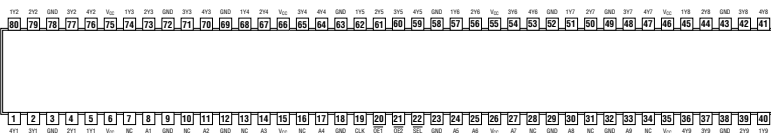
1-BIT TO 2-BIT ADDRESS DRIVER
WITH 3-STATE OUTPUTS



See page 695

162831

1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER
WITH 3-STATE OUTPUTS

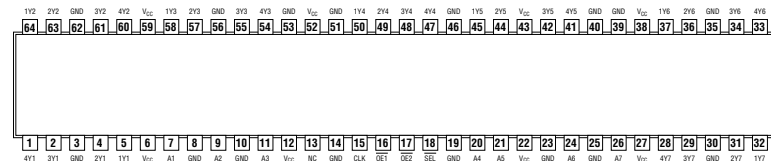


NC – No internal connection

See page 696

162832

1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER
WITH 3-STATE OUTPUTS

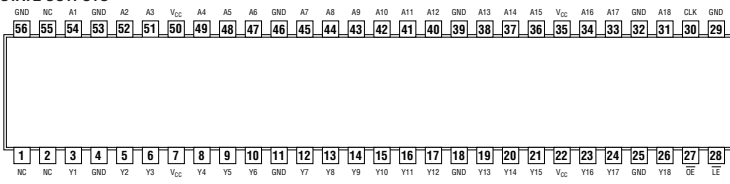


See page 697

162834

162835

18-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS



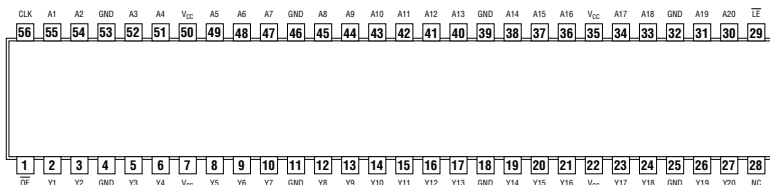
See page 698, 699

NC – No internal connection

Pin Assignments

162836

20-BIT UNIVERSAL BUS DRIVER
WITH 3-STATE OUTPUTS

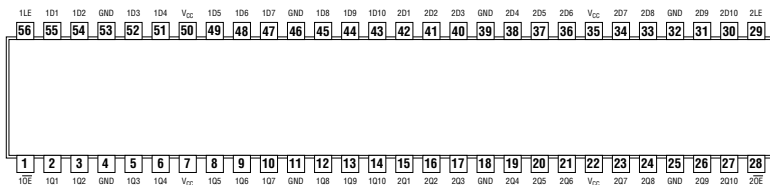


NC – No internal connection

See page 700

162841

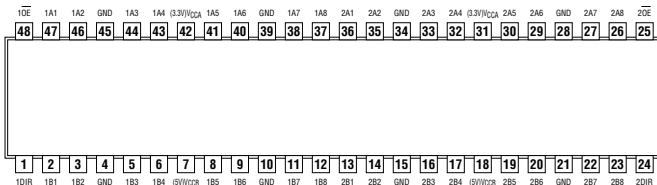
20-BIT BUS-INTERFACE D-TYPE LATCH
WITH 3-STATE OUTPUTS



See page 701

164245

16-BIT TRANSCEIVER AND 3.3-V TO 5-V SHIFTER
WITH 3-STATE OUTPUTS



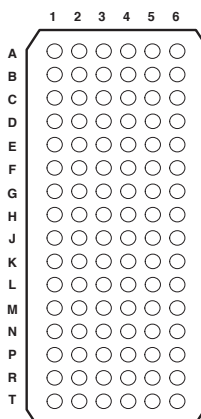
See page 702

Pin Assignments

322374

3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP
WITH 3-STATE OUTPUTS

GKE PACKAGE
(TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1Q2	1Q1	1 \overline{OE}	1CLK	1D1	1D2
B	1Q4	1Q3	GND	GND	1D3	1D4
C	1Q6	1Q5	V _{CC}	V _{CC}	1D5	1D6
D	1Q8	1Q7	GND	GND	1D7	1D8
E	2Q2	2Q1	GND	GND	2D1	2D2
F	2Q4	2Q3	V _{CC}	V _{CC}	2D3	2D4
G	2Q6	2Q6	GND	GND	2D5	2D6
H	2Q7	2Q8	2 \overline{OE}	2CLK	2D8	2D7
J	3Q2	3Q1	3 \overline{OE}	3CLK	3D1	3D2
K	3Q4	3Q3	GND	GND	3D3	3D4
L	3Q6	3Q5	V _{CC}	V _{CC}	3D5	3D6
M	3Q8	3Q7	GND	GND	3D7	3D8
N	4Q2	4Q1	GND	GND	4D1	4D2
P	4Q4	4Q3	V _{CC}	V _{CC}	4D3	4D4
R	4Q6	4Q5	GND	GND	4D5	4D6
T	4Q7	4Q8	4 \overline{OE}	4CLK	4D8	4D7

NC – No internal connection

See page 703

**FUNCTION
AND
ELECTRICAL
CHARACTERISTICS**

QUADRUPLE 2-INPUT POSITIVE-NAND GATES



- $Y = \overline{A \cdot B}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
I _{CC}	MAX	22	4.4	36	3	17.4	10.2	0.02	0.04	0.02	0.04	0.04	0.02	0.08	0.04	mA
I _{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
I _{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	UNIT
I _{CC}	MAX	0.02	0.08	0.02	0.02	-	0.02	0.01	0.01	mA
I _{OH}	MAX	-24	-24	-8	-8	-6	-12	-24	-24	mA
I _{OL}	MAX	24	24	8	8	6	12	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11
t _{PLH}	A or B	Y	MAX	22	15	4.5	11	4.5	6	23	27	25	30	7.4	8.5	7.3	12.3
t _{PHL}	A or B	Y	MAX	15	15	5	8	4	5.3	23	27	25	30	6.8	7	7.3	8.8

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V
t _{PLH}	A or B	Y	MAX	9.5	10.8	8.5	9	13	8.5	4.3	3
t _{PHL}	A or B	Y	MAX	8	13.2	8.5	9	13	8.5	4.3	3

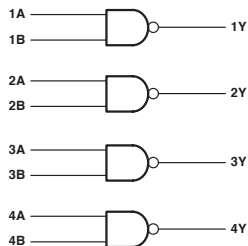
UNIT:ns

01

QUADRUPLE 2-INPUT POSITIVE-NAND GATES WITH OPEN-COLLECTOR OUTPUTS

● $Y = \overline{A \cdot B}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	HC	UNIT
I_{CC}	MAX	22	4.4	3	0.02	mA
V_{OH}	MAX	5.5	5.5	5.5	V_{CC}	V
I_{OL}	MAX	16	8	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	HC
t_{PLH}	A or B	Y	MAX	55	32	54	31
t_{PHL}	A or B	Y	MAX	15	28	28	25

UNIT:ns

QUADRUPLE 2-INPUT POSITIVE-NOR GATES



- $Y = \overline{A + B}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	CD74 AC	ACT 11	UNIT
I _{CC}	MAX	27	5.4	45	4	20.1	13	0.02	0.04	0.02	0.04	0.04	0.08	0.04	mA
I _{DH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	mA
I _{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	mA

PARAMETER	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I _{CC}	MAX	0.08	0.02	0.02	-	0.02	0.01	mA
I _{DH}	MAX	-24	-8	-8	-6	-12	-24	mA
I _{OL}	MAX	24	8	8	6	12	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	CD74 AC	ACT 11
t _{PLH}	A or B	Y	MAX	22	15	5.5	12	4.5	6.5	23	27	25	32	6.9	11.5	10.6
t _{PHL}	A or B	Y	MAX	15	15	5.5	10	4.5	5.3	23	27	25	32	6.4	11.5	8.7

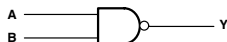
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t _{PLH}	A or B	Y	MAX	12.2	8.5	8.5	13	8.5	4.4
t _{PHL}	A or B	Y	MAX	12.2	8.5	8.5	13	8.5	4.4

UNIT: ns

03

**QUADRUPLE 2-INPUT
POSITIVE-NAND GATES
WITH OPEN-COLLECTOR
OUTPUTS**

Logic Diagram



● $Y = \overline{A \cdot B}$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	22	4.4	36	4	0.02	0.04	0.04	mA
V_{OH}	MAX	5.5	8	5.5	8	0.05	V_{CC}	V_{CC}	V
I_{OL}	MAX	16	0.1	20	0.1	4	4	4	mA

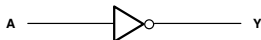
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A or B	Y	MAX	45	32	7.5	50	31	30	36
t_{PHL}	A or B	Y	MAX	15	28	7	13	25	30	36

UNIT: ns

HEX INVERTERS

Logic Diagram



- $Y = \bar{A}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
I_{CC}	MAX	33	6.6	54	4.2	26.3	15.3	0.02	0.04	0.02	0.04	0.04	0.02	0.08	0.04	mA
I_{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V	UNIT
I_{CC}	MAX	0.02	0.08	0.02	0.02	-	0.02	0.01	0.01	mA
I_{OH}	MAX	-24	-24	-8	-8	-6	-12	-24	-24	mA
I_{OL}	MAX	24	24	8	8	6	12	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11
t_{PLH}	A or B	Y	MAX	22	15	4.5	11	5	6	24	26	25	29	7.1	7.5	6.5	9.7
t_{PHL}	A or B	Y	MAX	15	15	5	8	4	5.3	24	26	25	29	6	7	6.5	9.6

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V
t_{PLH}	A or B	Y	MAX	9	9.3	8.5	8.5	12	8.5	4.5	2.8
t_{PHL}	A or B	Y	MAX	8.5	9.3	8.5	8.5	12	8.5	4.5	2.8

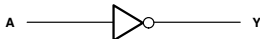
UNIT: ns

U04

HEX INVERTERS

- $Y = \bar{A}$
- Unbuffered Output

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	AHC	LV 3V	LV 5V	LVC 3V	UNIT
I _{cc}	MAX	0.02	0.04	0.02	-	0.02	0.01	mA
I _{oh}	MAX	-4	-4	-8	-6	-12	-24	mA
I _{ol}	MAX	4	4	8	6	12	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	AHC	LV 3V	LV 5V	LVC 3V
t _{PLH}	A or B	Y	MAX	20	21	8	13	8	3.8
t _{PHL}	A or B	Y	MAX	20	21	8	13	8	3.8

UNIT: ns

05

HEX INVERTERS WITH OPEN-COLLECTOR OUTPUTS

- $Y = \bar{A}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 AC	CD74 ACT	AHC	LV 3V	LV 5V	UNIT
I _{cc}	MAX	33	6.6	54	4.2	0.02	0.08	0.08	0.02	-	0.02	mA
I _{oh}	MAX	-	-	-	-	-24	-24	-	-	-	-	mA
V _{oh}	MAX	5.5	5.5	5.5	5.5	5.5	5.5	5.5	V _{cc}	5.5	5.5	V
I _{ol}	MAX	16	8	20	8	4	24	24	8	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	SN74 HC	CD74 AC	CD74 ACT	AHC	LV 3V	LV 5V
t _{PLH}	A or B	Y	MAX	55	32	7.5	54	29	-	-	-	12	8.5
t _{PHL}	A or B	Y	MAX	15	28	7	14	21	-	-	-	12	8.5
t _{PLZ}	A	Y	MAX	-	-	-	-	-	8.2	9.3	8.5	-	-
t _{PZL}	A	Y	MAX	-	-	-	-	-	6.5	10.8	8.5	-	-

UNIT: ns

06

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

$$\bullet Y = \bar{A}$$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	51	60	-	0.02	0.01	mA
I_{OH}	MAX	0.25	0.25	-	0.0025	-	mA
V_{OH}	MAX	30	30	5.5	5.5	5.5	V
I_{OL}	MAX	40	40	8	16	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V
t_{PLH}	A or B	Y	MAX	15	15	12	8.5	3.7
t_{PHL}	A or B	Y	MAX	23	20	12	8.5	3.7

UNIT: ns

07

HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

$$\bullet Y = A$$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

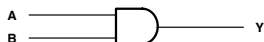
PARAMETER	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	41	45	-	0.02	0.01	mA
I_{OH}	MAX	0.25	0.25	-	0.0025	-	mA
V_{OH}	MAX	30	30	5.5	5.5	5.5	V
I_{OL}	MAX	40	40	8	16	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	LV 3V	LV 5V	LVC 3V
t_{PLH}	A or B	Y	MAX	15	10	12	8.5	2.9
t_{PHL}	A or B	Y	MAX	26	30	12	8.5	2.9

UNIT: ns

QUADRUPLE 2-INPUT POSITIVE-AND GATES



- $Y = A \cdot B$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
I _{CC}	MAX	33	8.8	57	4	24	12.9	0.02	0.04	0.02	0.04	0.04	0.02	0.08	0.04	mA
I _{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
I _{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC	ALVC	UNIT
I _{CC}	MAX	0.02	0.08	0.02	0.02	-	0.02	0.01	0.01	mA
I _{OH}	MAX	-24	-24	-8	-8	-6	-12	-24	-24	mA
I _{OL}	MAX	24	24	8	8	6	12	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11
t _{PLH}	A or B	Y	MAX	27	15	7	14	5.5	6.6	25	27	30	38	6.9	8.5	8.7	9
t _{PHL}	A or B	Y	MAX	19	20	7.5	10	5.5	6.3	25	27	30	38	6.5	7.5	8.7	8.2

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC	ALVC
t _{PLH}	A or B	Y	MAX	10	12.9	9	9	14	9	4.1	2.9
t _{PHL}	A or B	Y	MAX	10	12.9	9	9	14	9	4.1	2.9

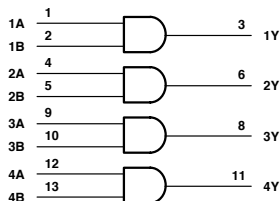
UNIT: ns

09

**QUADRUPLE 2-INPUT
POSITIVE-AND GATES
WITH OPEN-COLLECTOR
OUTPUTS**

$$\bullet Y = A \cdot B$$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC	UNIT
I_{CC}	MAX	33	8.8	57	4.2	26.3	15.3	mA
I_{OH}	MAX	-	0.1	0.25	0.1	-	-	mA
V_{OH}	MAX	5.5	5.5	5.5	5.5	V_{CC}		mA
I_{OL}	MAX	16	8	20	8	20	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC
t_{PLH}	A or B	Y	MAX	32	35	10	54	9.6	31
t_{PHL}	A or B	Y	MAX	24	35	10	15	4.8	25

UNIT: ns

TRIPLE 3-INPUT POSITIVE-NAND GATES



$$Y = \overline{A \cdot B \cdot C}$$

- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
I _{CC}	MAX	16.5	3.3	27	2.2	13	7.7	0.02	0.04	0.02	0.04	0.04	0.02	0.08	0.04	mA
I _{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
I _{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	LV 3V	LV 5V	LVC 3V	ALVC	UNIT
I _{CC}	MAX	0.04	0.08	-	0.02	0.01	0.01	mA
I _{OH}	MAX	-24	-24	-6	-12	-24	-24	mA
I _{OL}	MAX	24	24	6	12	24	24	mA

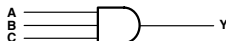
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11
t _{PLH}	A, B or C	Y	MAX	22	15	4.5	11	4.5	6	24	30	19	36	6.7	8	12.2	8.9
t _{PHL}	A, B or C	Y	MAX	15	15	5	10	4.5	5.3	24	30	19	36	7	6.5	12.2	8.2

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT	LV 3V	LV 5V	LVC 3V	ALVC
t _{PLH}	A, B or C	Y	MAX	10	-	13.5	9	4.9	3
t _{PHL}	A, B or C	Y	MAX	9.5	13.5	13.5	9	4.9	3

UNIT: ns

TRIPLE 3-INPUT POSITIVE-AND GATES



- $Y = A \cdot B \cdot C$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	ACT 11	SN74 ACT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	6.6	42	3	18	9.7	0.02	0.04	0.02	0.04	0.04	0.02	0.04	0.02	-	0.02	mA
I_{OH}	MAX	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	-6	-12	mA
I_{OL}	MAX	8	20	8	20	20	4	4	4	4	24	24	24	24	6	12	mA

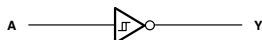
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	ACT 11	SN74 ACT
t_{PLH}	A, B or C	Y	MAX	15	7	13	6	6.6	25	30	21	42	6.5	8.5	9.6	10.5
t_{PHL}	A, B or C	Y	MAX	20	7.5	10	5.5	6.5	25	30	21	42	6.9	7.5	8.7	10.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V
t_{PLH}	A, B or C	Y	MAX	14	9
t_{PHL}	A, B or C	Y	MAX	14	9

UNIT: ns

HEX SCHMITT-TRIGGER INVERTERS



- $Y = \bar{A}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT	AHC	AHCT	UNIT
I_{CC}	MAX	60	21	0.02	0.04	0.02	0.04	0.02	0.08	0.02	0.08	0.02	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-4	-4	-24	-24	-24	-24	-8	-8	mA
I_{OL}	MAX	16	8	4	4	4	4	24	24	24	24	8	8	mA

PARAMETER	MAX or MIN	LV 3V	LV 5V	LVC 3V	ALVC 3V	UNIT
I_{CC}	MAX	-	0.02	0.01	0.01	mA
I_{OH}	MAX	-6	-12	-24	-24	mA
I_{OL}	MAX	6	12	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT
t_{PLH}	A or B	Y	MAX	22	22	31	41	40	57	11	10.5	12.5	14.5
t_{PHL}	A or B	Y	MAX	22	22	31	41	40	57	9.5	10.5	11	9.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V
t_{PLH}	A or B	Y	MAX	12	9	18.5	12	6.4	3.4
t_{PHL}	A or B	Y	MAX	12	9	18.5	12	6.4	3.4

UNIT: ns

16

HEX INVERTER BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

● $Y = \bar{A}$

RECOMMENDED OPERATING CONDITIONS

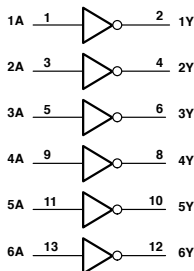
PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	51	mA
V_{OH}	MAX	15	V
I_{OL}	MAX	40	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	A	Y	MAX	15
t_{PHL}	A	Y	MAX	23

UNIT: ns

Logic Diagram



17

HEX BUFFERS/DRIVERS WITH OPEN-COLLECTOR HIGH-VOLTAGE OUTPUTS

● $Y = A$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	41	6.6
V_{OH}	MAX	15	V
I_{OL}	MAX	40	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	A	Y	MAX	15
t_{PHL}	A	Y	MAX	26

UNIT: ns

Logic Diagram



HEX SCHMITT-TRIGGER INVERTERS

- $Y = \overline{A}$
- P-N-P Input Reduce System Loading
($I_{IL} = -0.05\text{mA MAX}$)
- Excellent Noise Immunity with Typical Hysteresis of 0.8V

RECOMMENDED OPERATING CONDITIONS

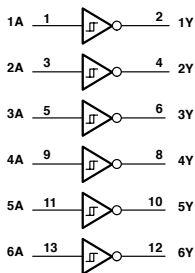
PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	30	mA
I_{OH}	MAX	-0.4	mA
I_{OL}	MAX	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t_{PLH}	A or B	Y	MAX	20
t_{PHL}	A or B	Y	MAX	30

UNIT: ns

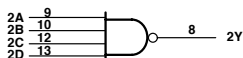
Logic Diagram



DUAL 4-INPUT POSITIVE-NAND GATES

- $Y = \overline{A \cdot B \cdot C \cdot D}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	CD74 AC	ACT 11	CD74 ACT	LV 3V	LV 5V	UNIT
I _{CC}	MAX	11	2.2	18	1.5	8.7	5.1	0.02	0.04	0.04	0.04	0.08	0.04	0.08	-	0.02	mA
I _{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	-24	-24	-6	-12	mA
I _{OL}	MAX	16	8	20	8	20	20	4	4	4	24	24	24	24	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	CD74 AC	ACT 11	CD74 ACT
t _{PLH}	A, B, C or D	Y	MAX	22	15	4.5	11	5	6	28	30	42	6.7	12.2	9.1	13.5
t _{PHL}	A, B, C or D	Y	MAX	15	15	5	10	4.5	5.3	28	30	42	7.3	12.2	9.2	13.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V
t _{PLH}	A, B, C or D	Y	MAX	11.5	8
t _{PHL}	A, B, C or D	Y	MAX	11.5	8

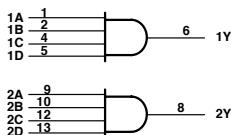
UNIT: ns

21

DUAL 4-INPUT
POSITIVE-AND
GATES

- $Y = A \cdot B \cdot C \cdot D$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V	UNIT
I_{CC}	MAX	4.4	2.3	12	7.3	0.02	0.04	0.04	0.04	0.04	-	0.02	mA
I_{OH}	MAX	-0.4	-0.4	-2	-1	-4	-4	-4	-24	-24	-6	-12	mA
I_{OL}	MAX	8	8	20	20	4	4	4	24	24	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V
t_{PLH}	A, B, C or D	Y	MAX	15	15	6	5.3	28	33	41	8.8	9.8	12	6
t_{PHL}	A, B, C or D	Y	MAX	20	10	6	5.5	28	33	41	6.9	8.9	12	8

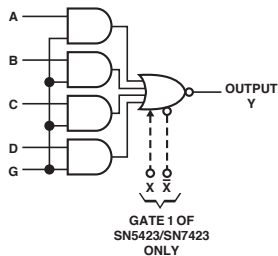
UNIT: ns

25

DUAL 4-INPUT
POSITIVE-NOR
GATES
WITH STROBE

- $Y = \overline{G(A + B + C + D)}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	19	mA
I_{OH}	MAX	-0.8	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	A or B	Y	MAX	22
t_{PHL}	A or B	Y	MAX	15

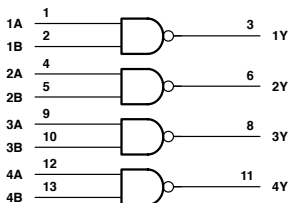
UNIT: ns

26

**QUADRUPLE 2-INPUT
HIGH-VOLTAGE INTERFACE
POSITIVE-NAND GATES**

$$\bullet Y = \overline{AB}$$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	22	4.4	mA
V_{OH}	MAX	15	15	V
I_{OL}	MAX	16	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
t_{PLH}	A or B	Y	MAX	24	32
t_{PHL}	A or B	Y	MAX	17	28

UNIT: ns

27

**TRIPLE 3-INPUT
POSITIVE-NOR GATES**

$$\bullet Y = \overline{A + B + C}$$

- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V	UNIT
I_{CC}	MAX	26	6.8	4	17.1	12	0.02	0.04	0.04	0.04	0.04	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-0.4	-2	-1	-4	-4	-4	-24	-24	-6	-12	mA
I_{OL}	MAX	16	8	8	20	20	4	4	4	24	24	6	12	mA

SWITCHING CHARACTERISTICS

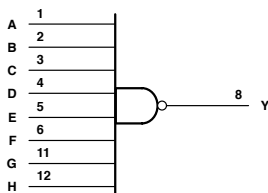
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	LV 3V	LV 5V
t_{PLH}	A, B or C	Y	MAX	15	15	15	5.5	5.5	23	29	35	7.7	10.1	14	9
t_{PHL}	A, B or C	Y	MAX	11	15	9	4.5	4.5	23	29	35	8.1	9.4	14	9

UNIT: ns

8-INPUT POSITIVE-NAND GATES

- $Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H}$
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11	UNIT
I _{CC}	MAX	6	1.1	10	0.9	4.9	4	0.02	0.04	0.04	0.04	0.04	mA
I _{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	mA
I _{OL}	MAX	16	8	20	8	20	20	4	4	4	24	24	mA

SWITCHING CHARACTERISTICS

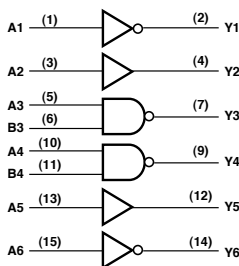
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	ACT 11
t _{PLH}	A thru H	Y	MAX	22	15	6	10	5	5.5	33	39	42	7.2	8.5
t _{PHL}	A thru H	Y	MAX	15	20	7	12	4.5	5	33	39	42	7.4	8.7

UNIT: ns

DELAY ELEMENTS

- Delay Elements for Generating Delay Line
- Inverting and Non-inverting Elements
- Buffer NAND Elements Rated at I_{OL} of 12/24mA
- P-N-P Inputs Reduce Fan-In (I_{IL} = -0.2mA MAX)
- Worst Case MIN/MAX Delays Guaranteed Across Temperature and V_{CC} Range

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I _{CC}	MAX	20	mA
I _{OH}	Y3, Y4 outputs	MAX	-1.2 mA
	All other outputs	MAX	-0.4 mA
I _{OL}	Y3, Y4 outputs	MAX	24 mA
	All other outputs	MAX	8 mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t _{PLH}	A1, A6	Y1, Y6	MAX	65
t _{PHL}				45
t _{PLH}	A2, A5	Y2, Y5	MAX	80
t _{PHL}				95
t _{PLH}	A3, B3	Y3, Y4	MAX	15
t _{PHL}				15

UNIT: ns

**QUADRUPLE 2-INPUT
POSITIVE-OR GATES**


$$\bullet Y = A + B$$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
I _{CC}	MAX	38	9.8	68	4.9	26.6	15.5	0.02	0.04	0.02	0.04	0.04	0.02	0.08	0.04	mA
I _{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
I _{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC	UNIT
I _{CC}	MAX	0.02	0.08	0.02	0.02	0.02	0.02	0.01	0.01	mA
I _{OH}	MAX	-24	-24	-8	-8	-6	-12	-24	-24	mA
I _{OL}	MAX	24	24	8	8	6	12	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC
t _{PLH}	A or B	Y	MAX	15	22	7	14	5.8	6.6	25	27	30	36	6.7	8.5
t _{PHL}	A or B	Y	MAX	22	22	7	12	5.8	-	25	27	30	36	5.9	7.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC 3V
t _{PLH}	A or B	Y	MAX	9.5	9	10	12.1	8.5	9	13	8.5	3.8	2.8
t _{PHL}	A or B	Y	MAX	9.5	8	10	12.1	8.5	9	13	8.5	3.8	2.8

UNIT: ns

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QUADRUPLE 2-INPUT POSITIVE-NOR BUFFERS WITH OPEN-COLLECTOR OUTPUTS

● $Y = \overline{A + B}$

RECOMMENDED OPERATING CONDITIONS

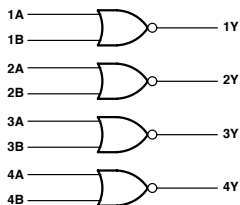
PARAMETER	MAX or MIN	TTL	LS	ALS	UNIT
I_{CC}	MAX	16.5	13.8	9	mA
V_{OH}	MAX	5.5	5.5	5.5	V
I_{OL}	MAX	48	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS
t_{PLH}	A or B	Y	MAX	15	32	33
t_{PHL}	A or B	Y	MAX	18	28	12

UNIT: ns

Logic Diagram



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HEX NONINVERTERS WITH OPEN-COLLECTOR OUTPUTS

● $Y = A$

RECOMMENDED OPERATING CONDITIONS

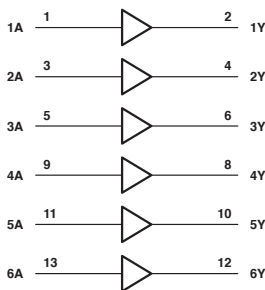
PARAMETER	MAX or MIN	ALS	UNIT
I_{CC}	MAX	63	mA
V_{OH}	MAX	5.5	V
I_{OL}	MAX	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A	Y	MAX	50
t_{PHL}	A	Y	MAX	14

UNIT: ns

Logic Diagram

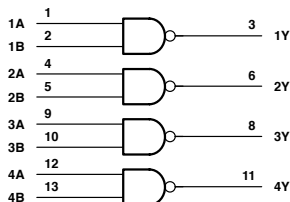


37

**QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS**

$$\bullet Y = \overline{A \cdot B}$$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	UNIT
I_{CC}	MAX	54	12	80	7.8	33	mA
I_{OH}	MAX	-1.2	-1.2	-3	-2.6	-15	mA
I_{OL}	MAX	48	24	60	24	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F
t_{PLH}	A or B	Y	MAX	22	24	6.5	8	6.5
t_{PHL}	A or B	Y	MAX	15	24	6.5	7	5

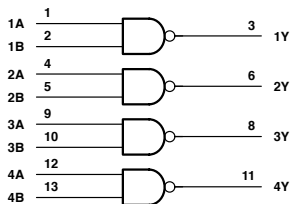
UNIT: ns

38

**QUADRUPLE 2-INPUT
POSITIVE-NAND BUFFERS
WITH OPEN-COLLECTOR OUTPUTS**

$$\bullet Y = \overline{A \cdot B}$$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	UNIT
I_{CC}	MAX	54	12	80	7.8	30	mA
V_{OH}	MAX	5.5	5.5	5.5	5.5	4.5	V
I_{OL}	MAX	48	24	60	24	64	mA

SWITCHING CHARACTERISTICS

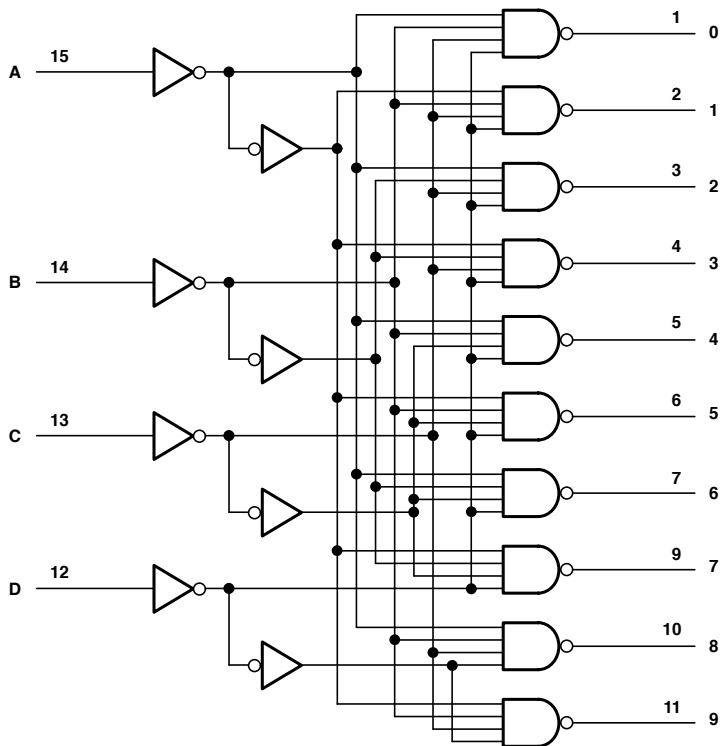
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F
t_{PLH}	A or B	Y	MAX	22	32	10	33	13
t_{PHL}	A or B	Y	MAX	18	28	10	12	5.5

UNIT: ns

4-LINE TO 10-LINE DECODERS

- All Outputs Are High for Invalid Input Conditions
- Also for Applications as
 - 3-Line to 8-Line Decoders
 - 4-Line to 16-Line Decoders
- Full Decoding of Valid Input Logic Ensures That All Inputs Remain Off for All Invalid Input Conditions

Logic Diagram



FUNCTION TABLE

No.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	L	H	H	H
8	H	L	L	L	H	H	H	H	H	H	H	L	H	H
9	H	L	L	H	H	H	H	H	H	H	H	H	L	H
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	56	13	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-4	mA
I_{OL}	MAX	16	8	4	4	4	mA

SWITCHING CHARACTERISTICS

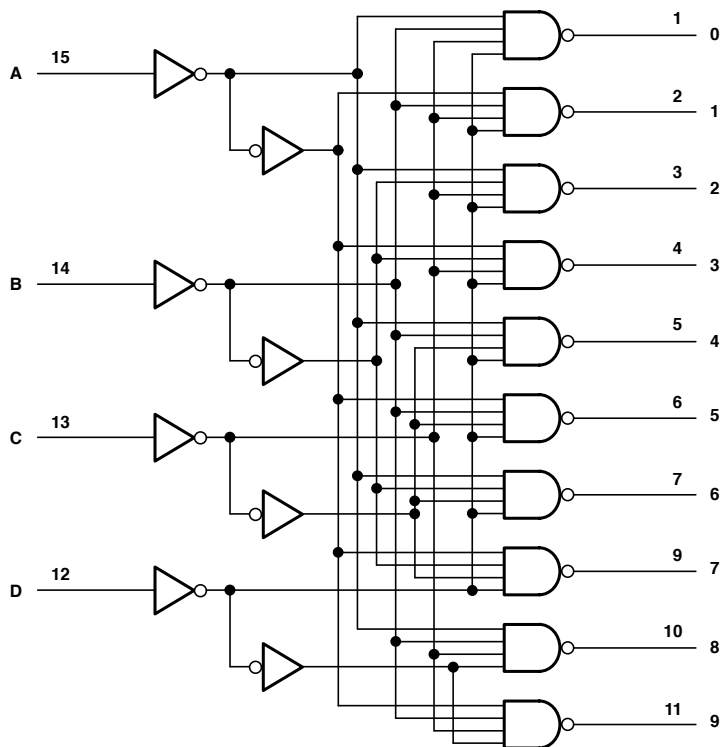
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH} 2Level Logic	A, B, C or D	0-9	MAX	25	25	38	45	53
t_{PHL} 2Level Logic		0-9		25	25	38	45	53
t_{PLH} 3Level Logic	A, B, C or D	0-9	MAX	30	30	38	45	53
t_{PHL} 3Level Logic		0-9		30	30	38	45	53

UNIT: ns

BCD-TO-DECIMAL DECODER/DRIVER

- 80-mA Sink-Current Capability
- All Outputs Are Off for Invalid BCD Input Conditions

Logic Diagram



FUNCTION TABLE

No.	INPUTS				OUTPUTS									
	D	C	B	A	0	1	2	3	4	5	6	7	8	9
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H
5	L	H	L	H	H	H	H	H	H	L	H	H	H	H
6	L	H	H	L	H	H	H	H	H	H	L	H	H	H
7	L	H	H	H	H	H	H	H	H	H	H	L	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H
	H	H	H	H	H	H	H	H	H	H	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	70	mA
$V_O(\text{on})$	MAX	0.9	V
I_{OL}	MAX	80	mA

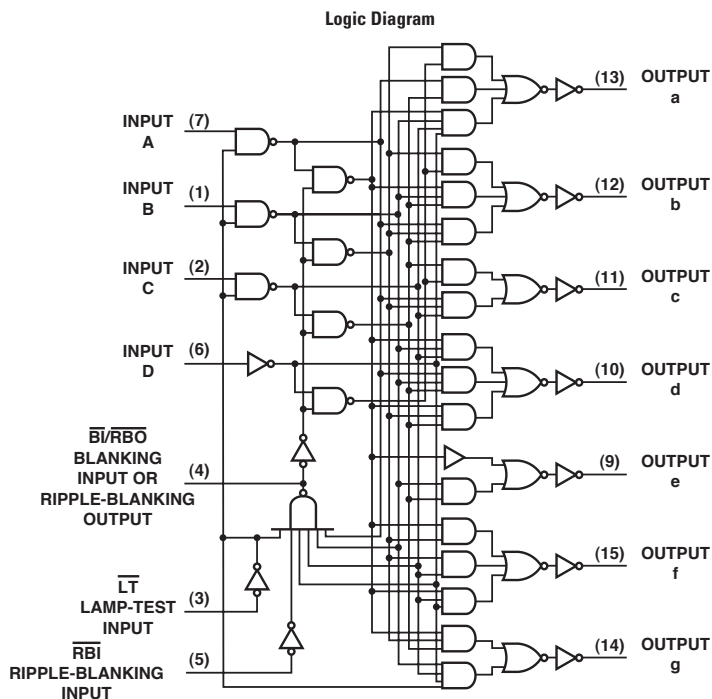
SWITCHING CHARACTERISTICS

PARAMETER	MAX or MIN	TTL
t_{PLH}	MAX	25
t_{PHL}		25

UNIT: ns

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS

- Open-Collector Outputs
- Lamp-Test Provision
- Leading/Trailing Zero Suppression



FUNCTION TABLE

No.	INPUTS					B/RBO	OUTPUTS							
	LT	RBI	D	C	B		A	a	b	c	d	e	f	g
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF
2	H	X	L	L	H	L	H	ON	ON	OFF	ON	ON	OFF	ON
3	H	X	L	L	H	H	H	ON	ON	ON	ON	OFF	OFF	ON
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON
6	H	X	L	H	H	L	H	OFF	OFF	ON	ON	ON	ON	ON
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON
9	H	X	H	L	L	H	H	ON	ON	ON	OFF	OFF	ON	ON
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON
11	H	X	H	L	H	H	H	OFF	OFF	ON	ON	OFF	OFF	ON
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I _{CC}	MAX	103	13	mA
I _{OH}	MAX	-0.2	-0.05	mA
I _{OL}	MAX	8	3.2	mA

SWITCHING CHARACTERISTICS

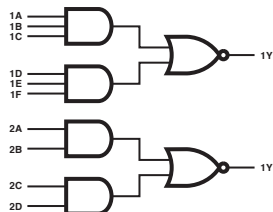
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
t _{off}	A	A to g	MAX	100	100
t _{on}	A	A to g	MAX	100	100
t _{off}	RBI	A to g	MAX	100	100
t _{on}	RBI	A to g	MAX	100	100

UNIT: ns

AND-OR INVERT GATES

- '51, 'S51: $Y = \overline{AB + CD}$
- 'F51, 'LS51: $1Y = \overline{(1A \cdot 1B \cdot 1C) + (1D \cdot 1E \cdot 1F)}$
- 'HC51: $2Y = \overline{(2A \cdot 2B) + (2C \cdot 2D)}$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	F	SN74 HC	UNIT
I_{CC}	MAX	14	2.8	22	7.5	0.08	mA
I_{OH}	MAX	-0.4	-0.4	-1	-1	-4	mA
I_{OL}	MAX	16	8	20	20	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	F	SN74 HC
t_{PLH}	Any	Y	MAX	22	20	5.5	6.5	35
t_{PHL}	Any	Y	MAX	15	20	5.5	4.5	35

UNIT: ns

4-2-3-2 INPUT AND-OR INVERT GATE

$$\bullet Y = \overline{ABCD + EF + GHI + JK}$$

RECOMMENDED OPERATING CONDITIONS

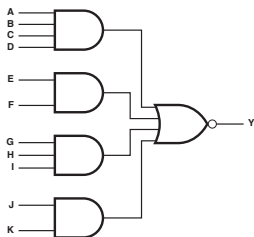
PARAMETER	MAX or MIN	S	F	UNIT
I _{CC}	MAX	16	4.7	mA
I _{OH}	MAX	-1	-1	mA
I _{OL}	MAX	20	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S	F
t _{PLH}	Any	Y	MAX	5.5	7
t _{PHL}	Any	Y	MAX	5.5	5.5

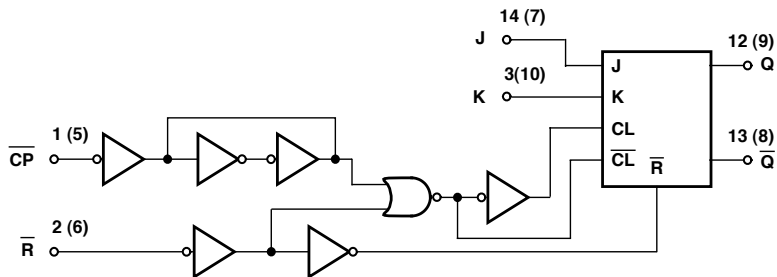
UNIT: ns

Logic Diagram

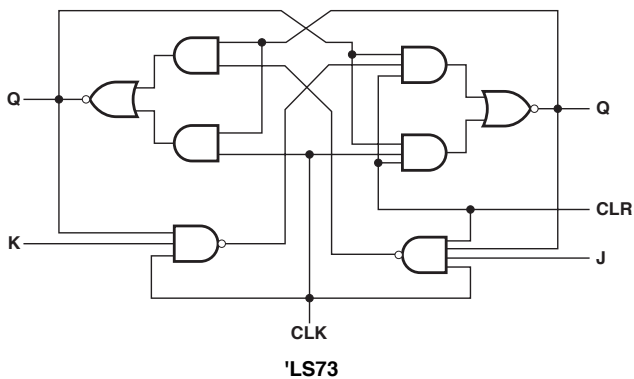


DUAL J-K FLIP-FLOPS WITH CLEAR

Logic Diagram



CD74HC/HCT73



'LS73

FUNCTION TABLE (SN74)

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	↓	L	L	Q ₀	\bar{Q} ₀
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	TOGGLE	TOGGLE
H	H	X	X	Q ₀	\bar{Q} ₀

TRUTH TABLE (CD74)

INPUTS				OUTPUTS	
\bar{R}	$\bar{C}P$	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	↓	L	L	No Change	No Change
H	↓	H	L	H	L
H	↓	L	H	L	H
H	↓	H	H	Toggle	Toggle
H	H	X	X	No Change	No Change

NOTE:

H = High Level (Steady State)

L = Low Level (Steady State)

X = Irrelevant

↓ = High-to-Low Transition

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	20	6	0.04	0.08	0.08	mA
I _{OH}	MAX	16	8	4	4	4	mA
I _{OL}	MAX	-0.4	-0.4	-4	-4	-4	mA

SWITCHING CHARACTERISTICS

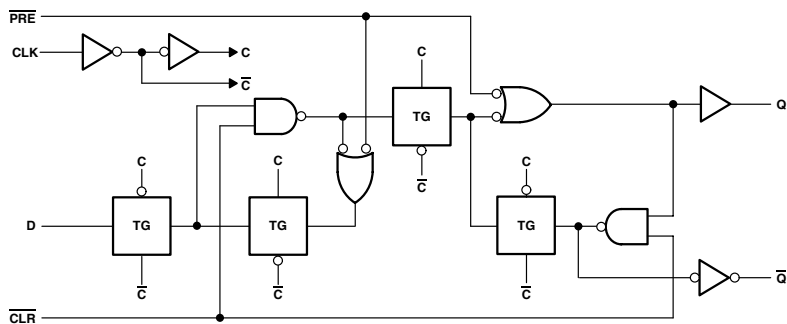
PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
t _{max}	CLOCK'L'			MIN	15	30	25	20	20
				MIN	20	-	20	-	-
				MIN	47	20	20	-	-
				MIN	-	-	-	24	24
t _{su}	CLK	J,K to $\bar{C}P$		MIN	0 *	20	25	-	-
				MIN	-	-	-	24	24
				MIN	0	0	0	-	-
				MIN	-	-	-	3	3
t _{PHL}	CLEAR	\bar{Q}	MAX	MAX	25	20	39	44	51
				MAX	-	20	39	44	51
t _{PLH}	CLEAR	Q	MAX	MAX	-	20	39	44	51
				MAX	40	20	39	44	51
t _{PLH}	CLOCK	Q or \bar{Q}	MAX	MAX	25	20	32	-	-
				MAX	40	20	32	-	-
t _{PLH}	$\bar{C}P$	Q	MAX	MAX	-	-	-	48	57
				MAX	-	-	-	48	57
t _{PLH}	$\bar{C}P$	\bar{Q}	MAX	MAX	-	-	-	48	54
				MAX	-	-	-	48	54

UNIT f_{max} : MHz, other : ns

DUAL D-TYPE POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUTS	
PRESET	CLEAR	CLOCK	D	Q	\bar{Q}
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H*	H*
H	H	↓	H	H	L
H	H	↓	L	L	H
H	H	L	X	Q ₀	\bar{Q} ₀

† This configuration is unstable; that is, it does not persist when PRE or CLR returns to its inactive (high) level.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
I _{CC}	MAX	15	8	25	4	16	16	0.04	0.08	0.04	0.08	0.04	0.02	0.08	0.04	mA
I _{OH}	MAX	-0.4	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	-24	-24	-24	mA
I _{OL}	MAX	16	8	20	8	20	20	4	4	4	4	24	24	24	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I _{CC}	MAX	0.02	0.08	0.02	0.02	-	0.02	0.01	mA
I _{OH}	MAX	-24	-24	-8	-8	-6	-12	-24	mA
I _{OL}	MAX	24	24	8	8	6	12	24	mA

SWITCHING CHARACTERISTICS

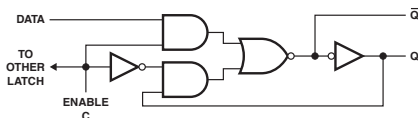
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11
t _{max}			MIN	15	25	75	34	105	100	25	20	24	16	125
t _w	CLOCK'H'		MIN	30	25	6	14.5	4	4	20	24	23	27	4
	CLOCK'L'		MIN	37	-	7.3	14.5	5.5	5	20	24	23	27	4
t _{su}	RESET or CLEAR 'L'		MIN	30	25	7	15	4	4	25	24	20	24	4
	D		MIN	20	20	3	15	4.5	3	25	18	15	18	3.5
t _h	PRE, CLR INACTIVE		MIN	20	-	-	10	2	2	6	-	0	5	1
			MIN	5	5	2	0	0	1	0	3	0	3	0
I _{PLH}	RESET	Q	MAX	25	25	6	13	7.5	7.1	58	60	44	60	7.1
I _{PHL}		\bar{Q}	MAX	40	40	13.5	15	10.5	10.5	58	60	44	60	9
I _{PLH}	CLEAR	Q	MAX	25	25	6	13	7.5	7.1	58	60	44	60	7.1
I _{PHL}		\bar{Q}	MAX	40	40	13.5	15	10.5	10.5	58	60	44	60	9
I _{PLH}	CLOCK	Q or \bar{Q}	MAX	25	25	9	16	8	7.8	44	53	35	53	8.2
I _{PHL}		Q or \bar{Q}	MAX	40	40	9	18	9	9.2	44	53	35	53	7.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t _{max}			MIN	125	110	85	125	85	75	65	45	75	100
t _w	CLOCK'H'		MIN	5	4.5	5	6	5.7	5	5	7	5	3.3
	CLOCK'L'		MIN	5	4.5	5	6	5.7	5	5	7	5	3.3
t _{su}	RESET or CLEAR 'L'		MIN	5	4	5	6	5	5	5	7	5	3.3
	D		MIN	3	3.5	4.5	3.5	4	5	5	7	5	3
t _h	PRE, CLR INACTIVE		MIN	0	-	2	0	-	3	3.5	5	3	2
			MIN	0.5	0	0	1	9.5	0.5	0	0.5	0.5	0
I _{PLH}	RESET	Q	MAX	10	10.5	9.6	11.5	11.5	11	13	18	11	5.4
I _{PHL}		\bar{Q}	MAX	10.5	11.5	12.5	12.5	12.5	11	13	18	11	5.4
I _{PLH}	CLEAR	Q	MAX	10	10.5	9.6	11.5	11.5	11	13	18	11	5.4
I _{PHL}		\bar{Q}	MAX	10.5	11.5	12.5	12.5	12.5	11	13	18	11	5.4
I _{PLH}	CLOCK	Q or \bar{Q}	MAX	10.5	10	9.4	14	9.5	10.5	10	17.5	10.5	5.2
I _{PHL}		Q or \bar{Q}	MAX	10.5	10	8.8	12	9.5	10.5	10	17.5	10.5	5.2

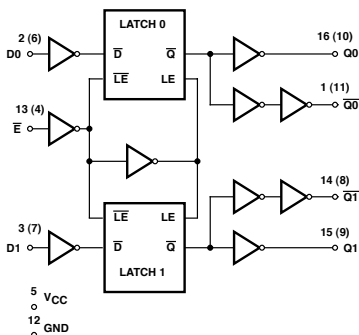
UNIT f_{max} : MHz, other : ns

4-BIT BISTABLE LATCHES

Logic Diagram



SN74LS75



CD74HC/HCT75

FUNCTION TABLE

INPUTS		OUTPUTS	
D	C	Q	\bar{Q}
L	H	L	H
H	H	H	L
X	L	Q_0	\bar{Q}_0

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	53	12	0.04	0.08	0.08	mA
I_{OH}	MAX	-0.4	-0.4	-4	-4	-4	mA
I_{OL}	MAX	16	8	4	4	4	mA

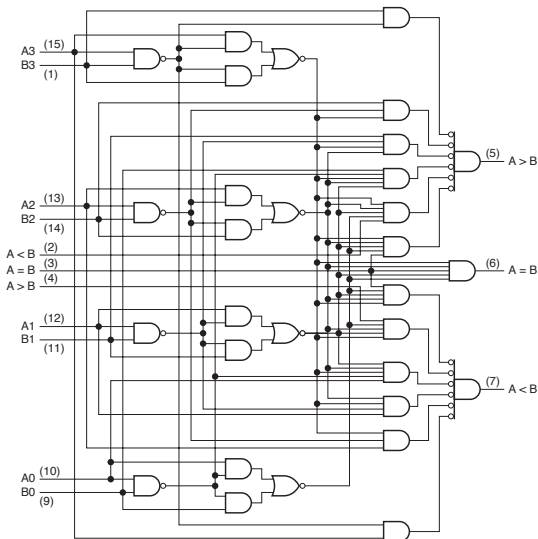
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
t_{w}			MIN	20	20	20	24	24
t_{su}				20	20	25	18	18
t_h			MIN	5	5	5	3	3
t_{PLH}	D	Q	MAX	30	27	30	33	42
t_{PHL}	D	Q	MAX	25	17	30	33	42
t_{PLH}	D	\bar{Q}	MAX	40	20	30	39	42
t_{PHL}	D	\bar{Q}	MAX	15	15	30	39	42
t_{PLH}	G	Q	MAX	30	27	33	39	42
t_{PHL}	G	Q	MAX	15	25	33	39	42
t_{PLH}	G	\bar{Q}	MAX	30	30	33	39	45
t_{PHL}	G	\bar{Q}	MAX	15	15	33	39	45

UNIT: ns

4-BIT MAGNITUDE COMPARATORS

Logic Diagram



FUNCTION TABLE

COMPARING INPUTS				CASCADING INPUTS			OUTPUTS		
A3, B3	A2, B2	A1, B1	A0, B0	A>B	A<B	A=B	A>B	A<B	A=B
A3>B3	X	X	X	X	X	X	H	L	L
A3<B3	X	X	X	X	X	X	L	H	L
A3=B3	A2>B2	X	X	X	X	X	H	L	L
A3=B3	A2<B2	X	X	X	X	X	L	H	L
A3=B3	A2=B2	A1>B1	X	X	X	X	H	L	L
A3=B3	A2=B2	A1<B1	X	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0>B0	X	X	X	H	L	L
A3=B3	A2=B2	A1=B1	A0<B0	X	X	X	L	H	L
A3=B3	A2=B2	A1=B1	A0=B0	H	L	L	H	L	L
A3=B3	A2=B2	A1=B1	A0=B0	H	H	L	L	L	L
A3=B3	A2=B2	A1=B1	A0=B0	L	L	L	H	H	L
A3=B3	A2=B2	A1=B1	A0=B0	X	X	H	L	L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	88	20	115	0.08	0.16	0.16	mA
I _{OH}	MAX	-0.4	-0.4	-1	-4	-4	-4	mA
I _{OL}	MAX	16	8	20	4	4	4	mA

SWITCHING CHARACTERISTICS

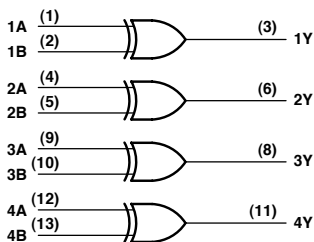
PARAMETER	INPUT	OUTPUT	Number of Gate Levels	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT
t _{PLH}	Any A or B data input	A, B, A, B	3	MAX	26	36	16	58	59	56
		A, B	4	MAX	35	45	18	50	53	60
t _{PHL}	Any A or B data input	A, B, A, B	3	MAX	30	30	16.5	58	59	56
		A, B	4	MAX	30	45	16.5	50	53	60
t _{PLH}	A, B, A, B	A, B	1	MAX	11	22	7.5	44	42	45
		A, B, A, B	1		17	17	8.5	44	42	45
t _{PHL}	A, B	A, B	2	MAX	20	20	10.5	37	-	-
		A, B	2		17	26	7.5	37	-	-
t _{PLH}	A, B, A, B	A, B	1	MAX	11	22	7.5	44	42	47
		A, B, A, B	1		17	17	8.5	44	42	47

UNIT: ns

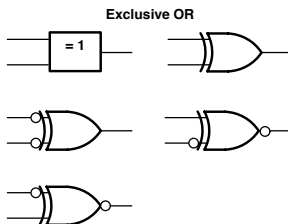
QUADRUPLE 2-INPUT EXCLUSIVE-OR GATES

- $Y = A \oplus B$ or $Y = \bar{A}B + A\bar{B}$
- 74AC11xxx : Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11	UNIT
I_{CC}	MAX	50	10	75	5.9	38	28	0.02	0.04	0.04	0.04	0.02	0.08	0.04	mA
I_{OH}	MAX	16	8	20	8	20	20	4	4	4	24	24	24	24	mA
I_{OL}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	-24	-24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	0.04	0.08	0.02	0.02	-	0.02	0.01	mA
I_{OH}	MAX	24	24	8	8	6	12	24	mA
I_{OL}	MAX	-24	-24	-8	-8	-6	-12	-24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	SN74 AC	CD74 AC	ACT 11
t_{PLH}	A or B	Y	MAX	23	23	10.5	17	7.5	6.5	25	36	48	7.6	9	10.8	9.6
t_{PHL}		Y	MAX	17	17	10	12	6.5	6.5	25	36	48	6.8	9.5	10.8	9
t_{PLH}	A or B	Y	MAX	30	30	10.5	17	6.5	8	25	36	48	7.6	9	10.8	9.6
t_{PHL}		Y	MAX	22	22	10	10	7	7.5	25	36	48	6.8	9.5	10.8	9

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t_{PLH} Input Low	A or B	Y	MAX	10	14.6	10	10	16.5	10	4.6
t_{PHL} Input Low		Y	MAX	10.5	14.6	10	10	16.5	10	4.6
t_{PLH} Input High	A or B	Y	MAX	10	14.6	10	10	16.5	10	4.6
t_{PHL} Input High		Y	MAX	10.5	14.6	10	10	16.5	10	4.6

UNIT: ns

DECADE COUNTER

FUNCTION TABLE

BCD COUNT SEQUENCE

Count	OUTPUTS			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	H	L	L
4	L	H	L	H
5	L	H	H	L
6	L	H	H	H
7	H	L	L	L
8	H	L	L	H
9	H	L	H	L

BI-QUINARY

Count	OUTPUTS			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	H	L	L
4	L	H	L	H
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

RESET/COUNT
FUNCTION TABLE

RESET INPUTS				OUTPUTS			
R ₀ (1)	R ₀ (2)	R ₁ (1)	R ₁ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	X	L	L	L	L
H	H	X	L	L	L	L	L
X	X	H	H	H	L	L	L
X	L	X	L				Count
L	X	L	X				Count
L	X	X	L				Count
X	L	L	X				Count

RECOMMENDED OPERATING CONDITIONS

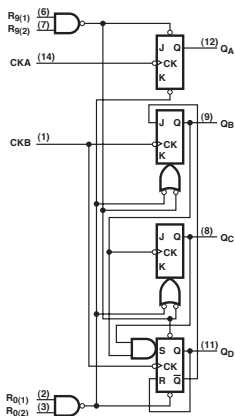
PARAMETER	MAX or MIN	TTL	LS	UNIT
I _{CC}	MAX	39	15	mA
I _{OH}	MAX	-0.8	-0.4	mA
I _{OL}	MAX	16	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
f _{max}	A	Q _A	MIN	32	32
	B	Q _B		16	16
t _w	A		MIN	15	15
	B			30	30
t _{su}	RESET		MIN	15	30
	RESET INACTIVE			25	25
t _{PLH}	A	Q _A	MAX	16	16
t _{PHL}				18	18
t _{PLH}	A	Q _D	MAX	48	48
t _{PHL}				50	50
t _{PLH}	B	Q _B	MAX	16	16
t _{PHL}				21	21
t _{PLH}	B	Q _C	MAX	32	32
t _{PHL}				35	35
t _{PLH}	B	Q _C	MAX	32	32
t _{PHL}				35	35
t _{PHL}	Set to 0	Any	MAX	40	40
t _{PLH}	Set to 9	Q _A , Q _D	MAX	30	30
t _{PHL}		Q _B , Q _C		40	40

UNIT f_{max}: MHz, other: ns

Logic Diagram

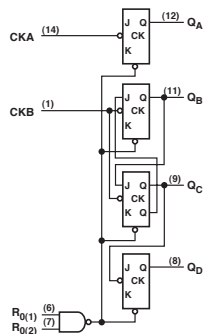


DIVIDE-BY-12 COUNTERS

FUNCTION TABLE

COUNT	OUTPUTS			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	H	L	L	L
7	H	L	L	H
8	H	H	L	L
9	H	H	L	H
10	H	H	L	L
11	H	H	L	H

RESET INPUTS		OUTPUTS			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X				COUNT
X	L				COUNT



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I _{CC}	MAX	39	15	mA
I _{OH}	MAX	-0.8	-0.4	mA
I _{OL}	MAX	16	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
f _{max}	A	Q _A	MIN	32	32
	B	Q _B		16	16
t _w	A		MIN	15	15
	B			30	30
	RESET			15	30
t _{su}	RESET INACTIVE		MIN	25	25
t _{PLH}	A	Q _A	MAX	16	16
t _{PHL}		Q _D		18	18
t _{PLH}	A	Q _D	MAX	48	48
t _{PHL}		Q _B		50	50
t _{PLH}	B	Q _B	MAX	16	16
t _{PHL}		Q _C		21	21
t _{PLH}	B	Q _C	MAX	16	16
t _{PHL}		Q _D		21	21
t _{PLH}	B	Q _D	MAX	32	32
t _{PHL}		Any		35	35
t _{PHL}	Set to 0	Any	MAX	40	40

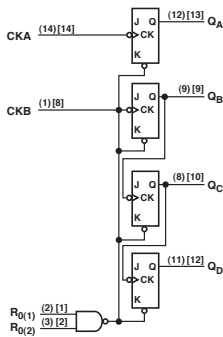
UNIT f_{max}: MHz, other: ns

4-BIT BINARY COUNTERS

FUNCTION TABLE

COUNT	OUTPUTS			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

RESET INPUTS		OUTPUTS			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	39	15	0.16	0.16	mA
I _{OH}	MAX	-0.8	-0.4	-4	-4	mA
I _{OL}	MAX	16	8	4	4	mA

SWITCHING CHARACTERISTICS

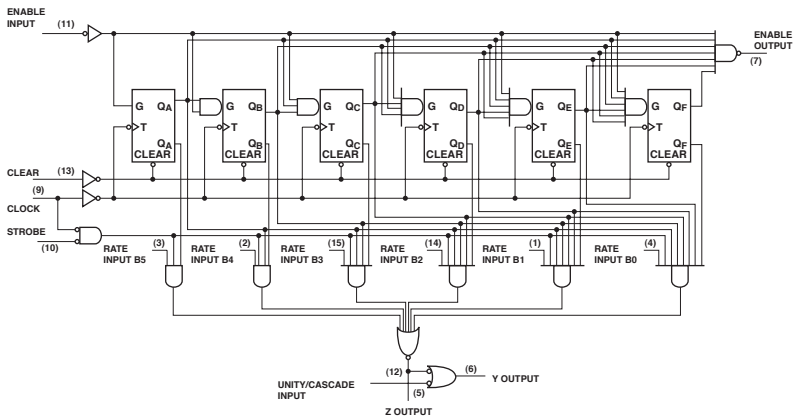
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT
f _{max}	A	QA	MIN	32	32	20	20
	B	QB		16	16	20	20
t _w	A	MIN	15	15	24	24	
	B		30	30	24	24	
	RESET		15	30	24	24	
t _{su}	RESET INACTIVE	MIN	25	25	-	-	
t _{PLH}	A	QA	MAX	16	16	38	51
t _{PHL}		QB	18	18	38	51	
t _{PLH}	A	QD	MAX	70	70	-	87
t _{PHL}		QD	70	70	-	87	
t _{PLH}	B	QB	MAX	16	16	41	51
t _{PHL}		QB	21	21	41	51	
t _{PLH}	B	QC	MAX	32	32	56	69
t _{PHL}		QC	35	35	56	69	
t _{PLH}	B	QD	MAX	51	51	74	87
t _{PHL}		QD	51	51	74	87	
t _{PHL}	Set to 0	ANY	MAX	40	40	-	-

UNIT f_{max} : MHz, other : ns

SYNCHRONOUS 6-BIT BINARY RATE MULTIPLIER

- Perform Fixed-Rate or Variable-Rate Frequency Division
- Typical Maximum Clock Frequency: 32MHz

Logic Diagram



FUNCTION TABLE

INPUTS							OUTPUTS					
CLEAR	ENABLE	STROBE	BINARY RATE				NUMBER OF CLOCK PULSES	UNITY/ CASCADE	LOGI LEVEL OR NUMBER OF PULSES			
			F	E	D	C			B	A	Y	Z
H	X	H	X	X	X	X	X	H	L	H	H	
L	L	L	L	L	L	L	L	64	H	L	H	1
L	L	L	L	L	L	L	L	64	H	L	H	1
L	L	L	L	L	L	L	L	64	H	2	2	1
L	L	L	L	L	L	H	L	64	H	4	4	1
L	L	L	L	L	H	L	L	64	H	8	8	1
L	L	L	L	H	L	L	L	64	H	16	16	1
L	L	L	H	L	L	L	L	64	H	32	32	1
L	L	L	H	H	H	H	H	64	H	63	63	1
L	L	L	H	H	H	H	H	64	L	H	63	1
L	L	L	H	L	H	L	L	64	H	40	40	1

RECOMMENDED OPERATING CONDITIONS

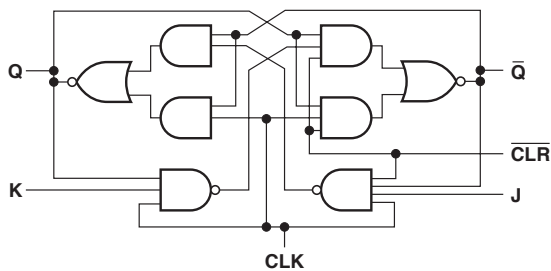
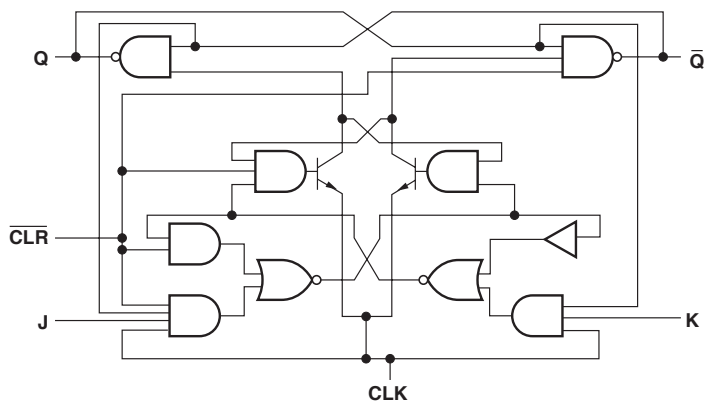
PARAMETER	MAX or MIN	TTL	UNIT
I _{CC}	MAX	120	mA
I _{OH}	MAX	16	mA
I _{OL}	MAX	-0.4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
f _{max}	A	QA	MIN	25
t _w	CLK		MIN	20
	CLR		MIN	15
t _{su}	Positive		MIN	25
	Negative		MIN	0
t _h	Positive		MIN	0
	Negative		MIN	20
t _{PLH}	ENABLE	ENABLE	MAX	20
t _{PHL}			MAX	21
t _{PLH}	STRB	Z	MAX	18
t _{PHL}			MAX	23
t _{PLH}	CLK	Y	MAX	39
t _{PHL}			MAX	30
t _{PLH}	CLK	Z	MAX	18
t _{PHL}			MAX	26
t _{PLH}	RATE	Z	MAX	10
t _{PHL}			MAX	14
t _{PLH}	UNITY /CAS	Y	MAX	14
t _{PHL}			MAX	10
t _{PLH}	STRB	Y	MAX	30
t _{PHL}			MAX	33
t _{PLH}	CLK	ENABLE	MAX	30
t _{PHL}			MAX	33
t _{PLH}	CLR	Y	MAX	36
t _{PHL}			Z	MAX
t _{PLH}	RATE	Y	MAX	23
t _{PHL}			MAX	23

UNIT: f_{max} - MHz; other - ns

Logic Diagram



FUNCTION TABLES

'107

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	\downarrow	L	L	Q ₀	Q ₀
H	\downarrow	H	L	H	L
H	\downarrow	L	H	L	H
H	\downarrow	H	H	TOGGLE	

'LS107A, HC107

INPUTS				OUTPUTS	
CLEAR	CLOCK	J	K	Q	\bar{Q}
L	X	X	X	L	H
H	\downarrow	L	L	Q ₀	Q ₀
H	\downarrow	H	L	H	L
H	\downarrow	L	H	L	H
H	\downarrow	H	H	TOGGLE	
H	H	X	X	Q ₀	Q ₀

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	20	6	0.04	0.08	0.08	mA
I _{OH}	MAX	-0.4	-0.4	-4	-4	-4	mA
I _{OL}	MAX	16	8	4	4	4	mA

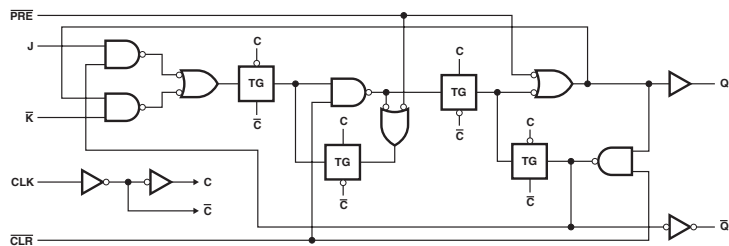
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
f _{max}			MIN	15	30	25	20	19
t _w	CLK H		MIN	20	20	20	-	-
	CLK L		MIN	47	-	20	-	-
	\bar{CP}		MIN	-	-	-	24	27
	\overline{CLR} L (or \bar{R})		MIN	25	25	20	25	36
t _{su}	J, K		MIN	0	20	25	30	30
	CLR INACTIVE		MIN	0	25	25	-	-
t _h			MIN	0	0	0	3	5
t _{PLH}	\overline{CLR} (or \bar{R})	\bar{Q}	MAX	25	20	39	47	57
t _{PHL}		Q	MAX	40	20	39	47	57
t _{PLH}	CLK	\bar{Q}	MAX	25	20	32	-	-
t _{PHL}		Q	MAX	40	20	32	-	-
t _{PLH}	\bar{CP}	Q	MAX	-	-	-	51	65
t _{PHL}		\bar{Q}	MAX	-	-	-	51	65
t _{PLH}	\bar{CP}	\bar{Q}	MAX	-	-	-	51	60
t _{PHL}		Q	MAX	-	-	-	51	60

 UNIT f_{max}: MHz, other: ns

DUAL J-K̄ POSITIVE-EDGE-TRIGGERED FLIP-FLOPS WITH PRESET AND CLEAR

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUTS	
PRESET	CLEAR	CLOCK	J	\bar{K}	Q	\bar{Q}
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H†	H†
H	H	↑	L	L	L	H
H	H	↑	H	L	TOGGLE	
H	H	↑	L	H	Q ₀	\bar{Q} ₀
H	H	↑	H	H	H	\bar{L}
H	H	L	X	X	Q ₀	\bar{Q} ₀

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} . Furthermore, this configuration is nonstable; that is, it will not persist when either PRE or CLR returns to its inactive (high) level.

RECOMMENDED OPERATING CONDITIONS

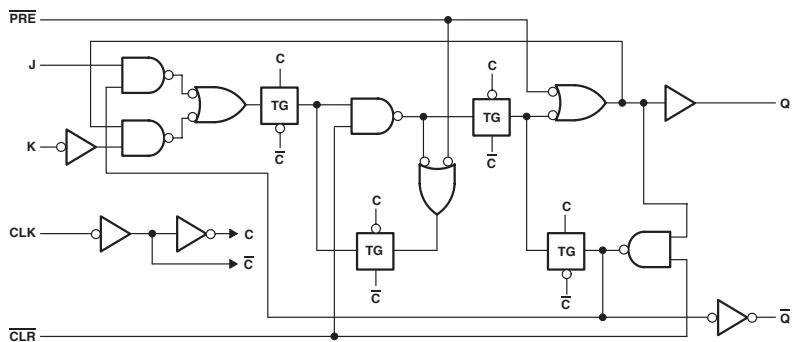
PARAMETER	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I _{CC}	MAX	15	8	4	17	17	0.04	0.08	0.08	0.08	0.08	mA
I _{OH}	MAX	-0.8	-0.4	-0.4	-2	-1	-4	-4	-4	-24	-24	mA
I _{OL}	MAX	16	4	8	20	20	4	4	4	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	
f _{max}			MIN	25	25	34	105	90	25	25	19	100	100	
t _w	CLK H		MIN	20	25	14.5	4	4	20	-	-	-	-	
			MIN	20	-	14.5	5.5	5	20	-	-	-	-	
			MIN	-	-	-	-	-	-	-	24	27	5	5
			MIN	20	25	15	4	4	25	-	-	-	-	
			MIN	20	25	15	4	4	25	-	-	-	-	
			MIN	-	-	-	-	-	-	-	24	36	4.5	5.5
t _{su}	J, K		MIN	10	25	15	5.5	3	25	-	-	-	-	
			MIN	10	-	10	2	2	6	-	-	-	-	
			MIN	-	-	-	-	-	-	-	30	30	5.5	5.5
			MIN	6	5	0	0	1	0	3	5	0	1	
t _{PHL}	PRE	Q	MAX	15	25	13	8	8	58	-	-	-	-	
		\bar{Q}	MAX	35	40	15	10.5	10.5	58	-	-	-	-	
t _{PHL}	CLR	\bar{Q}	MAX	15	25	13	8	8	58	-	-	-	-	
		Q	MAX	25	40	15	10.5	10.5	58	-	-	-	-	
t _{PLH}	CLK	\bar{Q}, Q	MAX	16	25	16	9	8	44	-	-	-	-	
		MAX	28	40	18	9	9.2	44	-	-	-	-		
t _{PLH}	$\bar{C}P$	Q	MAX	-	-	-	-	-	-	51	65	10.3	10.3	
			MAX	-	-	-	-	-	-	51	65	10.3	10.3	
t _{PHL}	$\bar{C}P$	\bar{Q}	MAX	-	-	-	-	-	-	51	60	10.3	10.3	
			MAX	-	-	-	-	-	-	51	60	10.3	10.3	
t _{PLH}	\bar{R}	\bar{Q}, Q	MAX	-	-	-	-	-	-	47	57	12.2	12.2	
			MAX	-	-	-	-	-	-	47	57	12.2	12.2	

UNIT f_{max} : MHz, other : ns

Logic Diagram



FUNCTION TABLE

CLEAR	INPUTS				OUTPUTS	
	A1	A2	B	B2	Q	\bar{Q}
L	X	X	X	X	L	H
X	H	H	X	X	L†	H†
X	X	X	L	X	L†	H†
X	X	X	X	L	L†	H†
H	L	X	↑	H		
H	L	X	H	↑		
H	X	L	↑	H		
H	X	L	H	↑		
H	H	↓	H	H		
H	↓	↓	H	H		
H	↓	H	H	H		
↑	L	X	H	H		
↑	X	L	H	H		

See explanation of function table on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LVC 3V	UNIT
I _{CC}	MAX	6	25	4.5	19	0.04	0.08	0.08	0.08	0.08	0.01	mA
I _{OH}	MAX	-0.4	-1	-0.4	-1	-4	-4	-4	-24	-24	-24	mA
I _{OL}	MAX	8	20	8	20	4	4	4	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	LVC 3V
t _{max}			MIN	30	80	30	100	20	20	20	150
t _w	$\overline{\text{PRE}}/\overline{\text{CLR}}$		MIN	25	8	10	5	25	24	27	-
	CLK H		MIN	20	6	16.5	5	25	-	-	3.3
	CLK L		MIN	-	6.5	16.5	5	25	-	-	3.3
	$\overline{\text{CP}}$		MIN	-	-	-	-	-	24	24	-
t _{su}	DATA		MIN	20	7	22	5	25	24	24	2.3
	$\overline{\text{PRE}}$ INACTIVE		MIN	25	-	20	5	25	-	-	2.4
	$\overline{\text{CLR}}$ INACTIVE		MIN	20	-	20	5	25	-	-	2.4
t _h			MIN	0	0	0	0	0	0	3	0.7
t _{PLH}	$\overline{\text{PRE}}$ or $\overline{\text{CLR}}$	Q or \bar{Q}	MAX	20	7	15	7.5	41	-	-	4.8
t _{PHL}		MAX	20	7	18	7.5	41	-	-	4.8	
t _{PLH}	CLK	Q or \bar{Q}	MAX	20	7	15	7.5	31	-	-	5.9
t _{PHL}		MAX	20	7	19	7.5	31	-	-	5.9	
t _{PLH}	$\overline{\text{CP}}$	Q or \bar{Q}	MAX	-	-	-	-	-	53	53	-
t _{PHL}		MAX	-	-	-	-	-	-	53	53	-
t _{PLH}	\bar{S}	Q or \bar{Q}	MAX	-	-	-	-	-	47	48	-
t _{PHL}		MAX	-	-	-	-	-	-	47	48	-
t _{PLH}	\bar{R}	Q or \bar{Q}	MAX	-	-	-	-	-	54	56	-
t _{PHL}		MAX	-	-	-	-	-	-	54	56	-

UNIT f_{max} : MHz, other : ns

MONOSTABLE MULTIVIBRATOR

- Internal Timing Resistors (2k Ω)
- Programmable Output Pulse Width with R_{ext}/C_{ext} : 40ns to 28s

FUNCTION TABLE

INPUTS			OUTPUTS	
A1	A2	B	Q	\bar{Q}
L	X	H	L	H
X	L	H	L \dagger	H \dagger
X	X	L	L \dagger	H \dagger
H	H	X	L \dagger	H \dagger
H	L	H		
\downarrow	H	H		
\downarrow	\downarrow	H		
L	X	\uparrow		
X	L	\uparrow		

See explanation of function table on page

\dagger These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

RECOMMENDED OPERATING CONDITIONS

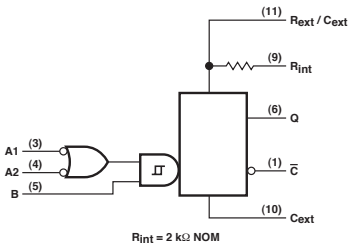
PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	40	mA
I_{OH}	MAX	-0.4	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_w (IN)			MIN	50
t_{PLH}	A	Q	MAX	70
t_{PHL}	B			80
t_{PLH}	A	\bar{Q}	MAX	55
t_{PHL}	B			65

UNIT: NS

Logic Diagram

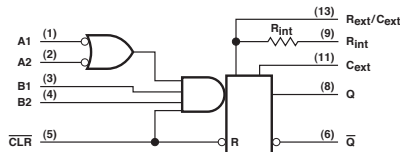


- NOTES: 1. An external capacitor may be connected between C_{ext} (positive) and R_{ext}/C_{ext} .
 2. To use the internal timing resistor, connect R_{int} to V_{CC} . For improved pulse width accuracy and repeatability, connect an external resistor between R_{ext}/C_{ext} and V_{CC} with R_{int} open-circuited.

RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

- Retriggerable for Very Long Output Pulse, Up to 100% Duty Cycle
- Internal Timing Resistors (5kΩ)

Logic Diagram



R_{int} is nominally 10 kΩ for '122 and 'LS122

FUNCTION TABLE

CLEAR	INPUTS				OUTPUTS	
	A1	A2	B	B2	Q	\bar{Q}
L	X	X	X	X	L	H
X	H	H	X	X	L†	H†
X	X	X	L	X	L†	H†
X	X	X	X	L	L†	H†
H	L	X	↑	H		
H	L	X	H	↑		
H	X	L	H	↑		
H	H	↓	H	H		
H	↓	↓	H	H		
H	↓	H	H	H		
↑	L	X	H	H		
↑	X	L	H	H		

See explanation of function table on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	66	11	mA
I_{OH}	MAX	-0.8	-0.4	mA
I_{OL}	MAX	16	8	mA

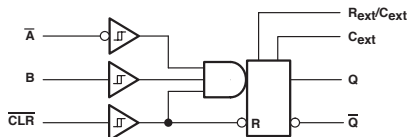
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
t_w			MIN	40	40
t_{PLH}	A	Q	MAX	33	33
	B			28	44
t_{PHL}	A	\bar{Q}	MAX	40	45
	B			36	56
t_{PLH}	CLEAR	Q	MAX	27	27
		\bar{Q}		40	45

UNIT: NS

DUAL RETRIGGERABLE MONOSTABLE MULTIVIBRATORS WITH CLEAR

- Retriggerable for Very Long Output Pulse, Up to 100% Duty Cycle



FUNCTION TABLE

CLEAR	INPUTS		OUTPUTS	
	\bar{A} (A)	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	†	$\text{—}\downarrow\text{—}$	$\text{—}\uparrow\text{—}$
H	†	H	$\text{—}\downarrow\text{—}$	$\text{—}\uparrow\text{—}$
†	L	H	$\text{—}\downarrow\text{—}$	$\text{—}\uparrow\text{—}$

See explanation of function table on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	66	20	0.16	0.16	0.65	0.975	0.28	0.65	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-8	-8	-6	-12	mA
I_{OL}	MAX	16	8	4	4	8	8	6	12	mA

SWITCHING CHARACTERISTICS

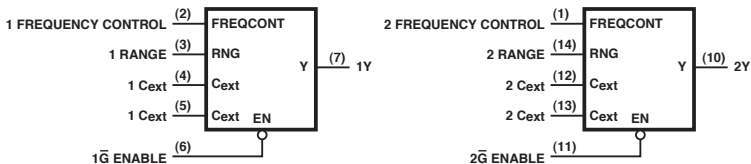
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V
t_W			MIN	40	40	30	30	5	5	5	5
t_{PLH}	\bar{A} (A)	Q	MAX	33	33	90	-	16	12	27.5	16
	B			28	44	90	-	16	12	27.5	16
t_{PHL}	\bar{A} (A)	\bar{Q}	MAX	40	45	96	-	16	12	27.5	16
	B			36	56	96	-	16	12	27.5	16
t_{PLH}	CLEAR (R)	Q	MAX	27	27	65	-	13	14	22	13
		\bar{Q}		40	45	65	-	13	14	22	13

UNIT: NS

DUAL VOLTAGE-CONTROLLED OSCILLATORS WITH ENABLE INPUTS

- Frequency Spectrum: 1Hz to 60MHz
- Typical f_{max} : 85MHz
- Typical Power Dissipation: 525mW

Block Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	S	UNIT
I_{CC}	MAX	150	mA
I_{OH}	MAX	-1	mA
I_{OL}	MAX	20	mA

SWITCHING CHARACTERISTICS

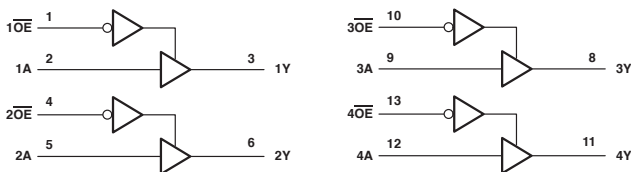
PARAMETER	MAX or MIN	S
t_o	MIN	60

UNIT: NS

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

● Y = A

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	UNIT
I _{CC}	MAX	54	20	40	0.08	0.16	0.08	0.16	49	49	30	mA
I _{OH}	MAX	-5.2	-2.6	-15	-6	-6	-6	-6	-15	-15	-32	mA
I _{OL}	MAX	16	24	64	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	LVTH 3V	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC	UNIT
I _{CC}	MAX	7	0.04	0.02	0.02	0.02	0.01	0.01	mA
I _{OH}	MAX	-32	-8	-8	-8	-16	-24	-24	mA
I _{OL}	MAX	64	8	8	8	16	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT
t _{PLH}	A	Y	MAX	13	15	6.5	30	30	33	38	5.7	6	4.9
t _{PHL}			MAX	18	18	8	30	30	33	38	7.7	8	4.9
t _{PZH}	\bar{G}	Y	MAX	17	20	8.5	30	38	35	38	10.3	11.1	5.9
t _{PZL}			MAX	25	25	9	30	38	35	38	11.7	12.8	6.8
t _{PHZ}			MAX	8	20	6	30	38	33	42	8.9	9.4	6.2
t _{PLZ}			MAX	12	20	6	30	38	33	42	8.6	9.9	6.2

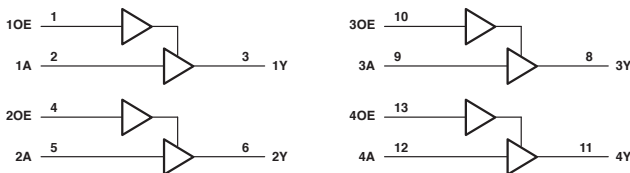
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC
t _{PLH}	A	Y	MAX	3.5	8.5	8.5	13	8.5	4.8	2.8
t _{PHL}			MAX	3.9	8.5	8.5	13	8.5	4.8	2.8
t _{PZH}	\bar{G}	Y	MAX	4	8	8	13	8	5.4	3.5
t _{PZL}			MAX	4	8	8	13	8	5.4	3.5
t _{PHZ}			MAX	4.5	10	10	15	10	4.6	4
t _{PLZ}			MAX	4.5	10	10	15	10	4.6	4

UNIT: NS

QUADRUPLE BUS BUFFER GATES WITH THREE-STATE OUTPUTS

● Y = A

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	SN64 BCT	ABT	LVTH 3V	UNIT
I _{CC}	MAX	62	22	48	0.08	0.16	0.16	51	51	30	7	mA
I _{OH}	MAX	-5.2	-2.6	-15	-6	-6	-6	-15	-15	-32	-32	mA
I _{OL}	MAX	16	24	64	6	6	6	64	64	64	64	mA

PARAMETER	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVC	UNIT
I _{CC}	MAX	0.04	0.02	0.02	0.02	0.01	0.01	mA
I _{OH}	MAX	-8	-8	-8	-16	-24	-24	mA
I _{OL}	MAX	8	8	8	16	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	SN64 BCT	ABT	LVTH 3V
t _{PLH}	A	Y	MAX	13	15	7	30	30	36	6.3	6.3	6.3	3.8
			MAX	18	18	8.5	30	30	36	7.4	7.4	5.7	3.9
t _{PZH}	G	Y	MAX	18	25	8.5	30	38	38	7.9	7.9	6.5	5.4
			MAX	25	35	8.5	30	38	38	10.5	10.5	6.5	5.2
t _{PHZ}	G	Y	MAX	16	25	7.5	30	38	42	10	10	6.8	3.8
			MAX	18	25	8	30	38	42	12.3	12.3	6.7	5.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LV 5V	LV 3V	LVC 3V	ALVC
t _{PLH}	A	Y	MAX	8.5	8.5	8.5	13	4.7	3.1
			MAX	8.5	8.5	8.5	13	4.7	3.1
t _{PZH}	G	Y	MAX	8	8	8	13	5.7	3.3
			MAX	8	8	8	13	5.7	3.3
t _{PHZ}	G	Y	MAX	10	10	10	15	6	3.7
			MAX	10	10	10	15	6	3.7

UNIT: ns

50-Ω LINE DRIVERS

$$\bullet Y = \overline{A + B}$$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	57	mA
I_{OH}	MAX	-42.4	mA
I_{OL}	MAX	48	mA

SWITCHING CHARACTERISTICS

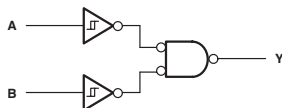
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	A, B	Y	MAX	9
t_{PHL}	A, B	Y	MAX	12

UNIT: ns

QUADRUPLE 2-INPUT POSITIVE-NAND SCHMITT TRIGGERS

$$\bullet Y = \overline{A \cdot B}$$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	40	14	68	0.02	0.04	0.04	0.02	0.02	0.02	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-1	-4	-4	-4	-8	-8	-6	-12	mA
I_{OL}	MAX	16	8	20	4	4	4	8	8	6	12	mA

SWITCHING CHARACTERISTICS

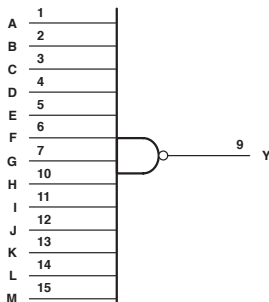
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V
t_{PLH}	A, B	Y	MAX	22	22	10.5	31	38	50	11	10	17.5	11
t_{PHL}	A, B	Y	MAX	22	22	13	31	38	50	11	8	17.5	11

UNIT: ns

13-INPUT POSITIVE-NAND GATES

$$Y = \overline{A \cdot B \cdot C \cdot D \cdot E \cdot F \cdot G \cdot H \cdot I \cdot J \cdot K \cdot L \cdot M}$$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	S	ALS	SN74 HC	UNIT
I_{CC}	MAX	10	0.34	0.02	mA
I_{OH}	MAX	-1	-0.4	-4	mA
I_{OL}	MAX	20	8	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S	ALS	SN74 HC
t_{PLH}	A to M	Y	MAX	6	11	38
t_{PHL}	A to M	Y	MAX	7	25	38

UNIT: ns

136

QUAD EXCLUSIVE-OR GATES WITH OPEN-COLLECTOR OUTPUTS

$$Y = A \oplus B = \overline{A}B + A\overline{B}$$

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

RECOMMENDED OPERATING CONDITIONS

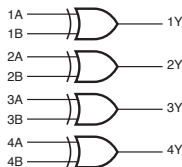
PARAMETER	MAX or MIN	TTL	LS	ALS	AS	UNIT
I_{CC}	MAX	50	10	5.9	31	mA
V_{OH}	MAX	5.5	5.5	5.5	5.5	V
I_{OL}	MAX	16	8	8	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS
t_{PLH}	A or B	Y (Other Output = L)	MAX	18	30	50	12.5
t_{PHL}	A or B	Y (Other Output = L)	MAX	50	30	15	7.1
t_{PLH}	A or B	Y (Other Output = L)	MAX	22	30	50	11.4
t_{PHL}	A or B	Y (Other Output = L)	MAX	55	30	15	10.7

UNIT: ns

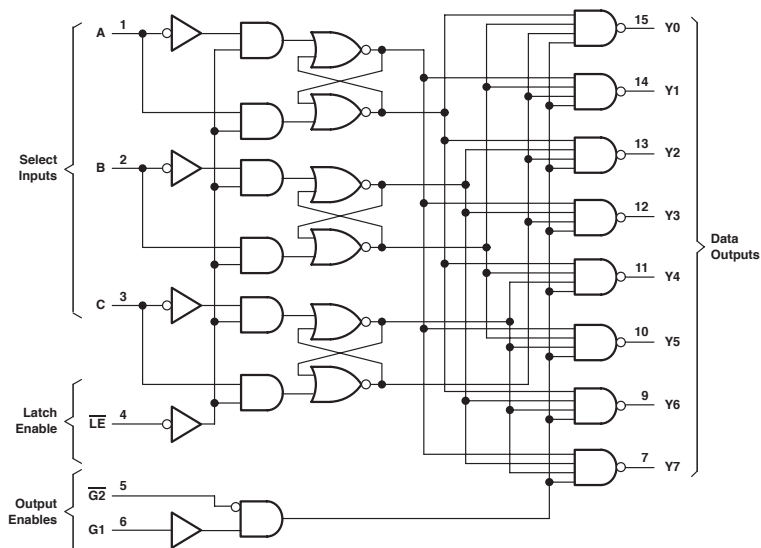
Logic Diagram



3-TO-8 LINE DECODERS/DEMULTIPLEXERS WITH ADDRESS LATCHES

- Incorporates Two Output Enables To Simplify Cascading

Logic Diagram



FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			SELECT			Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
LE	G1	G2	C	B	A								
X	X	H	X	X	X	H	H	H	H	H	H	H	
X	L	X	X	X	X	H	H	H	H	H	H	H	
L	H	L	L	L	L	L	H	H	H	H	H	H	
L	H	L	L	L	H	H	L	H	H	H	H	H	
L	H	L	L	H	L	H	H	L	H	H	H	H	
L	H	L	L	H	H	H	H	H	L	H	H	H	
L	H	L	H	L	H	H	H	H	H	L	H	H	
L	H	L	H	H	L	H	H	H	H	H	L	H	
L	H	L	H	H	H	H	H	H	H	H	H	L	
H	H	L	X	X	X	Depends upon the address previously applied while LE was at a logic low.							

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	UNIT
I _{CC}	MAX	18	11	24	0.08	0.16	0.08	0.16	mA
I _{OH}	MAX	-0.4	-0.4	-2	-4	-4	-4	-4	mA
I _{OL}	MAX	8	8	20	4	4	4	4	mA

SWITCHING CHARACTERISTICS

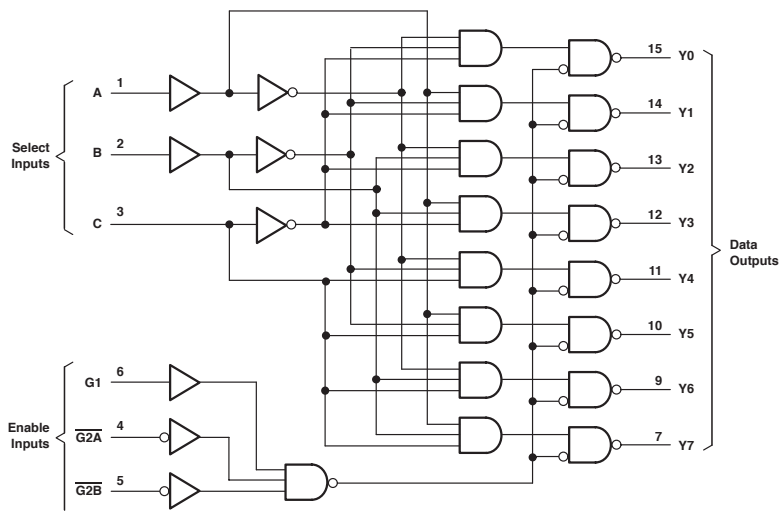
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
t _{PLH}	A, B, C	Y (CD74: \bar{Y})	MAX	24	20	12.5	48	54	48	57
t _{PHL}			MAX	38	20	12.5	48	54	48	57
t _{PLH}	$\bar{G2}$	Y (CD74: \bar{Y})	MAX	21	12	8	36	44	36	56
t _{PHL}			MAX	27	15	8.5	36	44	36	56
t _{PLH}	G1	Y (CD74: \bar{Y})	MAX	21	17	10	36	44	36	53
t _{PHL}			MAX	27	15	9	36	44	36	53
t _{PLH}	\bar{LE} (CD74: LE)	Y (CD74: \bar{Y})	MAX	27	22	13.5	48	57	52	66
t _{PHL}			MAX	38	20	14	48	57	52	66

UNIT:ns

3-TO-8 LINE DECODERS/DEMULTIPLEXRS

- 3 Enable Inputs to Simplify Cascading and /or Data Reception
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUTS										
ENABLE	SELECT											
G1	G2*	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	H	X	X	X	H	H	H	H	H	H	H	H
L	X	X	X	X	H	H	H	H	H	H	H	H
H	L	L	L	L	L	H	H	H	H	H	H	H
H	L	L	L	H	H	L	H	H	H	H	H	H
H	L	L	H	L	H	H	L	H	H	H	H	H
H	L	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	L	H	H	H	L	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	H	L	H	H
H	L	H	L	H	H	H	H	H	H	H	L	H
H	L	H	L	H	H	H	H	H	H	H	H	L

G2* = G2A-G2B

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	UNIT
I _{CC}	MAX	10	74	10	20	20	0.08	0.16	0.08	0.16	0.04	mA
I _{OH}	MAX	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-4	-24	mA
I _{OL}	MAX	8	20	8	20	20	4	4	4	4	24	mA

PARAMETER	MAX or MIN	CD74 AC	ACT 11	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I _{CC}	MAX	0.16	0.04	0.16	0.04	0.04	0.02	0.02	0.01	mA
I _{OH}	MAX	-24	-24	-24	-8	-8	-6	-12	-24	mA
I _{OL}	MAX	24	24	24	8	8	6	12	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11
t _{PLH}	A, B, C	Y (CD74:Y)	MAX	27	12	22	10	8.5	45	45	45	53	8.1
t _{PHL}			MAX	39	12	18	9.5	9	45	45	45	53	8.8
t _{PLH}	G2	Y (CD74:Y)	MAX	26	11	17	7.5	8	39	53	42	53	8.3
t _{PHL}			MAX	38	11	17	8.5	7.5	39	53	42	53	8.3
t _{PLH}	G1	Y (CD74:Y)	MAX	26	11	17	10	9	39	53	42	53	7.5
t _{PHL}			MAX	38	11	17	10	8.5	39	53	42	53	7.7

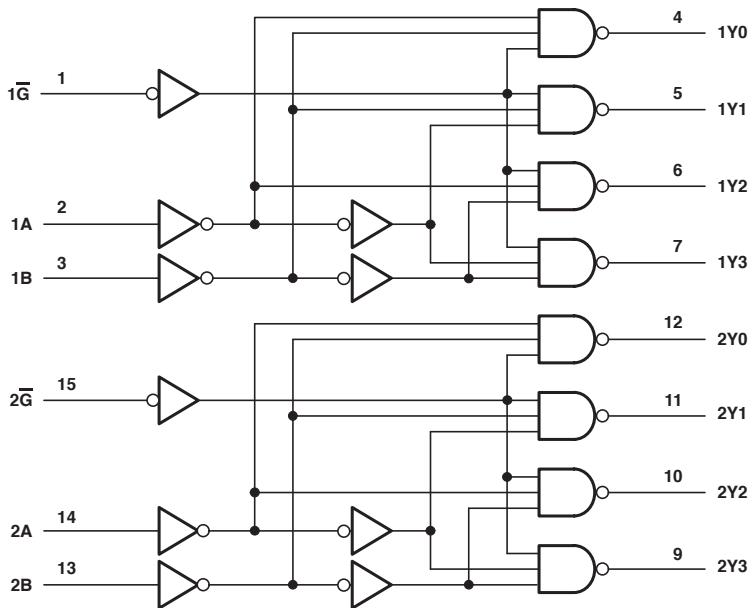
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	ACT 11	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t _{PLH}	A, B, C	Y (CD74:Y)	MAX	11	9.8	12	11.5	13	18	11.5	6.7
t _{PHL}			MAX	11	9.7	12	11.5	13	18	11.5	6.7
t _{PLH}	G2	Y (CD74:Y)	MAX	10	8.9	10.5	11.5	12	18	11.5	6.5
t _{PHL}			MAX	10	8.9	10.5	11.5	12	18	11.5	6.5
t _{PLH}	G1	Y (CD74:Y)	MAX	11	9.3	11	11.5	11.5	18.5	11.5	5.8
t _{PHL}			MAX	11	9.8	11	11.5	11.5	18.5	11.5	5.8

UNIT: ns

DUAL 2-TO-4-LINE DECODERS/DEMULTIPLEXERS

- Incorporate Two Enable Inputs to Simplify Cascading and /or Data Reception
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS				
ENABLE	SELECT						
G	B	A	Y0	Y1	Y2	Y3	
H	X	X	H	H	H	H	
L	L	L	L	H	H	H	
L	L	H	H	L	H	H	
L	H	L	H	H	L	H	
L	H	H	H	H	H	L	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	CD74 AC	ACT 11	CD74 ACT	UNIT
I _{CC}	MAX	11	90	13	0.08	0.08	0.08	0.16	0.16	0.08	0.16	mA
I _{DH}	MAX	-0.4	-1	-0.4	-4	-4	-4	-4	-24	-24	-24	mA
I _{OL}	MAX	8	20	8	4	4	4	4	24	24	24	mA

PARAMETER	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I _{CC}	MAX	0.04	0.02	-	0.02	0.01	mA
I _{DH}	MAX	-8	-8	-6	-12	-24	mA
I _{OL}	MAX	8	8	6	12	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	CD74 AC	ACT 11	CD74 ACT
t _{PLH}	A or B	Y (CD74: \bar{Y})	MAX	29	12	14	44	44	43	51	10.5	8.5	11.5
t _{PHL}	A or B	Y (CD74: \bar{Y})	MAX	38	12	14	44	44	43	51	10.5	8.5	11.5
t _{PLH}	G	Y (CD74: \bar{Y})	MAX	24	8	14	44	41	43	51	10.5	7.9	12
t _{PHL}	G	Y (CD74: \bar{Y})	MAX	32	10	15	44	41	43	51	10.5	7.5	12

PARAMETER	INPUT	OUTPUT	MAX or MIN	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t _{PLH}	A or B	Y (CD74: \bar{Y})	MAX	10.5	10.5	16.5	10.5	6.2
t _{PHL}	A or B	Y (CD74: \bar{Y})	MAX	10.5	10.5	16.5	10.5	6.2
t _{PLH}	G	Y (CD74: \bar{Y})	MAX	9.5	9.5	14.5	9.5	4.7
t _{PHL}	G	Y (CD74: \bar{Y})	MAX	9.5	9.5	14.5	9.5	4.7

UNIT: ns

DUAL 4-INPUT POSITIVE-NAND 50-Ω LINE DRIVERS

$$\bullet Y = \overline{ABCD}$$

RECOMMENDED OPERATING CONDITIONS

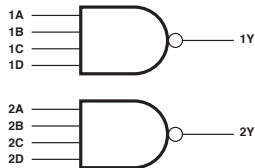
PARAMETER	MAX or MIN	S	UNIT
I_{CC}	MAX	44	mA
I_{OH}	MAX	-40	mA
I_{OL}	MAX	60	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S
t_{PLH}	A, B, C, D	Y	MAX	6.5
t_{PHL}			MAX	6.5

UNIT: ns

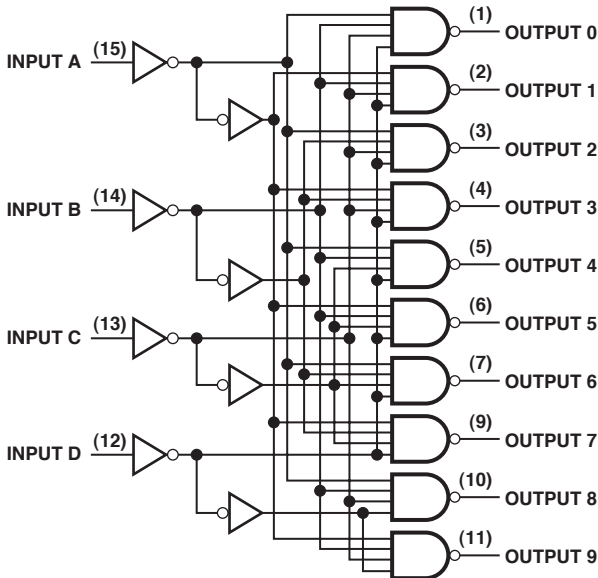
Logic Diagram



BCD-TO-DECIMAL DECODERS/DRIVERS FOR LAMPS, RELAYS, MOS

- Sink-Current Capability: 80mA
- Low Power Dissipation (SN74LS): 35mW (typ)

Logic Diagram



FUNCTION TABLE

No.	INPUTS				OUTPUTS										
	D	C	B	A	0	1	2	3	4	5	6	7	8	9	
0	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H
1	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H
2	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H
3	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H
4	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H
5	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H
6	L	H	H	L	H	H	H	H	H	L	H	H	H	H	H
7	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H
8	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H
9	H	L	L	H	H	H	H	H	H	H	H	H	H	L	L
INVALID	H	L	H	L	H	H	H	H	H	H	H	H	H	H	H
	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	L	H	H	H	H	H	H	H	H	H	H	H
	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

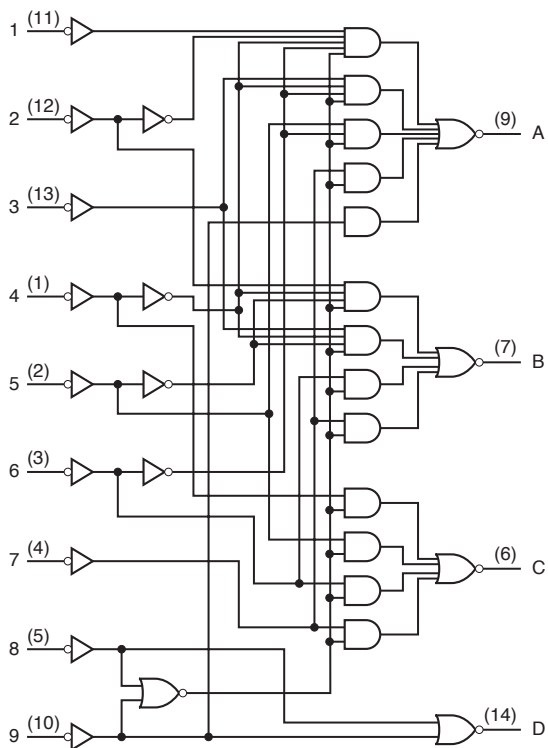
PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	70	13	mA
V_O (OFF)	MAX	15	15	mA

SWITCHING CHARACTERISTICS

PARAMETER	MAX or MIN	TTL	LS
t_{PLH}	MAX	50	50
t_{PHL}	MAX	50	50

UNIT: ns

Logic Diagram



FUNCTION TABLE

INPUTS									OUTPUTS			
1	2	3	4	5	6	7	8	9	D	C	B	A
H	H	H	H	H	H	H	H	H	H	H	H	H
X	X	X	X	X	X	X	X	L	L	H	H	L
X	X	X	X	X	X	X	L	H	L	H	H	H
X	X	X	X	X	L	H	H	H	H	L	L	L
X	X	X	X	L	H	H	H	H	H	L	H	L
X	X	X	L	H	H	H	H	H	H	L	H	H
X	X	L	H	H	H	H	H	H	H	H	L	L
X	L	H	H	H	H	H	H	H	H	H	L	H
L	H	H	H	H	H	H	H	H	H	H	H	L

RECOMMENDED OPERATING CONDITIONS

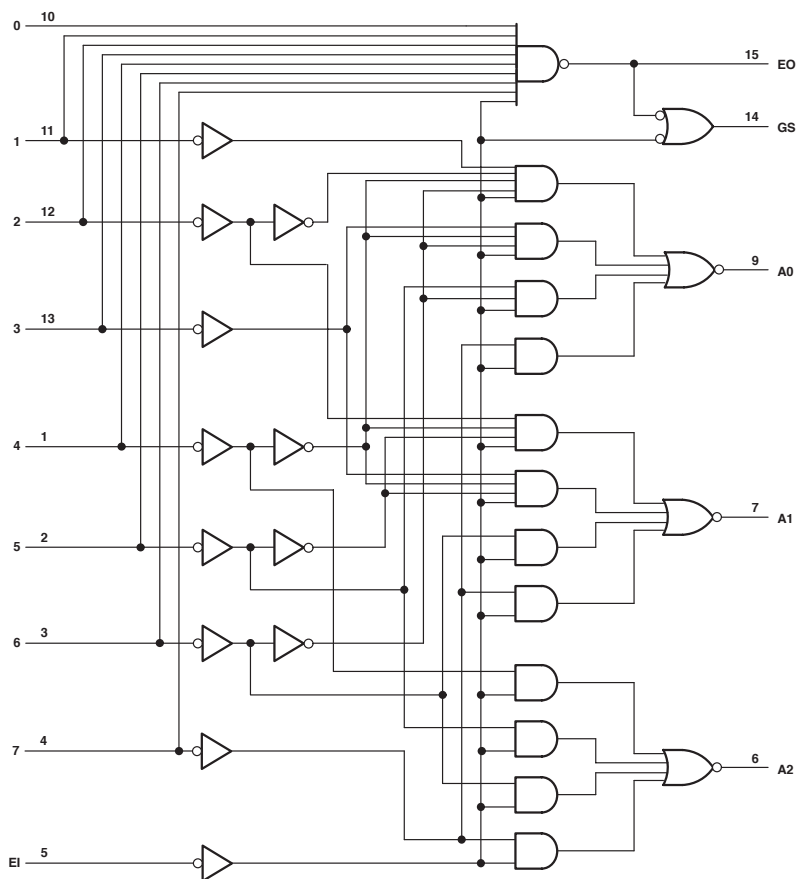
PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	70	20	0.08	0.16	0.16	mA
I_{OH}	MAX	-0.8	-0.4	-4	-4	-4	mA
I_{OL}	MAX	16	8	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	MAX	19	33	48	48	53
t_{PHL}	MAX	19	23	48	48	53

UNIT:ns

Logic Diagram



FUNCTION TABLE

INPUTS									OUTPUTS				
EI	0	1	2	3	4	5	6	7	A2	A1	A0	GS	EO
H	X	X	X	X	X	X	X	X	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	X	X	X	X	X	X	X	L	L	L	L	L	H
L	X	X	X	X	X	X	L	H	L	L	H	L	H
L	X	X	X	X	X	L	H	H	L	H	L	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	H	L	H
L	X	L	H	H	H	H	H	H	H	H	L	L	H
L	L	H	H	H	H	H	H	H	H	H	L	L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	UNIT
I _{CC}	MAX	60	20	0.08	mA
I _{OL}	MAX	16	8	4	mA
I _{OH}	MAX	-0.8	-0.4	-4	mA

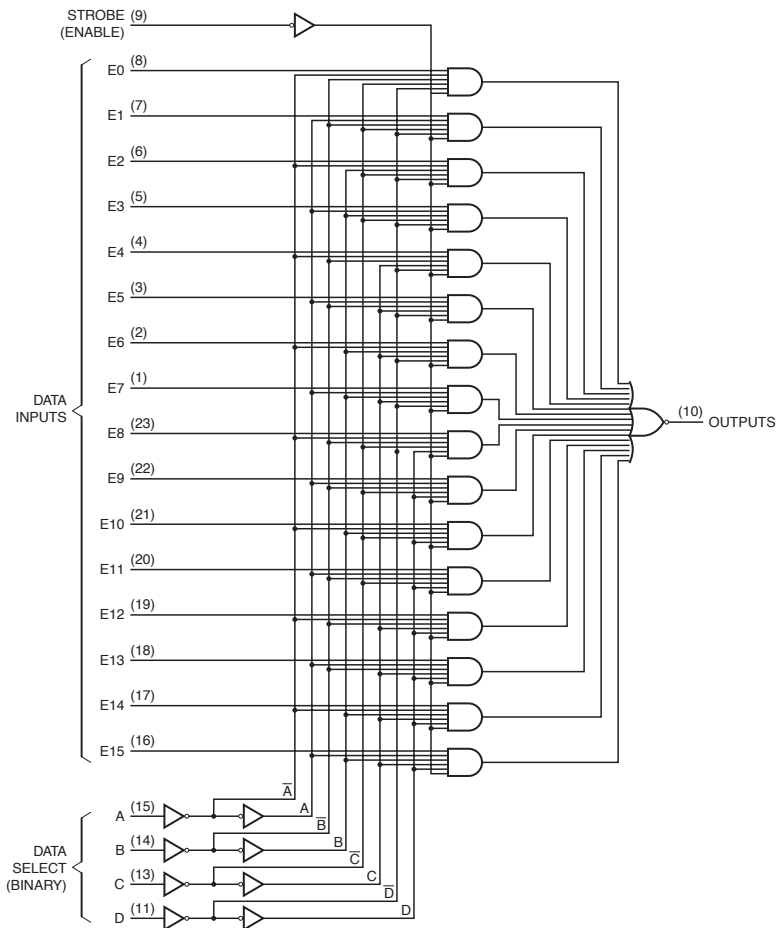
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	WAVEFORM	MAX or MIN	TTL	LS	SN74 HC
t _{PLH}	1 to 7	A0, A1 or A2	In-phase output	MAX	15	18	45
					14	25	45
t _{PHL}	1 to 7	A0, A1 or A2	Out-of-phase output	MAX	19	36	45
					19	29	45
t _{PLH}	0 to 7	E0	Out-of-phase output	MAX	10	18	38
					25	40	38
t _{PHL}	0 to 7	GS	In-phase output	MAX	30	55	48
					25	21	48
t _{PLH}	E1	A0, A1 or A2	In-phase output	MAX	15	25	49
					15	25	49
t _{PHL}	E1	GS	In-phase output	MAX	12	17	36
					15	36	36
t _{PLH}	E1	E0	In-phase output	MAX	15	21	41
					30	35	41

UNIT: ns

1-OF-16 DATA SELECTOR

Logic Diagram



FUNCTION TABLE

INPUTS					STROBE G	OUTPUT W
SELECT						
D	C	B	A	G		
X	X	X	X		H	
L	L	L	L		E0	
L	L	L	H		E1	
L	L	H	L		E2	
L	L	H	H		E3	
L	H	L	L		E4	
L	H	L	H		E5	
L	H	H	L		E6	
L	H	H	H		E7	
H	L	L	L		E8	
H	L	L	H		E9	
H	L	H	L		E10	
H	L	H	H		E11	
H	H	L	L		E12	
H	H	L	H		E13	
H	H	H	L		E14	
H	H	H	H		E15	

NOTES:

H = High Level, L = Low Level, X = irrelevant
 E0, E1 ... E15 = the complement of the level of the
 respective E input
 D0, D1 ... D7 = the level of the D respective input

RECOMMENDED OPERATING CONDITIONS

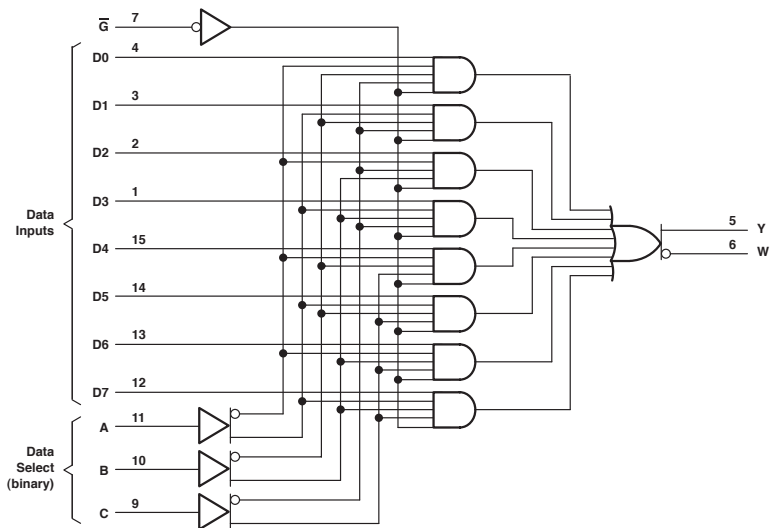
PARAMETER	MAX or MIN	TTL	UNIT
I _{CC}	MAX	48	mA
I _{DH}	MAX	-0.8	mA
I _{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t _{PLH}	A, B, C or D	W	MAX	35
t _{PHL}				33
t _{PLH}	Strobe \bar{G}	W	MAX	24
t _{PHL}				30
t _{PLH}	E0 thru E15 or E0 thru D7	W	MAX	14
t _{PHL}				20

UNIT:ns

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUTS		
SELECT				G	Y	W
C	B	A				
X	X	X	H	L	H	
L	L	L	L	D0	D0	
L	L	H	L	D1	D1	
L	H	L	L	D2	D2	
L	H	H	L	D3	D3	
H	L	L	L	D4	D4	
H	L	H	L	D5	D5	
H	H	L	L	D6	D6	
H	H	H	L	D7	D7	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I _{CC}	MAX	48	10	70	12	30	21	0.08	0.16	0.16	0.16	0.16	mA
I _{OH}	MAX	-0.8	-0.4	-1	-2.6	-15	-1	-6	-4	-4	-24	-24	mA
I _{OL}	MAX	16	8	20	24	48	24	6	4	4	24	24	mA

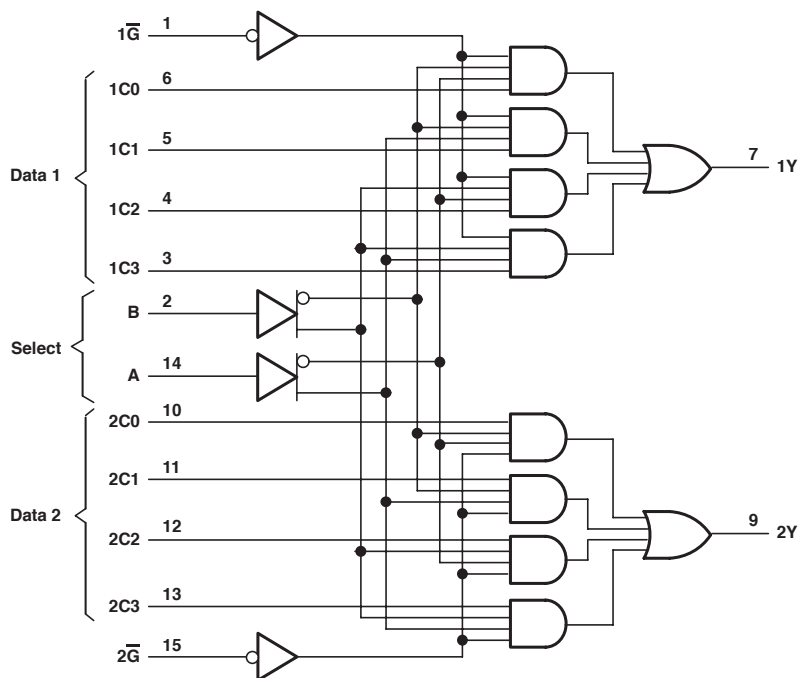
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
t _{PLH}	A, B or C	Y	MAX	38	43	18	18	14.5	12	63	56	62
t _{PHL}				38	30	18	24	15	9	63	56	62
t _{PLH}	A, B or C	W (CD74: \bar{Y})	MAX	26	23	15	24	12	9.5	63	62	65
t _{PHL}				30	32	13.5	23	12	7.5	63	62	65
t _{PLH}	D0 to D7	Y	MAX	20	32	16.5	10	10.5	7.5	49	51	57
t _{PHL}				27	26	18	15	11	7.5	49	51	57
t _{PLH}	D0 to D7	W (CD74: \bar{Y})	MAX	14	21	13	15	6.5	7	49	56	54
t _{PHL}				14	20	12	15	4.5	5	49	56	54
t _{PLH}	\bar{G}	Y	MAX	33	42	12	18	14	10.5	32	42	44
t _{PHL}				33	32	12	19	11	7.5	32	42	44
t _{PLH}	\bar{G}	W (CD74: \bar{Y})	MAX	21	24	7	19	6	7	32	44	54
t _{PHL}				23	30	7	23	10	6	32	44	54

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT
t _{PLH}	A, B or C	Y	MAX	18.2	20.2
t _{PHL}				18.2	20.2
t _{PLH}	A, B or C	W (CD74: \bar{Y})	MAX	19.6	21.6
t _{PHL}				19.6	21.6
t _{PLH}	D0 to D7	Y	MAX	13.5	15.5
t _{PHL}				13.5	15.5
t _{PLH}	D0 to D7	W (CD74: \bar{Y})	MAX	14.9	16.9
t _{PHL}				14.9	16.9
t _{PLH}	\bar{G}	Y	MAX	12.2	12.1
t _{PHL}				12.2	12.1
t _{PLH}	\bar{G}	W (CD74: \bar{Y})	MAX	13.5	13.5
t _{PHL}				13.5	13.5

UNIT: ns

Logic Diagram



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				STROBE	OUTPUTS
B	A	C0	C1	C2	C3	G	Y
X	X	X	X	X	X	H	L
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I _{CC}	MAX	60	10	70	14	33	20	0.08	0.16	0.16	0.16	0.16	mA
I _{DH}	MAX	-0.8	-0.4	-1	-2.6	-15	-1	-6	-4	-4	-24	-24	mA
I _{OL}	MAX	16	8	20	24	48	20	6	4	4	24	24	mA

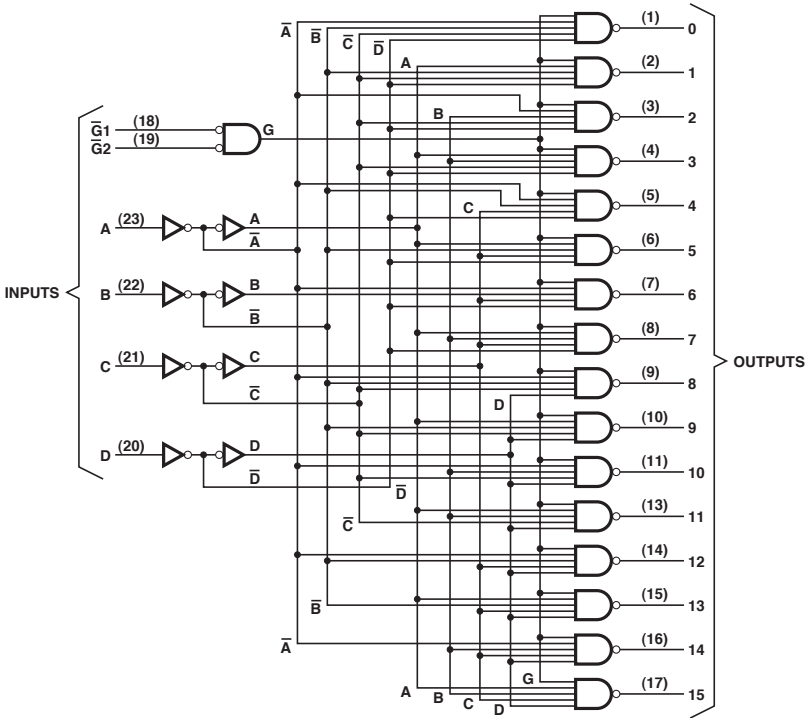
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
t _{PLH}	DATA	Y	MAX	18	15	9	10	7	8	35	44	51	13.3	18
t _{PHL}			MAX	23	26	9	15	8	7.5	35	44	51	13.3	18
t _{PLH}	SELECT	Y	MAX	34	29	18	21	12.5	12	38	48	51	20	22
t _{PHL}			MAX	34	38	18	21	11	10.5	38	48	51	20	22
t _{PLH}	STROBE	Y	MAX	30	24	15	18	11.5	10.5	24	36	41	11.8	12.6
t _{PHL}			MAX	23	32	13.5	18	9	8	24	36	41	11.8	12.6

UNIT: ns

4-LINE TO 16-LINE DECODER/DEMULTIPLEXER

Logic Diagram



FUNCTION TABLE

		INPUTS				OUTPUTS																
G ₁	G ₂	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
L	L	H	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	56	23	0.08	0.16	0.16	mA
I _{OH}	MAX	-0.8	24	-4	-4	-4	mA
I _{OL}	MAX	16	-0.4	4	4	4	mA

SWITCHING CHARACTERISTICS

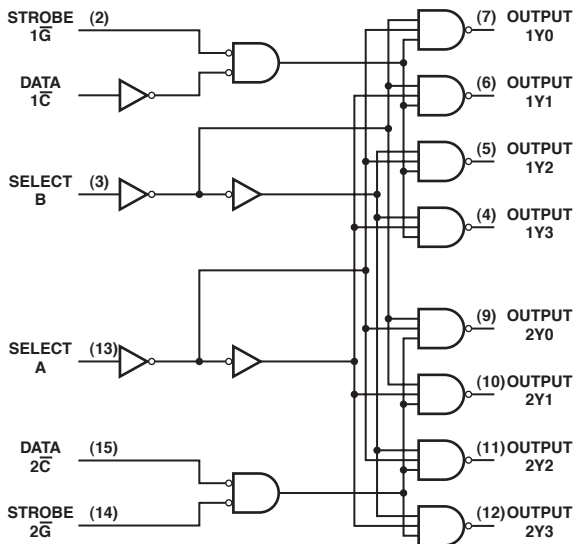
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	ALS	SN74 HC	CD74 HC	CD74 HCT
t _{PLH}	A, B, C, D	0 to 15 (CD74: Y0 to Y15)	MAX	36	12	45	53	53
t _{PHL}				33	12	45	53	53
t _{PLH}	G1 to G2	0 to 15 (CD74: Y0 to Y15)	MAX	30	12	45	53	51
t _{PHL}				27	12	45	53	51

UNIT: ns

DECODERS/DEMULPLEXERS

- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words
- Outputs: Totem Pole

Logic Diagram



FUNCTION TABLES

2-LINE TO 4-LINE DECODER OR
1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA	1Y0	1Y1	1Y2	1Y3
B	A	1G	1C				
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

2-LINE TO 4-LINE DECODER OR
1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA	2Y0	2Y1	2Y2	2Y3
B	A	2G	2C				
X	X	H	X	H	H	H	H
L	L	L	L	L	H	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE TO 8-LINE DECODER OR
1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE or DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

† C = inputs 1C and 2C connected together

‡ G = inputs 1G and 2G connected together

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	UNIT
I _{CC}	MAX	40	10	13	mA
I _{OH}	MAX	-0.8	-0.4	-0.4	mA
I _{OL}	MAX	16	8	8	mA

SWITCHING CHARACTERISTICS

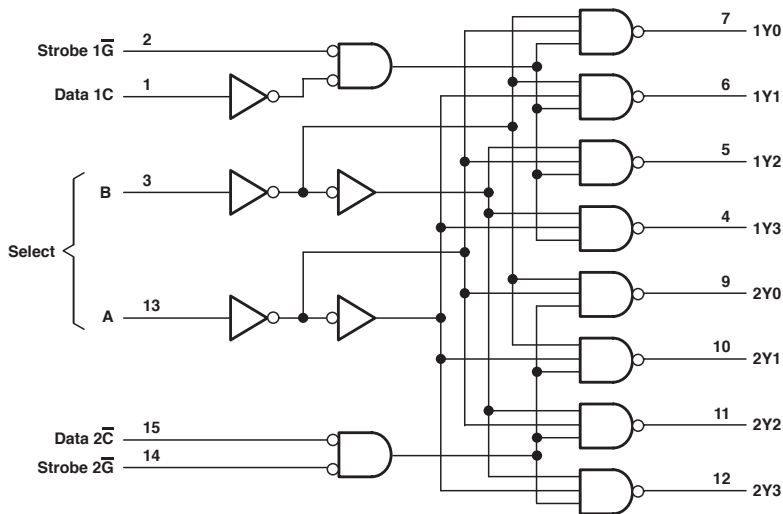
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS
t _{PLH}	A or B	Y	MAX	32	26	14
t _{PHL}	A or B			32	30	12
t _{PLH}	1C	Y	MAX	24	27	12
t _{PHL}	1C			30	27	14

UNIT: ns

DECODERS/DEMULTIPLEXERS

- Individual Strobes Simplify Cascading for Decoding or Demultiplexing Larger Words
- Outputs: Open-Collector

Logic Diagram



FUNCTION TABLES

2-LINE TO 4-LINE DECODER OR
1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA	1Y0	1Y1	1Y2	1Y3
B	A	1G	1C				
X	X	H	X	H	H	H	H
L	L	L	H	L	H	H	H
L	H	L	H	H	L	H	H
H	L	L	H	H	H	L	H
H	H	L	H	H	H	H	L
X	X	X	L	H	H	H	H

2-LINE TO 4-LINE DECODER OR
1-LINE TO 4-LINE DEMULTIPLEXER

INPUTS				OUTPUTS			
SELECT		STROBE	DATA	2Y0	2Y1	2Y2	2Y3
B	A	2G	2C				
X	X	H	X	H	H	H	H
L	L	L	L	L	L	H	H
L	H	L	L	H	L	H	H
H	L	L	L	H	H	L	H
H	H	L	L	H	H	H	L
X	X	X	H	H	H	H	H

3-LINE TO 8-LINE DECODER OR
1-LINE TO 8-LINE DEMULTIPLEXER

INPUTS				OUTPUTS							
SELECT			STROBE or DATA	(0)	(1)	(2)	(3)	(4)	(5)	(6)	(7)
C†	B	A	G‡	2Y0	2Y1	2Y2	2Y3	1Y0	1Y1	1Y2	1Y3
X	X	X	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H
L	H	H	L	H	H	H	L	H	H	H	H
H	L	L	L	H	H	H	H	L	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H
H	H	L	L	H	H	H	H	H	H	L	H
H	H	H	L	H	H	H	H	H	H	H	L

† C = inputs 1C and 2C connected together

‡ G = inputs 1G and 2G connected together

RECOMMENDED OPERATING CONDITIONS

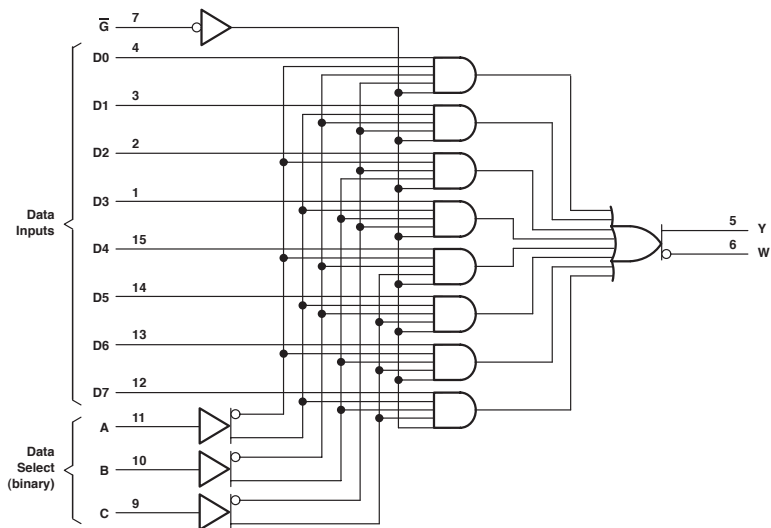
PARAMETER	MAX or MIN	TTL	LS	ALS	UNIT
I _{CC}	MAX	40	10	9	mA
I _{OL}	MAX	16	8	8	mA
V _{OH}	MAX	5.5	5.5	5.5	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS
t _{PLH}	2C 1G or 2G	Y	MAX	23	40	38
t _{PHL}				30	51	22
t _{PLH}	A or B	Y	MAX	34	46	55
t _{PHL}				34	51	25
t _{PLH}	1C	Y	MAX	27	48	50
t _{PHL}				33	48	23

UNIT: ns

Logic Diagram



FUNCTION TABLE

STROBE	INPUTS				OUTPUT
	SELECT	A	B		
H	X	X	X	X	L
L	L	L	L	X	L
L	L	H	X	L	H
L	H	X	L	L	L
L	H	X	H	X	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	UNIT
I _{CC}	MAX	48	16	78	11	28	23	0.08	0.16	0.08	0.16	mA
I _{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-6	-4	-6	-4	mA
I _{OL}	MAX	16	8	20	8	20	20	6	4	6	4	mA

PARAMETER	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I _{CC}	MAX	0.16	0.16	0.04	0.02	-	0.02	0.01	mA
I _{OH}	MAX	-24	-24	-8	-8	-6	-12	-24	mA
I _{OL}	MAX	24	24	8	8	6	12	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT
t _{PLH}	DATA	Y	MAX	14	14	7.5	14	6	6.5	32	38	35	38
				14	14	6.5	12	5.5	7	32	38	35	38
t _{PHL}	STROBE	Y	MAX	20	20	12.5	20	10.5	11	29	41	33	41
				21	21	12	13	7.5	7	29	41	33	41
t _{PLH}	SELECT	Y	MAX	23	23	15	24	11	11	31	44	40	44
				27	27	15	17	10	8	31	44	40	44

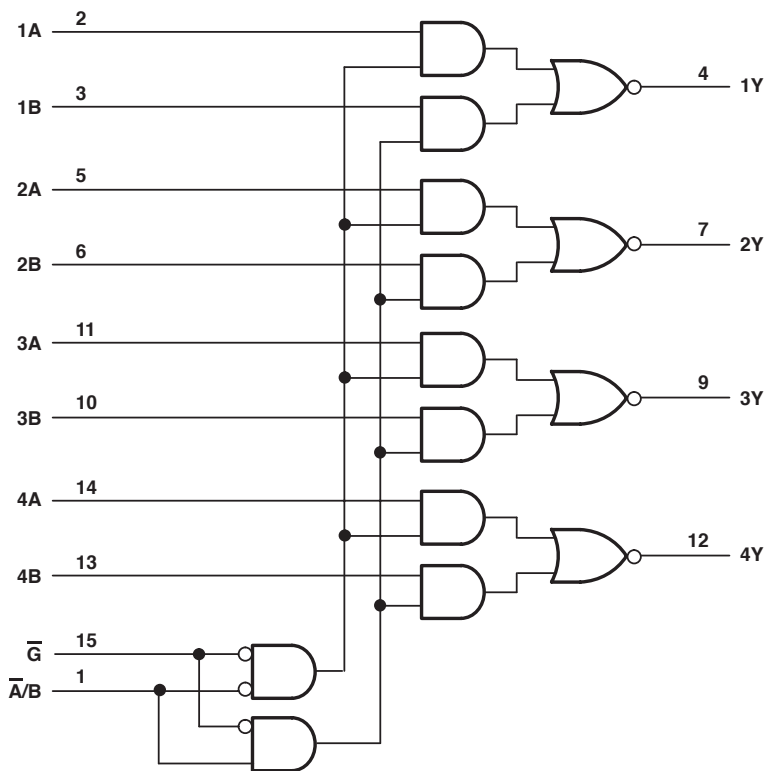
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t _{PLH}	DATA	Y	MAX	8.5	9.5	9.5	9.8	15	9.5	5.2
				8.5	9.5	9.5	9.8	15	9.5	5.2
t _{PHL}	STROBE	Y	MAX	13.5	13.5	12	12	19.5	12	6.5
				13.5	13.5	12	12	19.5	12	6.5
t _{PLH}	SELECT	Y	MAX	14.5	14.5	11.5	12	19	11.5	6.8
				14.5	14.5	11.5	12	19	11.5	6.8

UNIT: ns

QUAD 2-TO-1 LINE DATA SELECTORS/MULTIPLEXERS

- Buffered Inputs and Outputs

Logic Diagram



FUNCTION TABLE

STROBE	INPUTS				OUTPUT
	SELECT	A	B		
H	X	X	X	X	H
L	L	L	L	X	H
L	L	H	X	L	L
L	H	X	L	L	H
L	H	X	H	L	L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	11	81	10	22.5	15	0.08	0.16	0.16	mA
I _{OH}	MAX	-0.4	-1	-0.4	-2	-1	-6	-4	-4	mA
I _{OL}	MAX	8	20	8	20	20	6	4	4	mA

PARAMETER	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT	UNIT
I _{CC}	MAX	0.16	0.16	0.04	0.02	mA
I _{OH}	MAX	-24	-24	-8	-8	mA
I _{OL}	MAX	24	24	8	8	mA

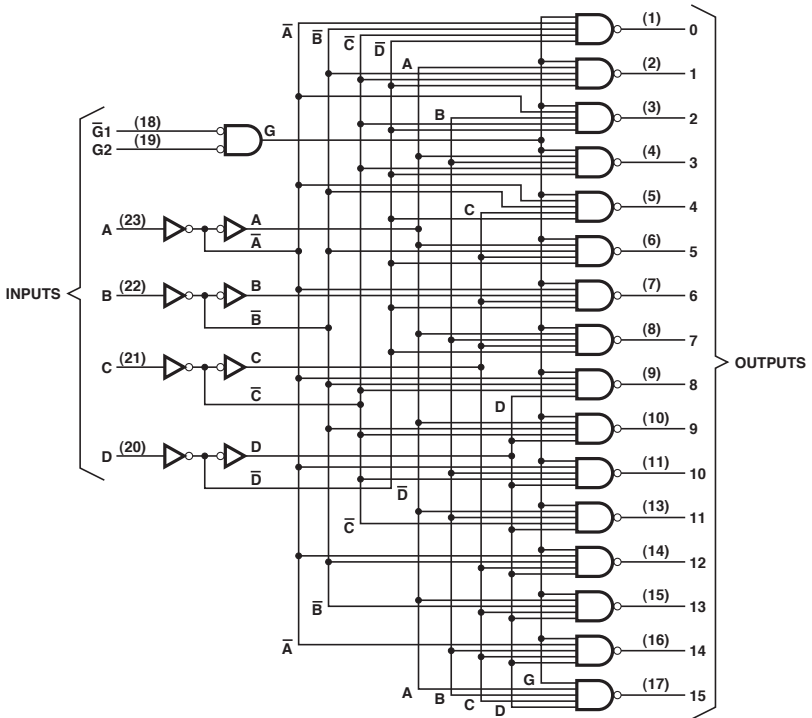
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
t _{PLH}	DATA	Y	MAX	12	6	15	5	7	32	42	42
				15	6	8	4.5	4.5	32	42	42
t _{PHL}	STROBE	Y	MAX	17	11.5	18	6.5	7	29	48	48
				24	12	18	10	6.5	29	48	48
t _{PLH}	SELECT	Y	MAX	20	12	18	9.5	9.5	31	45	45
				24	12	18	10.5	7	31	45	45

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT
t _{PLH}	DATA	Y	MAX	8	9.2	9.5	9.8
				8	9.2	9.5	9.8
t _{PHL}	STROBE	Y	MAX	11.9	12.4	12	12
				11.9	12.4	12	12
t _{PLH}	SELECT	Y	MAX	12.9	13.5	11.5	12
				12.9	13.5	11.5	12

UNIT: ns

Logic Diagram



FUNCTION TABLE

		INPUTS				OUTPUTS																
$\overline{G1}$	$\overline{G2}$	D	C	B	A	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	L	H	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	H	L	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H	H
L	L	L	H	L	L	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H	H
L	L	H	L	L	L	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H	H
L	L	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	L	H	L	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H	H
L	L	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	H	H	H
L	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	L	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	X	X	X	X	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	56	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

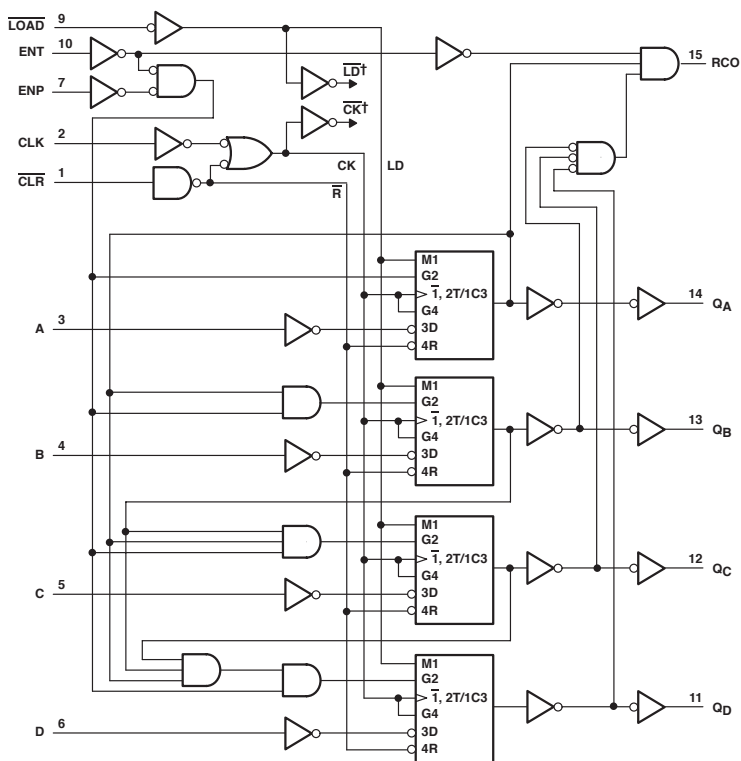
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	INPUT	ANY	MAX	36
t_{PHL}				36
t_{PLH}	STROBE	ANY	MAX	25
t_{PHL}				36

UNIT: ns

SYNCHRONOUS 4-BIT BINARY COUNTERS

- Asynchronous Clear Function
- Carry Output for n-Bit Cascading

Logic Diagram



† For simplicity, routing of complementary signals \overline{LD} and \overline{CK} is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
I _{CC}	MAX	101	32	21	53	55	0.08	0.16	0.16	0.08	0.08	-	0.02	mA
I _{OH}	MAX	-0.8	-0.4	-0.4	-2	-1	4	-4	-4	-24	-24	-6	-12	mA
I _{OL}	MAX	16	8	8	20	20	-4	4	4	24	24	-6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
f _{max}			MIN	25	25	40	75	90	25	20	20
t _w	CLOCK		MIN	25	25	-	-	7	20	24	24
	CLEAR			20	20	15	8	5	20	30	30
t _{su}	INPUT A, B, C, D		MIN	20	20	15	8	5	38	18	15
	ENABLE, P, T			20	20	15	8	11.5	43	15	20
	LOAD			25	20	15	8	11.5	34	18	18
	CLEAR INACTIVE			20	25	10	8	-	31	20	-
t _h			MIN	0	3	0	0	2	0	3	5
I _{PLH}	CLOCK	RIPPLE CARRY	MAX	35	35	20	16.5	15	54	56	63
I _{PHL}				35	35	20	12.5	15	54	56	63
I _{PLH}	CLOCK	ANY Q	MAX	25	24	15	7	9.5	51	56	59
I _{PHL}				29	27	20	13	11	51	56	59
I _{PLH}	ENABLE T	RIPPLE CARRY	MAX	16	14	13	9	8.5	49	36	48
I _{PHL}				16	14	13	8.5	8.5	49	36	48
I _{PHL}	CLEAR	ANY Q	MAX	38	28	24	13	13	53	63	75
I _{PHL}		RIPPLE CARRY	MAX	-	-	23	12.5	11.5	55	63	75

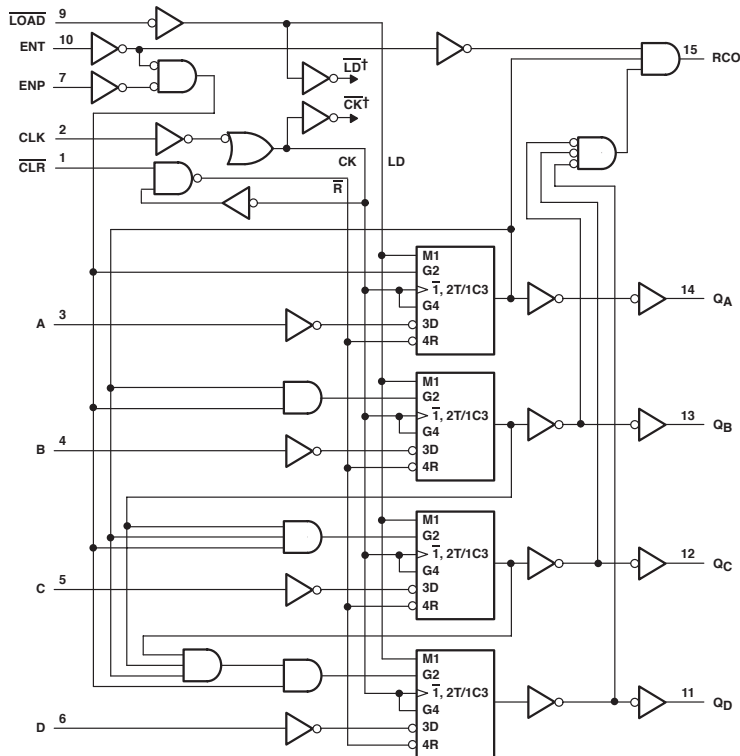
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT	LV 3V	LV 5V
f _{max}			MIN	103	91	50	85
t _w	CLOCK		MIN	4.8	5.4	5	5
	CLEAR			4.4	5.3	5	5
t _{su}	INPUT A, B, C, D		MIN	4.4	4.4	6.5	4.5
	ENABLE, P, T			-	-	9	6
	LOAD			5.3	5.3	9.5	6
	CLEAR INACTIVE			-	-	2.5	1.5
t _h			MIN	0	0	1	1
I _{PLH}	CLOCK	RIPPLE CARRY	MAX	15.2	15.2	23.5	14
I _{PHL}				15.2	15.2	23.5	14
I _{PLH}	CLOCK	ANY Q	MAX	15	15	18.5	11.5
I _{PHL}				15	15	18.5	11.5
I _{PLH}	ENABLE T	RIPPLE CARRY	MAX	9.4	9.8	18	11.5
I _{PHL}				9.4	9.8	18	11.5
I _{PHL}	CLEAR	ANY Q	MAX	15	15	19.5	12.5
I _{PHL}		RIPPLE CARRY	MAX	15	15	19	12

UNIT f_{max} : MHz, other : ns

SYNCHRONOUS 4-BIT BINARY COUNTERS

- Synchronous Clear Function
- Carry Output for n-Bit Cascading

Logic Diagram



† For simplicity, routing of complementary signals \overline{LD} and \overline{CK} is not shown on this overall logic diagram. The uses of these signals are shown on the logic diagram of the D/T flip-flops.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
I _{CC}	MAX	101	32	160	21	53	55	0.08	0.16	0.16	0.08	0.08	-	0.02	mA
I _{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	4	-4	-4	-24	-24	-6	-12	mA
I _{OL}	MAX	16	8	20	8	20	20	-4	4	4	24	24	-6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC
f _{max}			MIN	25	25	40	40	75	90	25
t _w	CLOCK		MIN	25	25	10	-	-	7	20
	CLEAR			20	20	10	12.5	6.7	-	-
t _{su}	INPUT A, B, C, D		MIN	20	20	4	15	8	5	38
				20	20	12	15	8	11.5	43
				25	20	14	15	8	11.5	34
				20	20	14	15	12	-	40
t _h			MIN	0	3	3	0	0	2	0
t _{PLH}	CLOCK	RIPPLE CARRY	MAX	35	35	25	20	16.5	15	54
t _{PHL}				35	35	25	20	12.5	15	54
t _{PLH}	CLOCK	ANY Q	MAX	25	24	15	15	7	9.5	51
t _{PHL}				29	27	15	20	13	11	51
t _{PLH}	ENABLE T	RIPPLE CARRY	MAX	16	14	15	13	9	8.5	49
t _{PHL}				16	14	15	13	8.5	49	

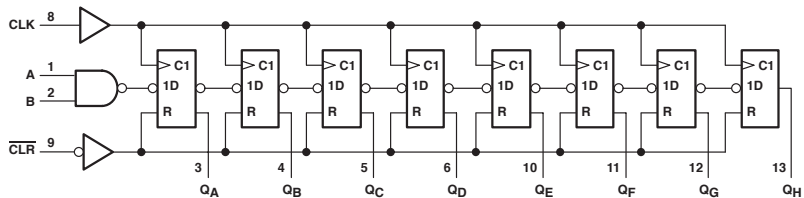
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V
f _{max}			MIN	20	20	103	91	50	85
t _w	CLOCK		MIN	24	24	4.8	5.4	5	5
	CLEAR			-	-	-	-	-	-
t _{su}	INPUT A, B, C, D		MIN	18	15	4.4	4.4	6.5	4.5
				15	20	4.4	5.3	9	6
				18	18	5.3	6.6	9.5	6
				20	20	5.3	6.6	4	3.5
t _h			MIN	3	5	0	0	1	1
t _{PLH}	CLOCK	RIPPLE CARRY	MAX	56	63	15.2	15.2	23.5	14
t _{PHL}				56	63	15.2	15.2	23.5	14
t _{PLH}	CLOCK	ANY Q	MAX	56	59	15	15	18.5	11.5
t _{PHL}				56	59	15	15	18.5	11.5
t _{PLH}	ENABLE T	RIPPLE CARRY	MAX	36	48	9.4	9.8	18	11.5
t _{PHL}				36	48	9.4	9.8	18	11.5

UNIT f_{max} : MHz, other : ns

8-BIT PARALLEL OUT SERIAL SHIFT REGISTERS

- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUTS				
CLEAR	CLOCK	A	B	QA	QB ... QH	
L	X	X	X	L	L	L
H	L	X	X	QA0	QB0	QH0
H	↑	H	H	H	QA _n	QH _n
H	↑	L	X	L	QA _n	QH _n
H	↑	X	L	L	QA _n	QH _n

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
I _{CC}	MAX	54	27	24	0.08	0.16	0.16	0.16	0.16	-	0.02	mA
I _{OH}	MAX	-0.4	-0.4	-0.4	-4	-4	-4	-24	-24	-6	-12	mA
I _{OL}	MAX	8	8	8	4	4	4	24	24	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
f _{max}			MIN	25	25	50	25	20	18	75	70
t _w	CLR "L"		MIN	20	20	16	25	18	27	4.5	4.5
	CLK "H"		MIN	20	20	10	20	24	27	6.7	7.1
	CLK "L"		MIN	20	20	10	20	24	27	6.7	7.1
t _{su}	DATA		MIN	15	15	6	25	18	18	2.5	2.5
	CLEAR INACTIVE		MIN	20	20	8	25	18	18	2.5	2.5
t _h			MIN	5	5	2	5	4	4	2.5	3
t _{PHL}	CLEAR	Q	MAX	42	36	20	51	42	57	13.9	15.8
t _{PLH}				30	27	16	44	51	54	12.5	14.9
t _{PHL}	CLOCK	Q	MAX	37	32	17	44	51	54	12.5	14.9

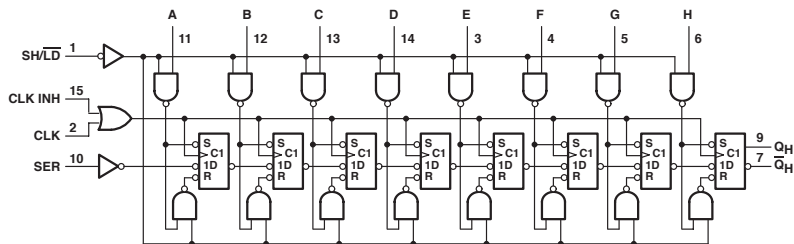
PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 3V	LV 5V
f _{max}			MIN	45	75
t _w	CLR "L"		MIN	5	5
	CLK "H"		MIN	5	5
	CLK "L"		MIN	5	5
t _{su}	DATA		MIN	6	4.5
	CLEAR INACTIVE		MIN	2.5	2.5
t _h			MIN	0	1
t _{PHL}	CLEAR	Q	MAX	18.5	12.5
t _{PLH}				18.5	12.5
t _{PHL}	CLOCK	Q	MAX	18.5	12.5

 UNIT f_{max}: MHz, other: ns

8-BIT SHIFT REGISTERS

- Complementary Outputs: Serial (QH, \overline{QH})
- Direct Overriding Load (Data) Inputs
- Parallel-to-Serial Data Conversion

Logic Diagram



FUNCTION TABLE

SHIFT/ LOAD	INPUTS				INTERNAL OUTPUTS		OUTPUT QH
	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	QA	QB	
L	X	X	X	a...h	a	b	h
H	L	L	X	X	QA0	QB0	QH0
H	L	↑	H	X	H	QAn	QGn
H	L	↑	L	X	L	QAn	QGn
H	H	X	X	X	QA0	QB0	QH0

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I _{CC}	MAX	63	30	24	0.08	0.16	0.16	-	0.02	mA
I _{DH}	MAX	-0.8	-0.4	-0.4	-4	-4	-4	-6	-12	mA
I _{OL}	MAX	16	8	8	4	4	4	6	12	mA

SWITCHING CHARACTERISTICS

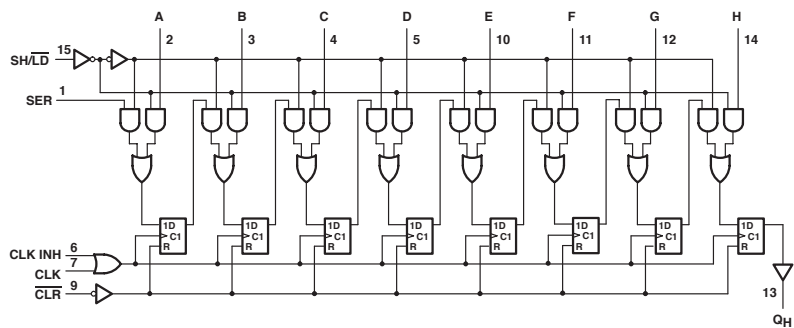
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
t _{max}			MIN	20	25	45	25	20	18	50	85
t _w	CLOCK	High	MIN	25	15	11	20	24	27	7	4
		Low	MIN	25	25	11	20	24	27	7	4
	SH/ $\overline{\text{LD}}$ "L"	High	MIN	15	25	-	-	-	-	-	-
		Low	MIN	15	17	12	20	24	30	9	6
t _{su}	CLK INH		MIN	30	30	11	25	24	30	5	3.5
	DATA			10	10	10	25	24	30	8.5	5
	SER			20	20	10	10	24	30	6	4
	SH/ $\overline{\text{LD}}$ "H"			45	45	10	20	-	-	6	4
t _h			MIN	0	0	4	5	11	11	0.5	1
t _{PLH}	CLOCK	Q _H or $\overline{\text{Q}}_{\text{H}}$	MAX	24	25	13	38	50	60	21.5	13.5
t _{PHL}				31	25	14	38	50	60	21.5	13.5
t _{PLH}	SH/ $\overline{\text{LD}}$	Q _H or $\overline{\text{Q}}_{\text{H}}$	MAX	31	35	20	38	53	60	22	13.5
t _{PHL}				40	35	22	38	53	60	22	13.5
t _{PLH}	H	Q _H	MAX	17	25	13	38	45	53	20	12.5
t _{PHL}				36	30	16	38	45	53	20	12.5
t _{PLH}	H	$\overline{\text{Q}}_{\text{H}}$	MAX	27	30	15	38	45	53	20	12.5
t _{PHL}				27	25	16	38	45	53	20	12.5

UNIT f_{max} : MHz, other : ns

8-BIT SHIFT REGISTERS

- Synchronous Load
- Direct Overriding Clear
- Parallel-to-Serial Conversion

Logic Diagram



FUNCTION TABLE

CLEAR	INPUTS					INTERNAL OUTPUTS		OUTPUT
	SHIFT/LOAD	CLOCK INHIBIT	CLOCK	SERIAL	PARALLEL A...H	QA	QB	
L	X	X	X	X	X	L	L	L
H	X	L	L	X	X	QA0	QB0	QH0
H	L	L	↑	X	a...h	a	b	h
H	H	L	↑	H	X	H	QA _n	QH _n
H	H	L	↑	L	X	L	QA _n	QH _n
H	X	H	↑	X	X	QA0	QB0	QH0

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I _{CC}	MAX	127	32	24	60	0.08	0.16	0.16	-	0.02	mA
I _{OH}	MAX	-0.8	-0.4	-0.4	-1	-4	-4	-4	-6	-12	mA
I _{OL}	MAX	16	8	8	20	4	4	4	6	12	mA

SWITCHING CHARACTERISTICS

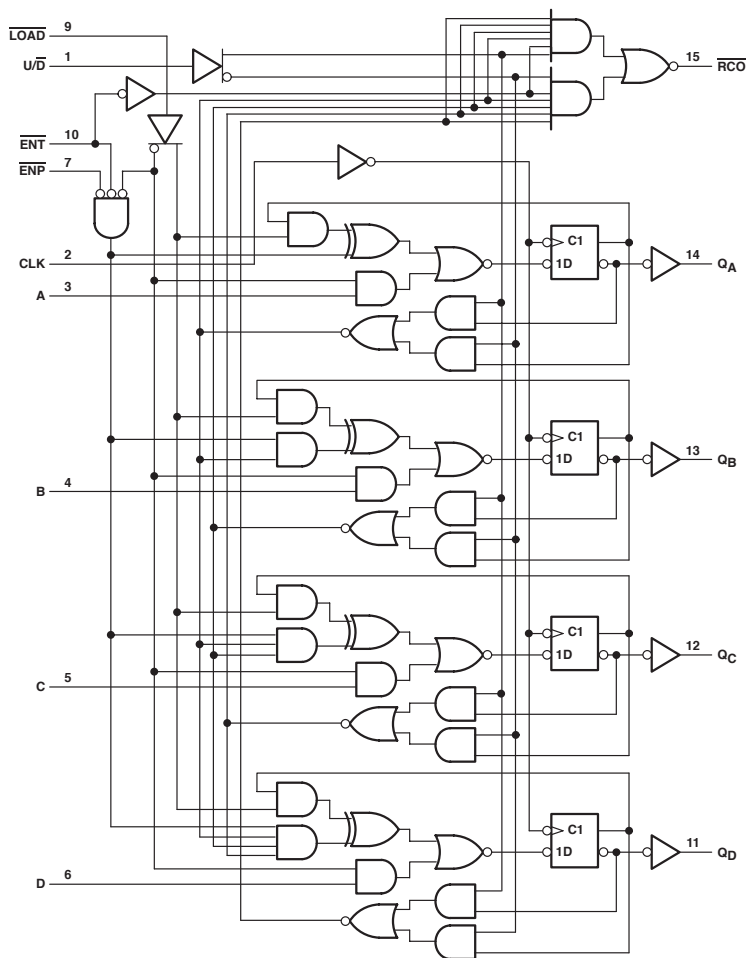
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
f _{max}			MIN	25	25	45	110	25	20	16	50	85
t _w	CLOCK		MIN	20	20	10	3.5	20	24	30	7	4
	CLEAR			20	25	9	4	25	30	53	7	5
t _{su}	Mode Control		MIN	30	30	16	4	36	44	45	6	4
	DATA			20	20	7	3	20	24	24	6	4.5
t _h			MIN	0	0	3	0	0	1	0	0	1
t _{PHL}	CLEAR	QH	MAX	35	30	14	9.5	30	48	60	18.5	12
t _{PLH}	CLOCK	QH	MAX	30	25	13	14	38	48	60	21.5	13.5
				26	20	12	9	38	48	60	21.5	13.5

 UNIT f_{max} : MHz, other : ns

4-BIT UP/DOWN SYNCHRONOUS ONOUS BINARY COUNTERS

- Fully Synchronous Operation for Counting and Programming
- Internal Carry Look-Ahead Circuitry for Fast Counting
- Carry Output for n-Bit Cascading

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	S	ALS	AS	F	UNIT
I _{CC}		MAX	45	160	25	63	52	mA
I _{OH}	\overline{RCO}	MAX	-0.4	-1	-0.4	-2	-1	mA
	Q	MAX	-1.2	-1	-0.4	-2	-1	mA
I _{OL}	\overline{RCO}	MAX	8	20	8	20	20	mA
	Q	MAX	24	20	8	20	20	mA

SWITCHING CHARACTERISTICS

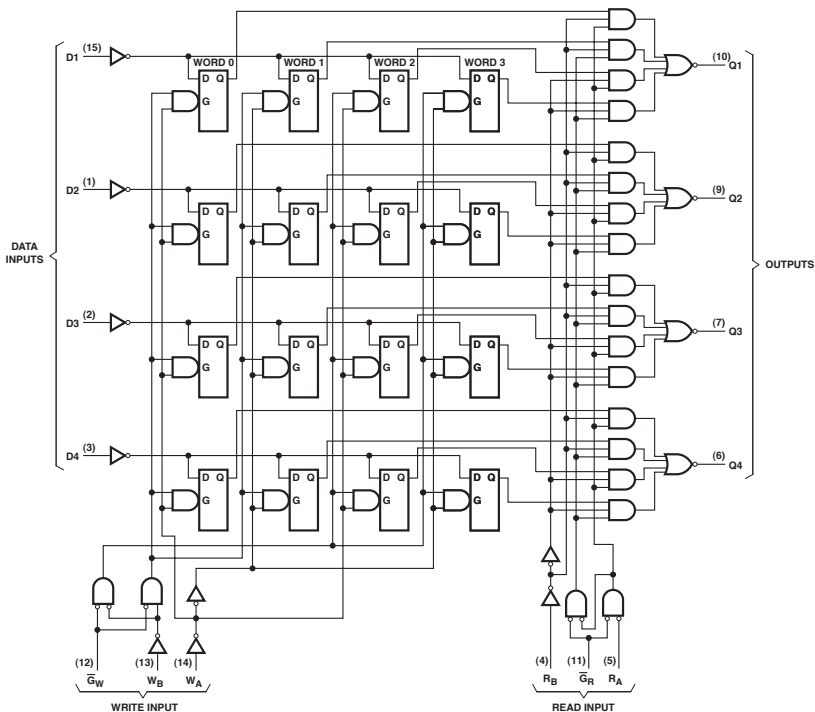
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F
f _{max}			MIN	20	40	40	75	90
t _{PLH}	CLK	\overline{RCO}	MAX	40	21	20	16.5	17
				25	28	20	13	12.5
t _{PHL}	CLK	ANY Q	MAX	25	15	15	13	9.5
				25	15	20	7	13
t _{PLH}	\overline{ENT}	\overline{RCO}	MAX	25	12	13	9	7
				20	25	16	9	9
t _{PHL}	U/ \overline{D}	\overline{RCO}	MAX	35	15	19	12	12.5
				25	22	19	13	12

UNIT f_{max} : MHz, other : ns

4-BY-4 REGISTER FILES

- Separate Read/Write Addressing Permits Simultaneous Reading and Writing
- Fast Access Times: Typically 20ns
- Expandable to 1024 Words of 4 Bits

Logic Diagram



WRITE FUNCTION TABLE

WRITE INPUTS			OUTPUTS			
\overline{W}_B	\overline{W}_A	\overline{G}_W	0	1	2	3
L	L	L	$Q = D$	Q_0	Q_0	Q_0
L	H	L	Q_0	$Q = D$	Q_0	Q_0
H	L	L	Q_0	Q_0	$Q = D$	Q_0
H	H	L	Q_0	Q_0	Q_0	$Q = D$
X	X	H	Q_0	Q_0	Q_0	Q_0

READ FUNCTION TABLE

READ INPUTS			OUTPUTS			
\overline{R}_B	\overline{R}_A	\overline{G}_R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	150	40	mA
V_{OH}	MAX	5.5	5.5	V
I_{OL}	MAX	16	8	mA

SWITCHING CHARACTERISTICS

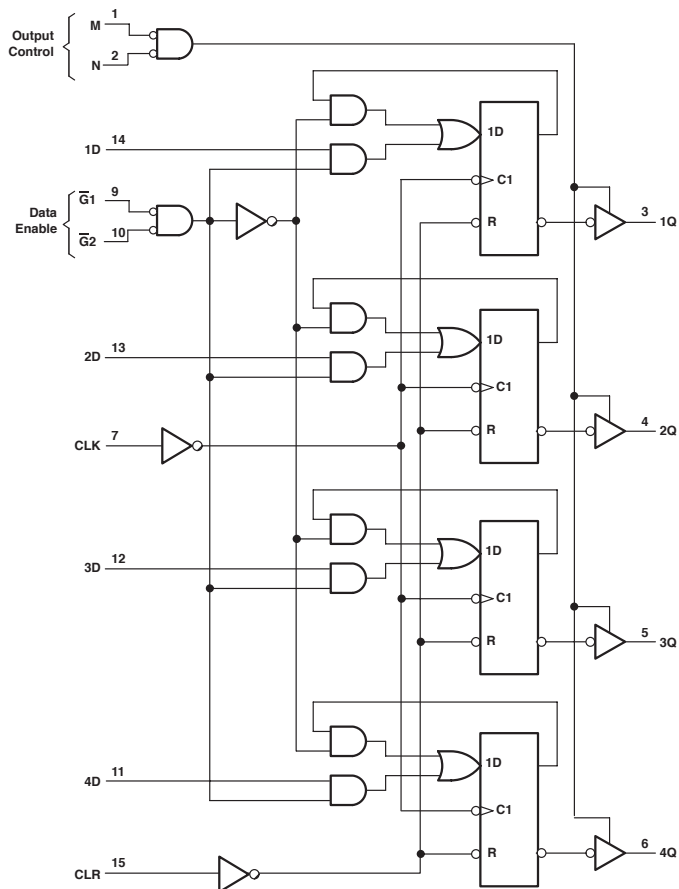
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
f_{max}			MIN		
t_W			MIN	25	25
t_{su}	D		MIN	10	10
	W		MIN	15	15
t_h	D		MIN	15	15
	W		MIN	5	5
t_{PLH}	READ ENABLE	Q	MAX	15	30
t_{PHL}	READ ENABLE	Q	MAX	30	30
t_{PLH}	READ SELECT	Q	MAX	35	40
t_{PHL}	READ SELECT	Q	MAX	40	40
t_{PLH}	WRITE ENABLE	Q	MAX	40	45
t_{PHL}	WRITE ENABLE	Q	MAX	45	40
t_{PLH}	DATA	Q	MAX	30	45
t_{PHL}	DATA	Q	MAX	45	35

 UNIT f_{max} : MHz, other : ns

4-BIT D-TYPE REGISTERS

- 3-State Outputs Interface Directly
- Fully Independent Clock Virtually

Logic Diagram



FUNCTION TABLE

		INPUTS				OUTPUT Q
CLEAR	CLOCK	DATA	ENABLE	DATA	D	
		G1	G2			
H	X	X	X	X	X	L
L	L	X	X	X	X	Q _O
L	↑	H	X	X	X	Q _O
L	↑	X	H	X	X	Q _O
L	↑	L	L	L	L	L
L	↑	L	L	H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	72	24	0.08	0.16	0.16	mA
I _{DH}	MAX	-5.2	-2.6	-6	-6	-6	mA
I _{OL}	MAX	16	24	6	6	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
f _{max}			MIN	25	25	25	20	13
t _w			MIN	20	25	20	24	28
t _{su}	DATA ENABLE		MIN	17	35	25	18	18
	DATA			10	17	25	18	27
	CLR INACTIVE		MIN	10	10	23	-	-
t _h	DATA ENABLE		MIN	2	0	0	0	0
	DATA			10	3	0	3	0
t _{PHL}	CLEAR	Q	MAX	27	35	38	53	66
t _{PLH}	CLOCK	Q	MAX	43	25	38	60	60
t _{PHL}				31	30	38	60	60
t _{PZH}	ENABLE	Q	MAX	30	23	38	45	45
t _{PZL}				30	27	38	45	45
t _{PHZ}	DISABLE	Q	MAX	14	20	38	45	-
t _{PLZ}				20	17	38	45	-

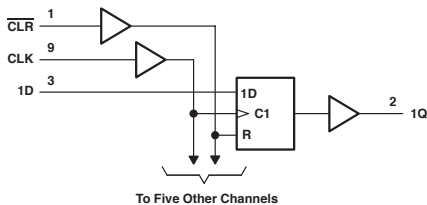
UNIT f_{max} : MHz, other : ns

HEX D-TYPE FLIP-FLOPS

- Buffered Clock and Direct Clear Inputs
- Fully Buffered Outputs for Maximum Isolation from External Disturbances

FUNCTION TABLE

INPUTS			OUTPUT
CLEAR	CLOCK	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
L	L	X	Q _O



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	65	26	144	19	45	55	0.08	0.16	0.16	mA
I _{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	mA
I _{OL}	MAX	16	8	20	8	20	20	4	4	4	mA

PARAMETER	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	UNIT
I _{CC}	MAX	0.16	0.16	0.04	0.04	-	0.02	mA
I _{OH}	MAX	-24	-24	-8	-8	-6	-12	mA
I _{OL}	MAX	24	24	8	8	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC
f _{max}			MIN	25	30	75	50	100	80	25	20	17	95
t _w	CLR LOW		MIN	20	20	10	10	5	5	20	24	38	4
			MIN	20	20	7	10	4	4	20	24	30	5.2
t _{su}	DATA INPUT		MIN	20	20	7	10	6	6	20	24	30	5.2
			MIN	20	20	5	10	4	4.5	25	18	24	2
t _h	CLR INACTIVE		MIN	25	25	5	6	6	5	25	-	-	-
			MIN	5	5	3	0	1	1	0	5	5	3
t _{PLH}	CLR	ANY Q	MAX	25	-	-	18	-	-	40	45	66	14.5
t _{PHL}			MAX	35	35	22	23	14	15	40	45	66	14.5
t _{PLH}	CLK	ANY Q	MAX	30	30	12	15	8	9	40	50	60	13.5
t _{PHL}			MAX	35	30	17	17	10	11	40	50	60	13.5

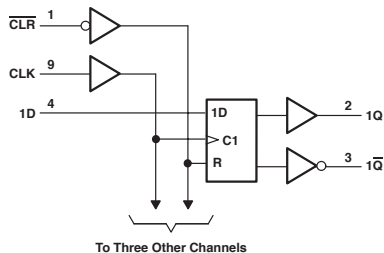
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V
f _{max}			MIN	80	80	65	50	80
t _w	CLR LOW		MIN	4	5	5	5	5
			MIN	6.2	5	5	5	5
t _{su}	DATA INPUT		MIN	6.2	5	5	5	5
			MIN	2	4.5	5	6	4.5
t _h	CLR INACTIVE		MIN	-	2.5	3.5	3	2.5
			MIN	2.5	0.5	0	0	0.5
t _{PLH}	CLR	ANY Q	MAX	15.5	-	-	17	11
t _{PHL}			MAX	15.5	11	13	17	11
t _{PLH}	CLK	ANY Q	MAX	14	10.5	10	16.5	10.5
t _{PHL}			MAX	14	10.5	10	16.5	10.5

UNIT f_{max}: MHz, other: ns

QUAD D-TYPE FLIP-FLOPS

- Complementary Outputs (Q , \bar{Q})
- Buffered Clock and Direct Clear Inputs
- Asynchronous Clear Function

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	CLOCK	D	Q	\bar{Q}
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	\bar{Q}_0

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	AC 11	CD74 AC	CD74 ACT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	45	18	96	14	34	34	0.04	0.16	0.16	0.08	0.16	0.16	-	0.02	mA
I_{OH}	MAX	-0.8	-0.4	-1	-0.4	-2	-1	-4	-4	-4	-24	-24	-24	-6	-12	mA
I_{OL}	MAX	16	8	20	8	20	20	4	4	4	24	24	24	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT
f_{max}			MIN	25	30	75	50	100	100	25	20	16
t_w	CLR LOW		MIN	20	20	10	10	5	5	20	24	30
				20	20	7	10	4	4	20	24	30
				20	20	7	10	5	5	20	24	30
t_{su}	DATA INPUT		MIN	20	20	5	10	3	3	25	24	30
				25	25	5	6	6	5	25	-	-
				5	5	3	0	1	1	0	5	5
t_h			MIN	5	5	3	0	1	1	0	5	5
t_{PLH}	CLR	ANY Q or \bar{Q}	MAX	25	30	15	18	9	9	38	53	53
35				30	22	23	13	13	38	53	53	
t_{PHL}	CLK	ANY Q or \bar{Q}	MAX	30	25	12	15	7.5	7.5	38	53	50
35				25	17	17	10	9.5	38	53	50	

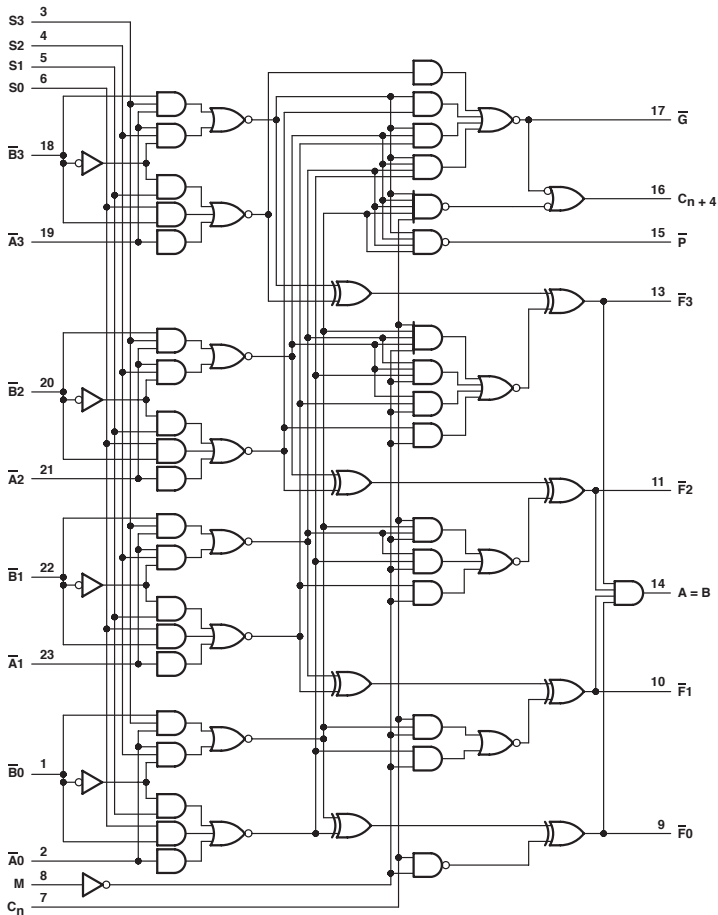
PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	CD74 AC	CD74 ACT	LV 3V	LV 5V
f_{max}			MIN	125	100	114	45	75
t_w	CLR LOW		MIN	4	4	4	5	5
				4	5	5	5	5
				4	5	5	5	5
t_{su}	DATA INPUT		MIN	5.5	2	2	5	4
				5.5	-	-	5	5
				0.5	2	2	1	1
t_h			MIN	0.5	2	2	1	1
t_{PLH}	CLR	ANY Q or \bar{Q}	MAX	6.8	12.2	13	15.5	9.5
9.3				12.2	13	15.5	9.5	
t_{PHL}	CLK	ANY Q or \bar{Q}	MAX	6.9	12.2	11.5	17	10.5
9.3				12.2	11.5	17	10.5	

UNIT f_{max} : MHz, other : ns

ARITHMETIC LOGIC UNITS/FUNCTION GENERATORS

- Full Look-Ahead for High-Speed Operations on Long Words
- Input Clamping Diodes Minimize Transmission-Line Effects

Logic Diagram



FUNCTION TABLE (ACTIVE LOW)

SELECTION	ACTIVE-LOW DATA		
	M = H LOGIC FUNCTION	M = L; ARITHMETIC OPERATIONS	
		Cn = L (no carry)	Cn = H (with carry)
L L L L	$F = \overline{A}$	F = A MINUS 1	F = A
L L L H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
L L H L	$F = \overline{A + B}$	F = AB MINUS 1	F = AB
L L H H	$F = 1$	F = MINUS 1/2'S COMPL	F = 0
L H L L	$F = \overline{A + \overline{B}}$	F = A PLUS (A + \overline{B})	F = A PLUS (A + \overline{B}) PLUS 1
L H L H	$F = \overline{B}$	F = AB PLUS (A + \overline{B})	F = AB PLUS (A + \overline{B}) PLUS 1
L H H L	$F = \overline{A \oplus \overline{B}}$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	$F = \overline{A + \overline{B}}$	F = A + \overline{B}	F = (A + \overline{B}) PLUS 1
H L L L	$F = \overline{AB}$	F = A PLUS (A + B)	F = A PLUS (A + B) PLUS 1
H L L H	$F = A \oplus B$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	$F = \overline{B}$	F = AB PLUS (A + B)	F = AB PLUS (A + B) PLUS 1
H L H H	$F = \overline{A + B}$	F = (A + B)	F = (A + B) PLUS 1
H H L L	F = 0	F = A PLUS A'	F = A PLUS A PLUS 1
H H L H	$F = \overline{AB}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H L	$F = \overline{AB}$	F = AB PLUS A	F = AB PLUS A PLUS 1
H H H H	F = A	F = A	F = A PLUS 1

FUNCTION TABLE (ACTIVE HIGH)

SELECTION	ACTIVE-HIGH DATA		
	M = H LOGIC FUNCTION	M = L; ARITHMETIC OPERATIONS	
		Cn = H (no carry)	Cn = L (with carry)
L L L L	$F = \overline{A}$	F = A	F = A PLUS 1
L L L H	$F = \overline{A + \overline{B}}$	F = A + B	F = (A + B) PLUS 1
L L H L	$F = \overline{AB}$	F = A + \overline{B}	F = (A + \overline{B}) PLUS 1
L L H H	F = 0	F = MINUS 1/2'S COMPL	F = 0
L H L L	$F = \overline{A + \overline{B}}$	F = A PLUS AB	F = A PLUS AB PLUS 1
L H L H	$F = \overline{B}$	F = (A + B) PLUS AB	F = (A + B) PLUS AB PLUS 1
L H H L	$F = A \oplus B$	F = A MINUS B MINUS 1	F = A MINUS B
L H H H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
H L L L	$F = \overline{A + B}$	F = A PLUS AB	F = A PLUS AB PLUS 1
H L L H	$F = A \oplus \overline{B}$	F = A PLUS B	F = A PLUS B PLUS 1
H L H L	$F = \overline{B}$	F = (A + \overline{B}) PLUS AB	F = (A + \overline{B}) PLUS AB PLUS 1
H L H H	$F = \overline{AB}$	F = AB MINUS 1	F = AB
H H L L	F = 1	F = A PLUS A'	F = A PLUS A PLUS 1
H H L H	$F = \overline{A + \overline{B}}$	F = (A + B) PLUS A	F = (A + B) PLUS A PLUS 1
H H H L	$F = \overline{A + B}$	F = (A + \overline{B}) PLUS A	F = (A + \overline{B}) PLUS A PLUS 1
H H H H	F = A	F = A MINUS 1	F = A

RECOMMENDED OPERATING CONDITIONS

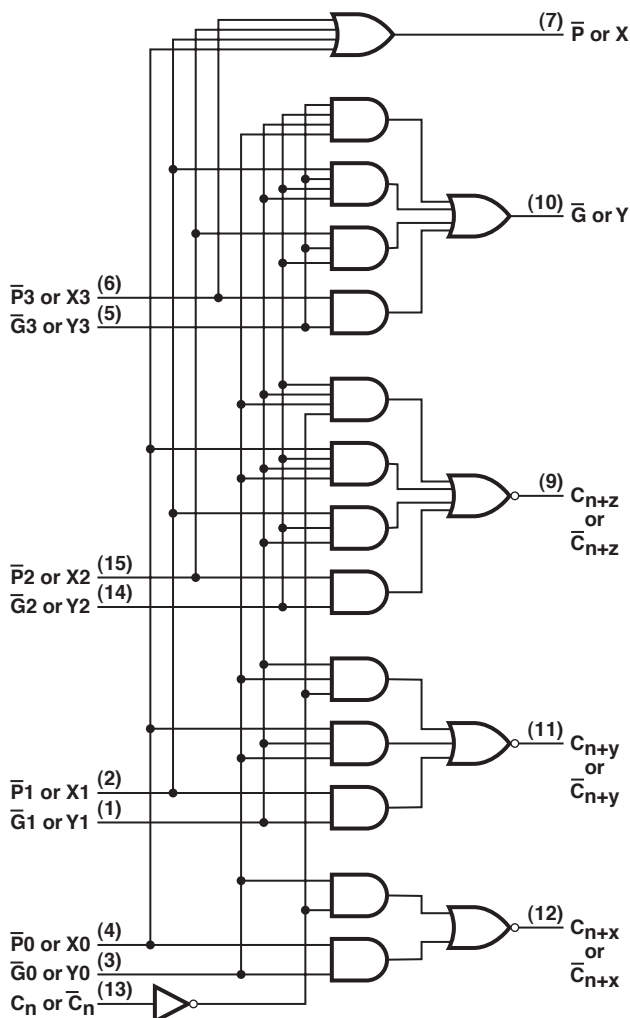
PARAMETER		MAX or MIN	TTL	LS	S	AS	UNIT
I _{CC}		MAX	150	37	220	200	mA
I _{OH}	All outputs except $A = B$	MAX	-0.8	-0.4	-1	-2	mA
	\overline{B}		-	-	-	-3	mA
I _{OL}	All outputs except \overline{B}	MAX	16	8	20	20	mA
	\overline{B}		16	8	20	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	AS
t _{PLH}	C _n	C _n · 4	MAX	18	27	10.5	9
t _{PHL}				19	20	10.5	9
t _{PLH}	$\overline{A}, \overline{B}$	C _n · 4	MAX	43	38	18.5	12
t _{PHL}				41	38	18.5	12
t _{PLH}	C _n	F	MAX	19	26	12	9
t _{PHL}				18	20	12	9
t _{PLH}	$\overline{A}_1, \overline{B}_1$	\overline{F}_1	MAX	42	32	16.5	9.5
t _{PHL}				32	20	16.5	8

UNIT: ns

Logic Diagram



FUNCTION TABLE

\bar{G} OUTPUTS

INPUTS						OUTPUT	
\bar{G}_3	\bar{G}_2	\bar{G}_1	\bar{P}_3	\bar{P}_2	\bar{P}_1	\bar{P}_0	\bar{G}
L	X	X	X	X	X	X	L
X	L	X	X	L	X	X	L
X	X	L	X	L	L	X	L
X	X	X	L	L	L	L	L
X	X	X	L	L	L	L	L
All other combinations							H

\bar{P} OUTPUTS

INPUTS				OUTPUT
\bar{P}_3	\bar{P}_2	\bar{P}_1	\bar{P}_0	\bar{P}
L	L	L	L	L
All other combinations				H

C_{n+x} OUTPUTS

INPUTS			OUTPUT
\bar{G}_0	\bar{P}_0	C_n	C_{n+x}
L	X	X	H
X	L	H	H
All other combinations			L

C_{n+y} OUTPUTS

INPUTS						OUTPUT
\bar{G}_1	\bar{G}_0	\bar{P}_1	\bar{P}_0	C_n		C_{n+y}
L	X	X	X	X		H
X	L	L	X	X		H
X	X	L	L	H		H
All other combinations						L

C_{n+z} OUTPUTS

INPUTS							OUTPUT
\bar{G}_2	\bar{G}_1	\bar{G}_0	\bar{P}_2	\bar{P}_1	\bar{P}_0	C_n	C_{n+z}
L	X	X	X	X	X	X	H
X	L	X	L	X	X	X	H
X	X	L	L	L	X	X	H
X	X	X	L	L	L	H	H
All other combinations							L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	S	AS	UNIT
I_{CC}	MAX	72	109	36	mA
I_{OH}	MAX	-0.8	-1	-2	mA
I_{OL}	MAX	16	20	20	mA

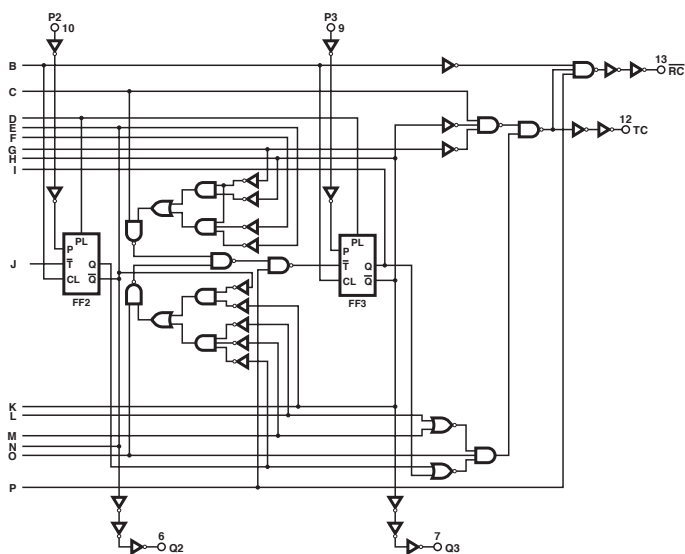
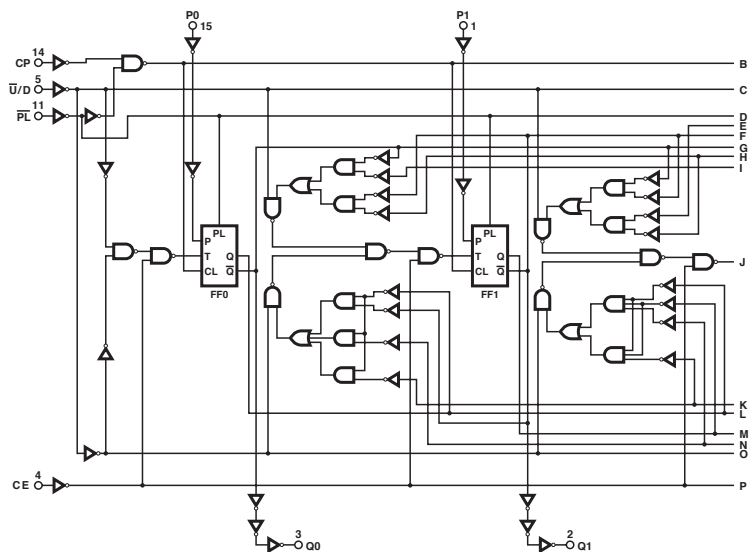
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	S	AS
t_{PLH}	C_n	$C_n + X, C_n + Y$ or $C_n + Z$	MAX	10	10	10
t_{PHL}				10.5	10.5	9.5
t_{PLH}	P or \bar{G}	$C_n + X, C_n + Y$ or $C_n + Z$	MAX	7	7	10.5
t_{PHL}				7	7	6
t_{PLH}	P or \bar{G}	\bar{G}	MAX	7.5	7.5	12
t_{PHL}				10.5	10.5	8
t_{PLH}	\bar{P}	\bar{P}	MAX	6.5	6.5	7.5
t_{PHL}				10	10	6

UNIT: ns

SYNCHRONOUS UP/DOWN DECADE COUNTER

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	UNIT
I _{CC}	MAX	105	35	22	0.08	0.16	mA
I _{OH}	MAX	-0.8	-0.4	-0.4	-4	-4	mA
I _{OL}	MAX	16	8	8	4	4	mA

SWITCHING CHARACTERISTICS

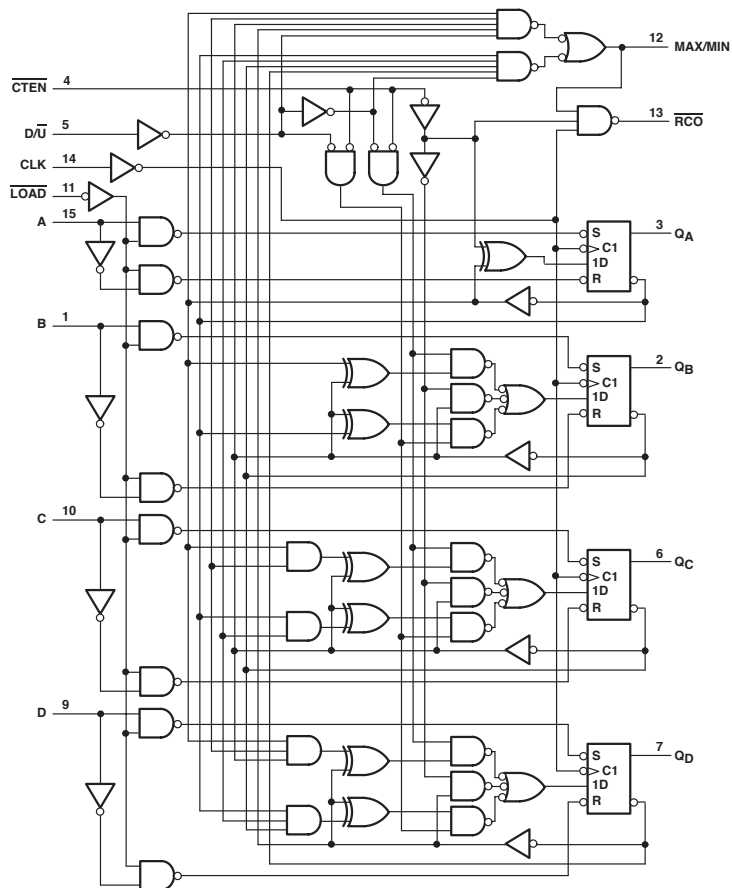
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC
f _{max}			MIN	20	20	25	17	25
t _w	CLK (CP)		MIN	25	25	20	30	20
	LOAD (PL)			35	35	20	30	25
t _{su}	Data, high or low		MIN	20	20	20	38	15
t _h	Data hold time		MIN	0	5	5	5	2
t _{PLH}	LOAD (PL)	Q	MAX	33	33	30	66	49
				50	50	30	66	49
t _{PHL}	DATA	Q	MAX	22	32	21	60	44
				50	40	21	60	44
t _{PLH}	CLK (CP)	RCO (RC)	MAX	20	20	20	30	31
				24	24	20	30	31
t _{PHL}	CLK (CP)	Q	MAX	24	24	18	48	43
				36	36	18	48	43
t _{PLH}	CLK (CP)	MAX/MIN (TC)	MAX	42	42	31	63	53
				52	52	31	63	53
t _{PLH}	D/U (U/D)	RCO (RC)	MAX	45	45	37	57	38
				45	45	28	57	38
t _{PHL}	D/U (U/D)	MAX/MIN (TC)	MAX	33	33	25	48	41
				33	33	25	48	41

UNIT f_{max} : MHz other : ns

SYNCHRONOUS UP/DOWN COUNTERS

- Count Enable Control Input
- Ripple Clock Output for Cascading
- Asynchronously Presentable with Load Control

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	105	35	22	0.08	0.16	0.16	mA
I _{OH}	MAX	-0.8	-0.4	-0.4	-4	-4	-4	mA
I _{OL}	MAX	16	8	8	4	4	4	mA

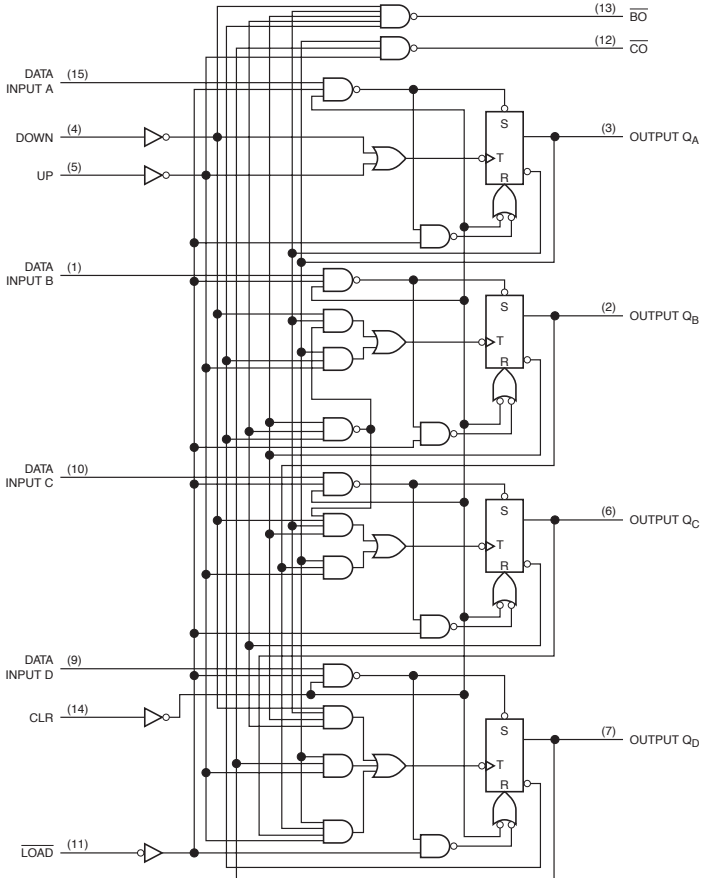
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT
f _{max}			MIN	20	20	30	17	25	25
t _w	CLK		MIN	25	25	16.5	30	20	20
	LOAD			35	35	20	30	25	25
t _{su}	DATA		MIN	20	20	20	38	15	15
t _h	DATA		MIN	0	5	5	5	2	2
t _{PLH}	LOAD	QA, QB QC, QD	MAX	33	33	30	66	49	50
				50	50	30	66	49	50
t _{PLH}	DATA A, B, C, D	QA, QB QC, QD	MAX	22	32	21	60	44	48
				50	40	21	60	44	48
t _{PLH}	CLK	RIPPLE CLK	MAX	20	20	20	30	31	34
				24	24	20	30	31	34
t _{PLH}	CLK	QA, QB QC, QD	MAX	24	24	18	48	43	44
				36	36	18	48	43	44
t _{PLH}	CLK	MAX or MIN	MAX	42	42	31	63	53	53
				52	52	31	63	53	53
t _{PLH}	D/ \bar{U}	RIPPLE CLK	MAX	45	45	37	57	38	38
				45	45	28	57	38	38
t _{PLH}	D/ \bar{U}	MAX or MIN	MAX	33	33	25	48	41	48
				33	33	25	48	41	48

UNIT f_{max} : MHz, other : ns

PRESETTABLE SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

Logic Diagram



FUNCTION TABLE

CLOCK UP	CLOCK DOWN	RESET	PARALLEL LOAD	FANCTION
↑	H	L	H	Count Up
H	↑	L	H	Count Down
X	X	H	X	Reset
X	X	L	L	Load Preset inputs

NOTE: H = High Voltage Level, L = Low Voltage Level, X = Don't Care, ↑ = Transition from Low to High Level

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I _{CC}	MAX	0.16	mA
I _{OH}	MAX	-4	mA
I _{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

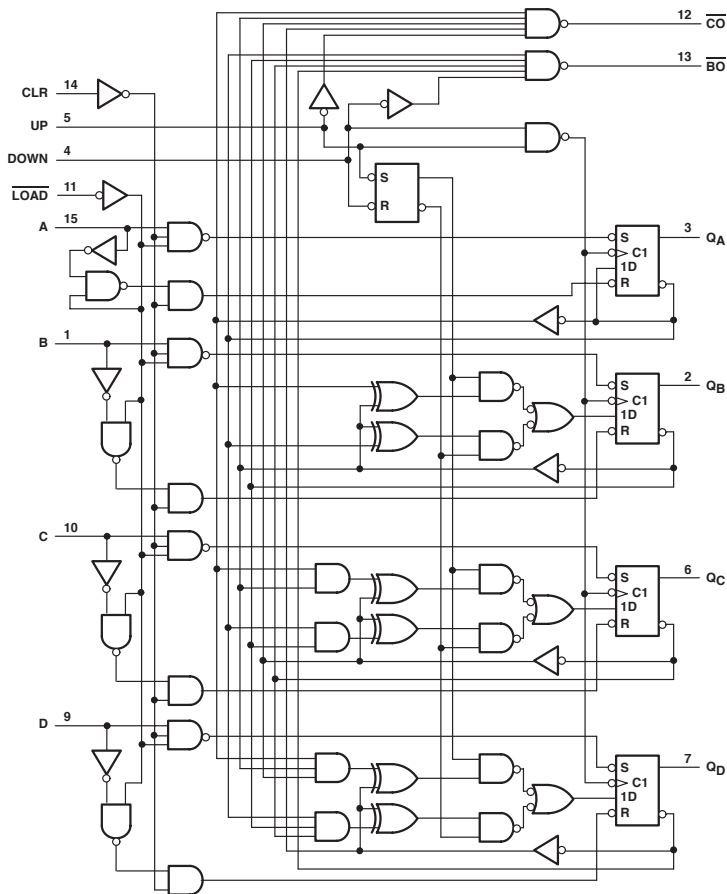
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t _w	CPU, CPD		MIN	35
	PL			24
	MR			30
t _{su}	P _n to PL		MIN	24
t _h	P _n to PL		MIN	0
	CPD to CPU, CPD to CPU			24
t _{PLH}	CPU	TCU	MAX	38
t _{PHL}				38
t _{PLH}	CPD	TCD	MAX	38
t _{PHL}				38
t _{PLH}	CPD	Q _n	MAX	65
t _{PHL}				65
t _{PLH}	CPD	Q _n	MAX	65
t _{PHL}				65
t _{PLH}	PL	Q _n	MAX	66
t _{PHL}				66
t _{PHL}	MR	Q _n	MAX	60

UNIT:ns

SYNCHRONOUS UP/DOWN DUAL CLOCKCOUNTERS

- Parallel Asynchronous Load for Modulo-N Count Lengths
- Asynchronous Clear

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	102	34	22	54	0.08	0.16	0.16	mA
I _{OH}	MAX	-0.4	-0.4	-0.4	-1	-4	-4	-4	mA
I _{OL}	MAX	16	8	8	20	4	4	4	mA

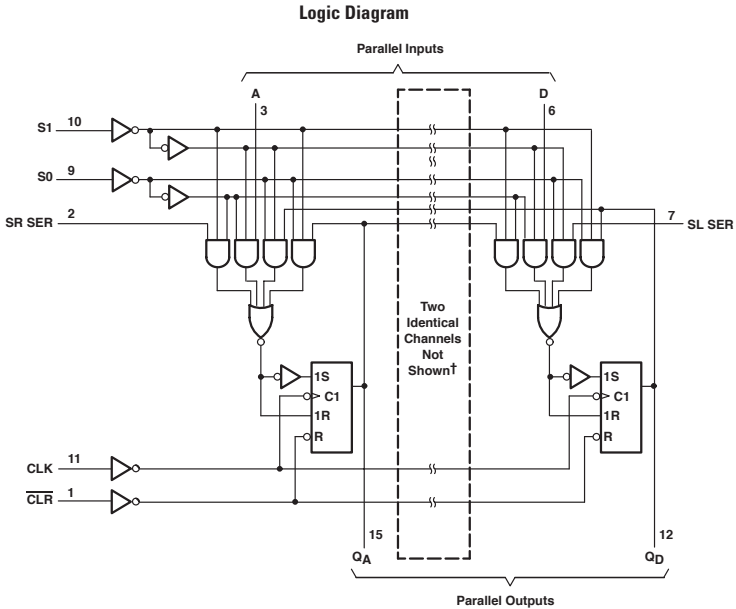
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	F	SN74 HC	CD74 HC	CD74 HCT
t _{max}			MIN	25	25	30	85	17	17	15
t _w			MIN	20	20	20	4	30	30	35
t _{su}			MIN	20	20	20	3.5	28	24	22
t _h			MIN	0	5	5	2.5	5	0	0
t _{PLH}	UP	$\overline{C0}$	MAX	26	26	16	9	41	38	41
t _{PHL}				24	24	18	9	41	38	41
t _{PLH}	DOWN	$\overline{B0}$	MAX	24	24	16	9	41	38	41
t _{PHL}				24	24	18	9	41	38	41
t _{PLH}	UP or DOWN	ANY Q	MAX	38	38	19	9	63	65	60
t _{PHL}				47	47	17	13	63	65	60
t _{PLH}	\overline{LOAD}	ANY Q	MAX	40	40	30	11	65	66	69
t _{PHL}				40	40	28	13	65	66	69
t _{PHL}	CLR	ANY Q	MAX	35	35	17	12	60	60	65

UNIT f_{max} : MHz, other : ns

4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTERS

- Direct Overriding Clear
- Parallel-to-Serial, Serial-to-Parallel Conversions
- Left or Right Shifts



† I/O ports not shown: Q_B (14) and Q_C (13)

FUNCTION TABLE

CLEAR	INPUTS						OUTPUTS						
	MODE		CLOCK	SERIAL		PARALLEL				Q _A	Q _B	Q _C	Q _D
	S1	S0		LEFT	RIGHT	A	B	C	D				
L	X	X	X	X	X	X	X	X	L	L	L	L	
H	X	X	L	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	
H	H	H	↑	X	X	a	b	c	a	b	c	d	
H	L	H	↑	X	H	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}	
H	L	H	↑	X	L	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}	
H	H	L	↑	H	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	H	
H	H	L	↑	L	X	X	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	L	
H	L	L	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	63	23	135	53	0.1	0.16	0.16	mA
I _{OH}	MAX	-0.8	-0.4	-1	-2	-4	-4	-4	mA
I _{OL}	MAX	16	8	20	20	4	4	4	mA

SWITCHING CHARACTERISTICS

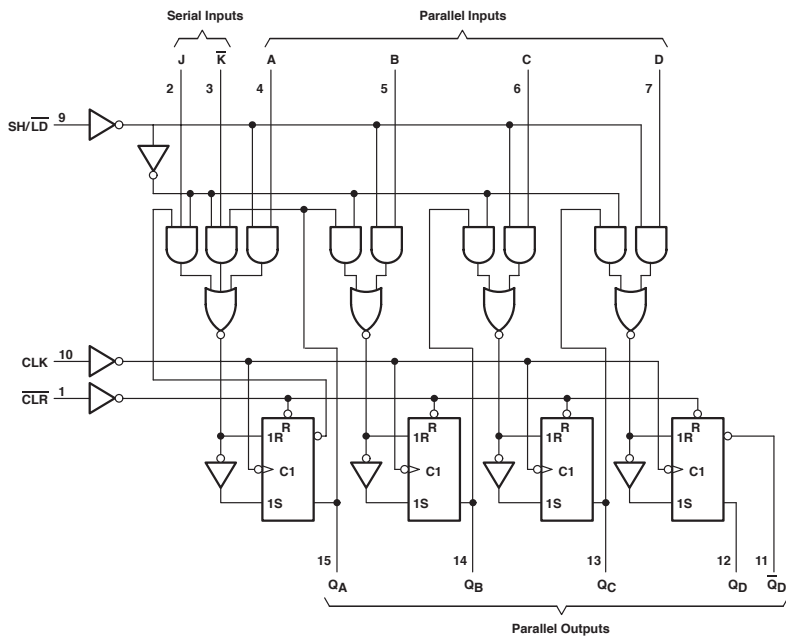
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	CD74 HCT
f _{max}			MIN	25	25	70	80	25	20	18
t _w	CLR		MIN	20	20	12	4.5	20	24	24
	CLK "H"			20	20	7	4	20	24	24
	CLK "H"			20	20	7	7	20	24	24
t _{su}	Mode Control		MIN	30	30	11	9.5	25	24	30
	DATA			20	20	5	4	25	21	21
	CLR INACTIVE			25	25	9	6	-	-	-
t _h			MIN	0	0	3	0.5	0	0	0
t _{PHL}	CLR	ANY	MAX	30	30	18.5	12	38	42	60
t _{PLH}				22	22	12	7	36	53	56
t _{PHL}	CLOCK	ANY	MAX	26	26	16.5	7	36	53	56

UNIT f_{max} : MHz, other : ns

4-BIT PARALLEL-ACCESS SHIFT REGISTERS

- Direct Overriding Clear
- Parallel-to-Serial, Serial-to-Parallel Conversions

Logic Diagram



FUNCTION TABLE

INPUTS						OUTPUTS							
CLEAR	SHIFT/ LOAD	CLOCK	SERIAL		PARALLEL				Q _A	Q _B	Q _C	Q _D	Q̄ _D
			J	K̄	A	B	C	D					
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	Q̄ _D
H	H	L	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q̄ _{D0}
H	H	↑	L	H	X	X	X	X	Q _{A0}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q̄ _{Cn}
H	H	↑	L	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Cn}
H	H	↑	H	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Cn}
H	H	↑	H	L	X	X	X	X	Q _{An}	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Cn}

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC	UNIT
I _{CC}	MAX	63	21	109	57	0.1	0.16	mA
I _{OH}	MAX	-0.8	-0.4	-1	-2	-4	-4	mA
I _{OL}	MAX	16	8	20	20	4	4	mA

SWITCHING CHARACTERISTICS

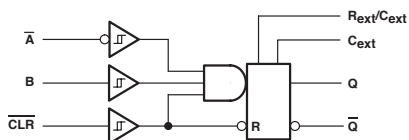
PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	S	AS	SN74 HC	CD74 HC
f _{max}				MIN	30	30	70	70	25	20
t _w	CLOCK			MIN	16	16	7	4	20	24
	CLEAR				12	12	12	7.2	20	24
t _{su}	Shift / Load			MIN	25	25	11	8	25	30
	Serial & Parallel Data				20	15	5	3.5	25	30
	Clear Inactive Data				25	25	9	6	25	30
TRELEASE				MAX	10	20	6	-	-	-
t _h				MIN	0	0	3	1	0	-
t _{PHL}		CLEAR	Q _A , Q _D	MAX	30	30	18.5	11.5	38	45
t _{PLH}		CLOCK		MAX	22	22	12	8.5	36	53
t _{PHL}					26	26	16.5	10.5	36	53

UNIT f_{max} : MHz, other : ns

DUAL MONOSTABLE MULTIVIBRATORS

- Overriding Clear Terminates Outputs Pulse

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
CLEAR	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L†	H†
X	X	L	L†	H†
H	L	↑		
H	↓	H		
↑	L	H		

See explanation of function table on page

† These lines of the functional tables assume that the indicated steady-state conditions at the A and B inputs have been set up long enough to complete any pulse started before the set up.

RECOMMENDED OPERATING CONDITIONS

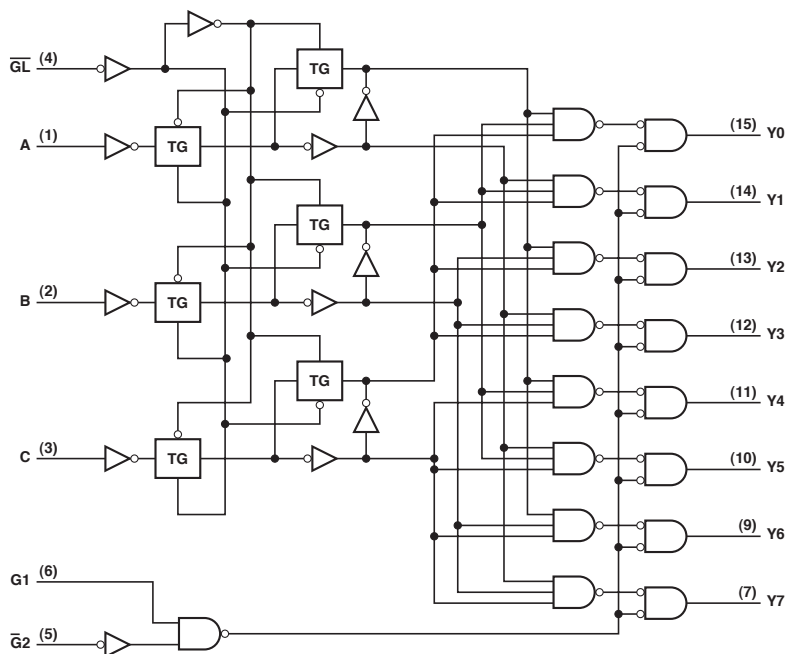
PARAMETER	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I _{CC}	MAX	80	27	0.16	0.16	0.28	0.65	mA
I _{OH}	MAX	-0.8	-0.4	-4	-4	-6	-12	mA
I _{OL}	MAX	16	8	4	4	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	CD74 HC	CD74 HCT	LV 3V	LV 5V
t _{PLH}	A (HC, LV: \bar{A})	Q	MAX	70	70	63	63	27.5	16
	B			55	55	63	63	27.5	16
t _{PHL}	A (HC, LV: \bar{A})	\bar{Q}	MAX	80	80	51	51	27.5	16
	B			65	65	51	51	27.5	16
t _{PHL}	Clear	Q	MAX	27	55	48	57	22	13
t _{PLH}		\bar{Q}		40	65	54	56	22	13

UNIT: ns

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUTS								
LE	OE0	OE1	A2	A1	A0	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
X	X	H	X	X	X	L	L	L	L	L	L	L	L
X	L	X	X	X	X	L	L	L	L	L	L	L	L
L	H	L	L	L	L	H	L	L	L	L	L	L	L
L	H	L	L	L	H	L	H	L	L	L	L	L	L
L	H	L	L	H	L	L	L	H	L	L	L	L	L
L	H	L	L	H	H	L	L	L	L	H	L	L	L
L	H	L	H	H	H	L	L	L	L	L	L	H	L
L	H	L	H	H	H	L	L	L	L	L	L	L	H
H	H	L	X	X	X	Depends upon the address previously applied while LE was at a logic low.							

RECOMMENDED OPERATING CONDITIONS

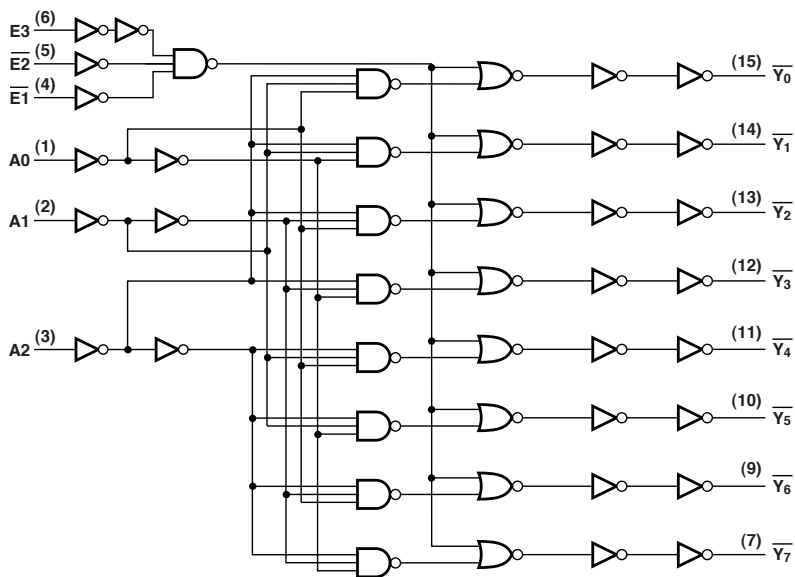
PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	0.08	0.16	0.16	mA
I _{DH}	MAX	-4	-4	-4	mA
I _{OL}	MAX	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
t _w	LE Pulse Width		MIN	20	15	15
t _{su}	An to LE		MIN	19	15	15
t _h	An to LE		MIN	5	9	5
t _{PLH}	An	Y	MAX	48	48	57
t _{PHL}				48	48	57
t _{PLH}	OE	Y	MAX	44	44	60
t _{PHL}				44	44	60

UNIT:ns

Logic Diagram



FUNCTION TABLE

INPUTS						OUTPUTS							
ENABLE			ADDRESS			Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
E3	E2	E1	A2	A1	A0								
X	X	H	X	X	X	L	L	L	L	L	L	L	L
L	X	X	X	X	X	L	L	L	L	L	L	L	L
X	H	X	X	X	X	L	L	L	L	L	L	L	L
H	L	L	L	L	L	H	L	L	L	L	L	L	L
H	L	L	L	L	H	L	H	L	L	L	L	L	L
H	L	L	L	H	L	L	L	H	L	L	L	L	L
H	L	L	L	H	H	L	L	L	H	L	L	L	L
H	L	L	H	L	L	L	L	L	L	H	L	L	L
H	L	L	H	H	L	L	L	L	L	L	H	L	L
H	L	L	H	H	H	L	L	L	L	L	L	H	L
H	L	L	H	H	H	L	L	L	L	L	L	L	H

Note: H = High Voltage Level, L = Low Voltage Level, X = Don't Care

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I _{CC}	MAX	0.16	0.16	0.16	0.16	mA
I _{DH}	MAX	-4	-4	-24	-24	mA
I _{OL}	MAX	4	4	24	24	mA

SWITCHING CHARACTERISTICS

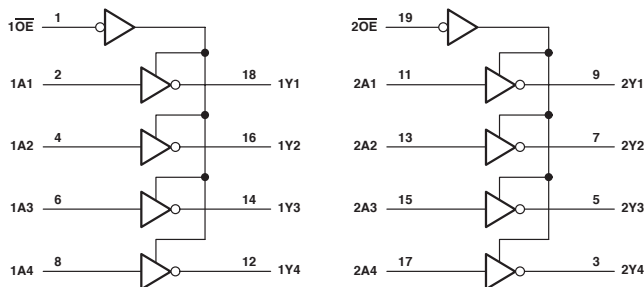
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
t _{PLH}	Address	Y	MAX	45	53	15	15
t _{PHL}				45	53	15	15
t _{PLH}	E1, E2	Y	MAX	-	-	11.9	11.9
t _{PHL}				-	-	11.9	11.9
t _{PLH}	E3	Y	MAX	-	-	16.6	16.6
t _{PHL}				-	-	16.6	16.6

UNIT:ns

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	ALS A-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVT 3V	UNIT
ICCH	MAX	27	135	11	11	17	29	0.08	0.16	0.08	0.16	31	0.25	0.19	mA
ICCL	MAX	44	150	23	23	75	75	0.08	0.16	0.08	0.16	71	30	5	mA
ICCZ	MAX	50	150	25	25	38	63	0.08	0.16	0.08	0.16	9	0.25	0.19	mA
I _{OH}	MAX	-15	-15	-15	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	mA
I _{OL}	MAX	24	64	24	48	64	64	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	LVCZ 3V	UNIT
ICCH	MAX	0.19	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.1	mA
ICCL	MAX	5	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.1	mA
ICCZ	MAX	0.19	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.1	mA
I _{OH}	MAX	-32	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	mA
I _{OL}	MAX	64	24	24	24	24	24	24	8	8	8	16	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	ALS A-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVT 3V
t _{PLH}	A	Y	MAX	14	7	9	9	6.5	8	25	30	32	33	5.6	4.8	3.8
				18	7	9	9	6.5	5.7	25	30	32	33	4	4.8	4
t _{PZH}	\overline{G}	Y	MAX	23	10	13	13	6.4	6.1	38	-	44	-	8.8	5.2	4.6
				30	15	18	18	9	10	38	-	44	-	10.5	6.2	4.4
t _{PZL}	\overline{G}	Y	MAX	25	9	10	10	5	6.3	38	-	44	-	8.1	6.4	4.4
				20	15	12	12	9.5	9.5	38	-	44	-	9.5	5.8	4.3

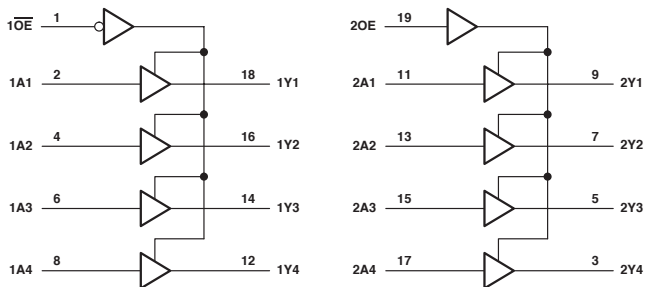
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	LVCZ 3V
t _{PLH}	A	Y	MAX	3.8	8.4	7	7.2	10.6	9.5	8.6	8.5	9.5	12.5	8.5	6.5	6.5
				4	7.2	6.5	7.2	8.7	8.5	8.6	8.5	9.5	12.5	8.5	6.5	6.5
t _{PZH}	\overline{G}	Y	MAX	4.6	9.2	8	12	12.5	9.5	13.4	10.5	13	16	10.5	8	8
				4.4	8.7	8.5	12	12.3	10.5	13.4	10.5	13	16	10.5	8	8
t _{PZL}	\overline{G}	Y	MAX	4.4	6.6	9.5	12	10	10.5	13.4	10.5	13	17	15.5	7	7
				4.3	7.7	9.5	12	10.8	10.5	13.4	10.5	13	17	15.5	7	7

UNIT: ns

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	ABT	LVTH 3V	SN74 AC	UNIT
ICCH	MAX	27	160	18	35	60	0.08	0.16	0.16	43	0.25	0.19	0.04	mA
ICCL	MAX	46	180	26	90	90	0.08	0.16	0.16	85	30	5	0.04	mA
ICCZ	MAX	54	180	30	56	90	0.08	0.16	0.16	10	0.25	0.19	0.04	mA
I _{OH}	MAX	-15	-15	-15	-15	-15	-6	-6	-6	-15	-32	-32	-24	mA
I _{OL}	MAX	24	64	24	64	64	6	6	6	64	64	64	24	mA

PARAMETER	MAX or MIN	SN74 ACT	CD74 ACT	UNIT
ICCH	MAX	0.04	0.16	mA
ICCL	MAX	0.04	0.16	mA
ICCZ	MAX	0.04	0.16	mA
I _{OH}	MAX	-24	-24	mA
I _{OL}	MAX	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 BCT	ABT	LVTH 3V	SN74 AC
t _{PLH}	A	Y	MAX	18	9	11	6.2	6.2	29	33	38	4.9	4.6	3.5	7.5
				18	9	10	6.2	6.5	29	33	38	5.9	4.6	3.4	7.5
t _{PZH}	$\overline{1G}$	Y	MAX	23	12	21	9	6.7	38	-	-	8.7	6.8	4.5	9.5
				30	15	21	7.5	8	38	-	-	9.4	6.8	4.4	9.5
t _{PHZ}	$\overline{1G}$	Y	MAX	25	9	10	6	7	38	-	-	8.1	7.1	4.5	10.5
				20	15	15	9	7	38	-	-	9.9	5.9	4.7	10.5
t _{PZH}	2G	Y	MAX	23	12	21	10.5	6.7	38	-	-	8.7	6.8	4.5	9.5
				30	15	21	8.5	8	38	-	-	9.4	6.8	4.4	9.5
t _{PHZ}	2G	Y	MAX	25	9	10	7	7	38	-	-	8.1	7.1	4.5	10.5
				20	15	15	12	7	38	-	-	9.9	5.9	4.7	10.5

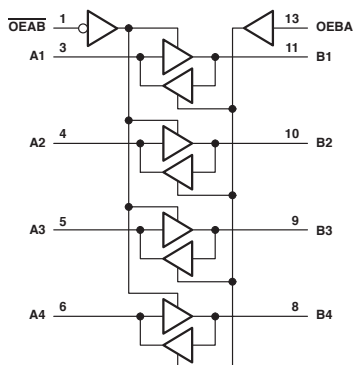
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 ACT	CD74 ACT
t _{PLH}	A	Y	MAX	9.5	9.6
				8.5	9.6
t _{PZH}	$\overline{1G}$	Y	MAX	9.5	13.4
				10.5	13.4
t _{PHZ}	$\overline{1G}$	Y	MAX	10.5	13.4
				10.5	13.4
t _{PZH}	2G	Y	MAX	9.5	13.4
				10.5	13.4
t _{PHZ}	2G	Y	MAX	10.5	13.4
				10.5	13.4

UNIT: ns

QUADRUPLE BUS TRANSCEIVERS

- Two-Way Asynchronous Communication Between Data Buses
- PNP Inputs Reduce DC Loading

Logic Diagram



FUNCTION TABLE

INPUTS		OPERATION
$\bar{G}AB$	$G\bar{B}A$	
L	L	A to B
H	H	B to A
H	L	Isolation
L	H	Latch A and B (A = B)

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CCH}	MAX	38	25	44	0.08	0.16	0.16	mA
I_{CCL}	MAX	50	30	74	0.08	0.16	0.16	mA
I_{CCZ}	MAX	54	32	56	0.08	0.16	0.16	mA
I_{QH}	MAX	-15	-15	-	-	-6	-6	mA
I_{QL}	MAX	24	24	64	6	6	6	mA

SWITCHING CHARACTERISTICS

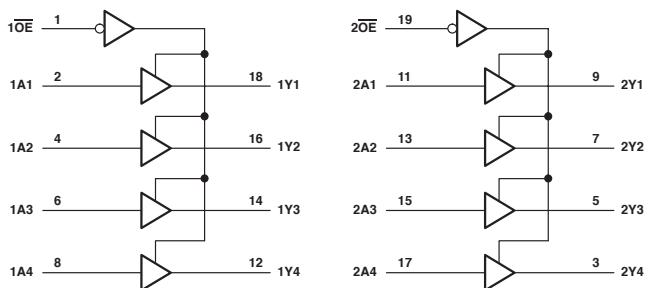
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A or B	A or B	MAX	18	11	7.5	25	27	33
t_{PHL}	A or B	A or B	MAX	18	11	6.5	25	27	33
t_{PZH}	$\bar{G}AB$	B	MAX	23	20	9	38	45	51
t_{PZL}				30	20	7.5	38	45	51
t_{PHZ}	$\bar{G}AB$	B	MAX	25	14	6.5	38	45	53
t_{PLZ}				20	22	9	38	45	53
t_{PZH}	GAB	A	MAX	23	20	10.5	38	45	51
t_{PZL}				30	20	8.5	38	45	51
t_{PHZ}	GAB	A	MAX	25	14	7	38	45	53
t_{PLZ}				20	22	11	38	45	53

UNIT: ns

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- PNP Inputs Reduce DC Loading
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	ALS C-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	LVT 3V	LVTH 3V	LVTT	LVTZ 3V	UNIT
ICCH	MAX	27	160	17	17	34	60	0.08	0.16	0.08	0.16	40	40	0.25	0.19	0.19	0.19	0.225	mA
ICCL	MAX	46	180	24	24	90	90	0.08	0.16	0.08	0.16	80	80	30	5	5	12	15	mA
ICCZ	MAX	54	180	27	27	54	90	0.08	0.16	0.08	0.16	10	10	0.25	0.19	0.19	0.19	0.225	mA
I _{OH}	MAX	-15	-15	-15	-15	-15	-15	-6	-6	-6	-6	-15	-15	-32	-32	-32	-32	-32	mA
I _{OL}	MAX	24	64	24	48	64	64	6	6	6	6	64	64	64	64	64	64	64	mA

PARAMETER	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V	UNIT
ICCH	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	0.1	0.01	0.01	mA
ICCL	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	0.1	0.01	0.01	mA
ICCZ	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	0.1	0.01	0.01	mA
I _{OH}	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	-24	-24	-24	mA
I _{OL}	MAX	24	24	24	24	24	24	8	8	8	16	24	24	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	ALS C-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT
I _{PLH}	A	Y	MAX	18	9	10	10	6.2	6.2	29	33	35	38	5	5.3	4.6
				18	9	10	10	6.2	6.5	29	33	35	38	5.5	6	4.6
I _{PZH}	\bar{G}	Y	MAX	23	12	20	20	9	6.7	38	-	44	-	8.7	9	5.1
				30	15	20	20	7.5	8	38	-	44	-	8.9	9.4	6.1
I _{PHZ}	\bar{G}	Y	MAX	25	9	10	10	6	7	38	-	44	-	7.7	8	6.6
				20	15	13	13	9	7	38	-	44	-	8.9	9.8	5.7

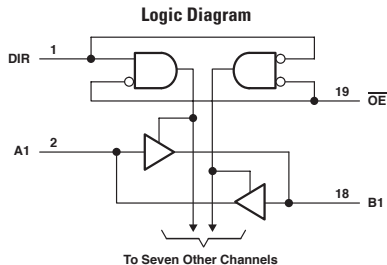
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT 3V	LVTH 3V	LVTT	LVTZ 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V
I _{PLH}	A	Y	MAX	3.5	3.5	4.1	4.1	7.3	7.5	8.2	9.9	10	9.6	8.5	9.5	13.5
				3.3	3.3	4.1	4.1	6.9	7.5	8.2	9.2	10	9.6	8.5	9.5	13.5
I _{PZH}	\bar{G}	Y	MAX	4.5	4.5	5.2	5.2	8.5	8	12	12.5	9.5	13.4	10.5	13	16
				4.4	4.4	5.2	5.2	8.5	8.5	12	11.4	10.5	13.4	10.5	13	16
I _{PHZ}	\bar{G}	Y	MAX	4.4	4.4	5.6	5.6	7.3	9.5	12	10.4	10.5	13.4	10.5	13	18
				4.4	4.4	5.1	5.1	8.2	9.5	12	11.2	10.5	13.4	10.5	13	18

PARAMETER	INPUT	OUTPUT	MAX or MIN	LV 5V	LVC 3V	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V
I _{PLH}	A	Y	MAX	8.5	5.9	5.9	5.9	2.8	2.8
				8.5	5.9	5.9	5.9	2.8	2.8
I _{PZH}	\bar{G}	Y	MAX	10.5	7.6	7.6	7.6	4.5	4.5
				10.5	7.6	7.6	7.6	4.5	4.5
I _{PHZ}	\bar{G}	Y	MAX	15.5	6.5	5.8	6.5	4.2	4.2
				15.5	6.5	5.8	6.5	4.2	4.2

UNIT: ns

OCTAL BUS TRANSCEIVERS

- 3-State Outputs Drive Bus Lines Directly
- PNP Inputs Reduce DC Loading on Bus Lines
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



FUNCTION TABLE

ENABLE G	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS C-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	ABTH	LVT 3V	LVTH 3V	LVTR 3V	UNIT
I _{CCH}	MAX	70	45	45	97	90	0.08	0.16	0.08	0.16	57	57	0.25	0.25	0.19	0.19	0.19	mA
I _{CCL}	MAX	90	55	55	143	120	0.08	0.16	0.08	0.16	90	90	30	30	5	5	12	mA
I _{CCZ}	MAX	95	58	58	123	110	0.08	0.16	0.08	0.16	15	15	0.25	0.25	0.19	0.19	0.19	mA
I _{OH} (A port)	MAX	-15	-15	-15	-15	-3	-6	-4	-6	-4	-3	-3	-32	-32	-32	-32	-32	mA
I _{OH} (B port)	MAX	-15	-15	-15	-15	-15	6	-4	-6	-4	-15	-15	-32	-32	-32	-32	-32	mA
I _{OL} (A port)	MAX	24	24	48	64	24	-6	4	6	4	24	24	64	64	64	64	32	mA
I _{OL} (B port)	MAX	24	24	48	64	64	6	4	6	4	64	64	64	64	64	64	32	mA

PARAMETER	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	LVCH 3V	LV CZ 3V	ALVC 3V	ALVCH 3V	UNIT
I _{CCH}	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	0.1	0.01	0.01	mA
I _{CCL}	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	0.1	0.01	0.01	mA
I _{CCZ}	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	0.1	0.01	0.01	mA
I _{OH} (A port)	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	-24	-24	-24	mA
I _{OH} (B port)	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	-24	-24	-24	mA
I _{OL} (A port)	MAX	24	24	24	24	24	24	8	8	8	16	24	24	24	24	24	mA
I _{OL} (B port)	MAX	24	24	24	24	24	24	8	8	8	16	24	24	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS C-1	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	SN64 BCT	ABT	ABTH
t_{PLH}	A, B	B, A	MAX	12	10	10	7.5	7	26	33	28	39	7	7	3.6	3.6
t_{PHL}				12	10	10	7	7	26	33	28	39	7	7	3.9	3.9
t_{PZH}	\bar{G}	A, B	MAX	40	20	20	9	8	58	45	58	48	10.9	10.9	5.6	5.6
t_{PZL}				40	20	20	8.5	9	58	45	58	48	11.6	11.6	6.2	6.2
t_{PHZ}	\bar{G}	A, B	MAX	28	10	10	5.5	7.5	50	45	50	45	9.3	9.3	5.9	5.9
t_{PLZ}				25	15	15	9.5	7.5	50	45	50	45	9.1	9.1	4.5	4.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT 3V	LVTH 3V	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t_{PLH}	A, B	B, A	MAX	3.5	3.5	9.5	7	8.5	10	8	10	8.5	9.5	13.5	8.5	6.3
t_{PHL}				3.5	3.5	6.9	7	8.5	9.1	9	10	8.5	9.5	13.5	8.5	6.3
t_{PZH}	\bar{G}	A, B	MAX	5.5	5.5	11.4	9	14	13.2	11	14	12	16	19	12	8.5
t_{PZL}				5.5	5.5	9.5	9.5	14	12.9	12	14	12	16	19	12	8.5
t_{PHZ}	\bar{G}	A, B	MAX	5.9	5.9	9.5	10	14	12.9	11	14.4	11	16.5	22	16	7.5
t_{PLZ}				5	5	10.4	10	14	13.9	11	14.4	11	16.5	22	16	7.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V
t_{PLH}	A, B	B, A	MAX	6.3	6.3	3.4	3.4
t_{PHL}				6.3	6.3	3.4	3.4
t_{PZH}	\bar{G}	A, B	MAX	8.5	8.5	5.5	5.5
t_{PZL}				8.5	8.5	5.5	5.5
t_{PHZ}	\bar{G}	A, B	MAX	7.5	7.5	5.5	5.5
t_{PLZ}				7.5	7.5	5.5	5.5

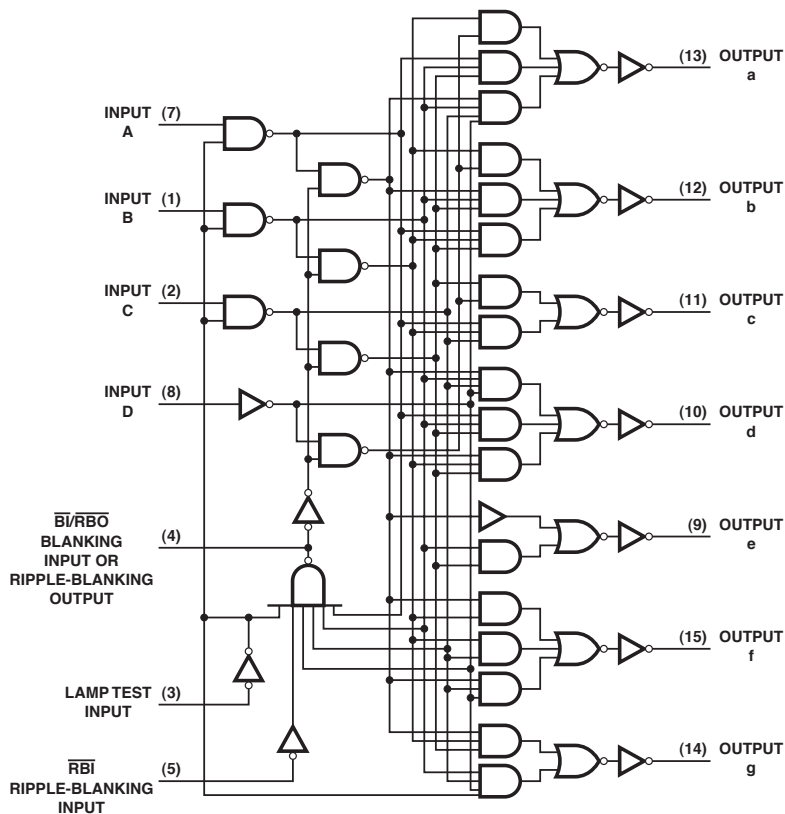
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTR 3V
t_{PLH}	A	B	MAX	4.2
	B	A		4.4
t_{PHL}	A	B	MAX	4.6
	B	A		4.1
t_{PZH}	\bar{G}	B	MAX	5.5
		A		6
t_{PZL}	\bar{G}	B	MAX	6.6
		A		6.4
t_{PHZ}	\bar{G}	B	MAX	6.1
		A		5.8
t_{PLZ}	\bar{G}	B	MAX	5.2
		A		5.2

UNIT: ns

BCD-TO-SEVEN-SEGMENT DECODERS/DRIVERS WITH RIPPLE BLANKING

- Open-Collector Outputs Drive Indicators Directly
- Lamp-Test Provision
- Leading/Trailing Zero Suppression

Logic Diagram



FUNCTION TABLE

DECIMAL OR FUNCTION	INPUTS					$\overline{\text{BI/RBO}}$	OUTPUTS							
	$\overline{\text{LT}}$	$\overline{\text{RBI}}$	D	C	B		A	a	b	c	d	e	f	g
0	H	H	L	L	L	L	H	ON	ON	ON	ON	ON	ON	OFF
1	H	X	L	L	L	H	H	OFF	ON	ON	OFF	OFF	OFF	OFF
2	H	X	L	L	H	L	H	ON	ON	ON	OFF	ON	OFF	ON
3	H	X	L	L	H	H	H	ON	ON	ON	ON	ON	OFF	ON
4	H	X	L	H	L	L	H	OFF	ON	ON	OFF	OFF	ON	ON
5	H	X	L	H	L	H	H	ON	OFF	ON	ON	OFF	ON	ON
6	H	X	L	H	H	L	H	ON	OFF	ON	ON	ON	ON	ON
7	H	X	L	H	H	H	H	ON	ON	ON	OFF	OFF	OFF	OFF
8	H	X	H	L	L	L	H	ON	ON	ON	ON	ON	ON	ON
9	H	X	H	L	L	H	H	ON	ON	ON	ON	ON	OFF	ON
10	H	X	H	L	H	L	H	OFF	OFF	OFF	ON	ON	OFF	ON
11	H	X	H	L	H	H	H	OFF	OFF	OFF	ON	OFF	OFF	ON
12	H	X	H	H	L	L	H	OFF	ON	OFF	OFF	OFF	ON	ON
13	H	X	H	H	L	H	H	ON	OFF	OFF	ON	OFF	ON	ON
14	H	X	H	H	H	L	H	OFF	OFF	OFF	ON	ON	ON	ON
15	H	X	H	H	H	H	H	OFF	OFF	OFF	OFF	OFF	OFF	OFF
BI	X	X	X	X	X	X	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
RBI	H	L	L	L	L	L	L	OFF	OFF	OFF	OFF	OFF	OFF	OFF
LT	L	X	X	X	X	X	H	ON	ON	ON	ON	ON	ON	ON

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	103	13	mA
$V_o(\text{off})$	MAX	15	15	V
$I_o(\text{on})$	MAX	40	24	mA
I_{OH}	MAX	-0.2	-0.05	mA
I_{OL}	MAX	8	3.2	mA

SWITCHING CHARACTERISTICS

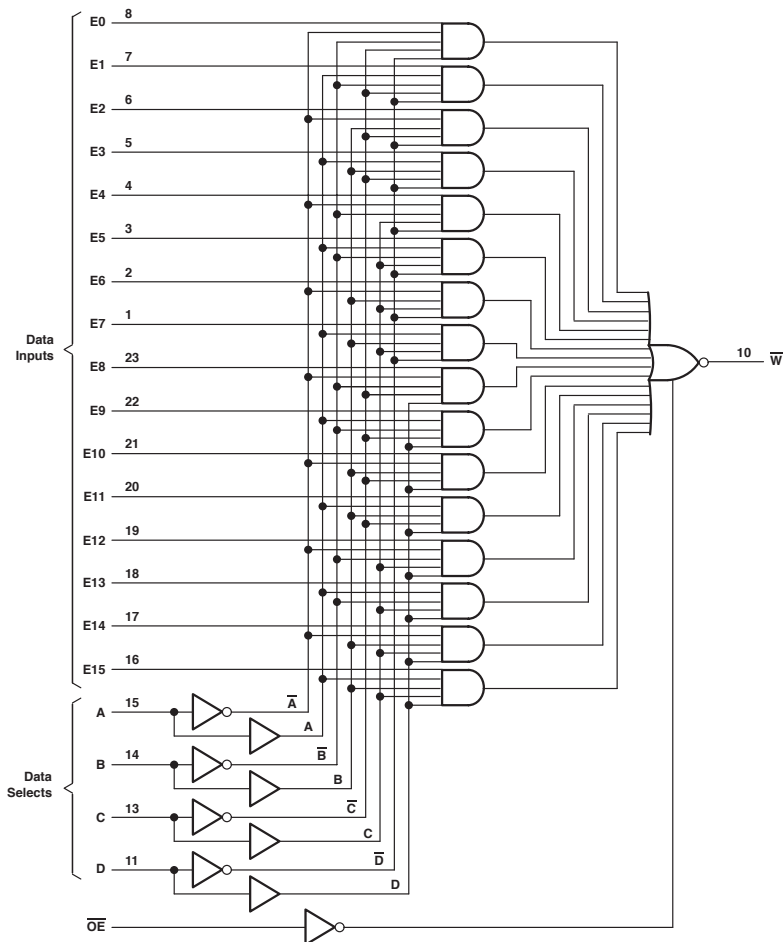
PARAMETER	MAX or MIN	TTL	LS
t_{off}	INPUT A	MIN	100
t_{on}		100	
t_{off}	INPUT $\overline{\text{RBI}}$	MIN	100
t_{on}		100	

UNIT: ns

1-OF-16 DATA SELECTOR/MULTIPLEXER

- 4-Line to 1-Line Multiplexers That Can Select 1-of-16 Data Inputs
- Applications:
 - Boolean Function Generator
 - Parallel-to-Serial Converter
 - Data Source Selector
- Buffered 3-State Bus Driver Inputs Permit Multiplexing From n Lines to One Line
- 3-State Outputs

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT	
\bar{G}	A	B	C	D	Ei	\bar{W}
L	L	L	L	L	E0	E0
L	H	L	L	L	E1	E1
L	L	H	L	L	E2	E2
L	H	H	L	L	E3	E3
L	L	L	H	L	E4	E4
L	H	L	H	L	E5	E5
L	L	H	H	L	E6	E6
L	H	H	H	L	E7	E7
L	L	L	L	H	E8	E8
L	H	L	L	H	E9	E9
L	L	H	L	H	E10	E10
L	H	H	L	H	E11	E11
L	L	L	H	H	E12	E12
L	H	L	H	H	E13	E13
L	L	H	H	H	E14	E14
L	H	H	H	H	E15	E15
H	X	X	X	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	UNIT
I _{CC}	MAX	50	mA
I _{DH}	MAX	-15	mA
I _{DL}	MAX	48	mA

SWITCHING CHARACTERISTICS

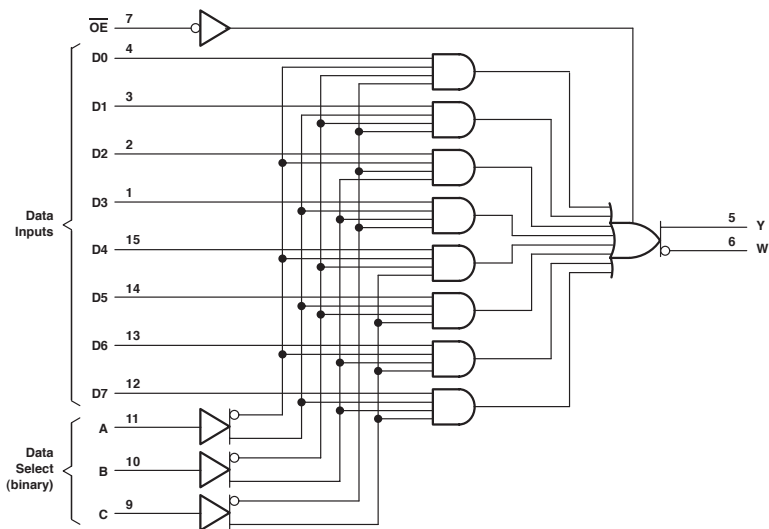
PARAMETER	INPUT	OUTPUT	MAX or MIN	AS
t _{PLH}	DATA	\bar{W}	MAX	8
t _{PHL}				7
t _{PLH}	SELECT	\bar{W}	MAX	13
t _{PHL}				10.5
t _{PZH}	\bar{G}	\bar{W}	MAX	7
t _{PZL}				9
t _{PHZ}	\bar{G}	\bar{W}	MAX	6
t _{PLZ}				6.5

UNIT: ns

DATA SELECTORS/MULTIPLEXERS

- 3-State Version of '151
- 3-State Outputs Interface Directly with System Bus
- Perform Parallel-to-Serial Conversion
- Complementary Outputs Provide True and Inverted Data

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUTS	
SELECT			STROBE	Y	W
C	B	A	G		
X	X	X	H	Z	Z
L	L	L	L	D0	D0
L	L	H	L	D1	D1
L	H	L	L	D2	D2
L	H	H	L	D3	D3
H	L	L	L	D4	D4
H	L	H	L	D5	D5
H	H	L	L	D6	D6
H	H	H	L	D7	D7

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 AC	CD74 AC	UNIT
I _{CC}	MAX	62	12	85	14	24	0.08	0.16	0.16	0.16	0.16	mA
I _{OH}	MAX	-5.2	-2.6	-6.5	-2.6	-3	-6	-4	-4	-24	-24	mA
I _{OL}	MAX	16	8	20	24	24	6	4	4	24	24	mA

SWITCHING CHARACTERISTICS

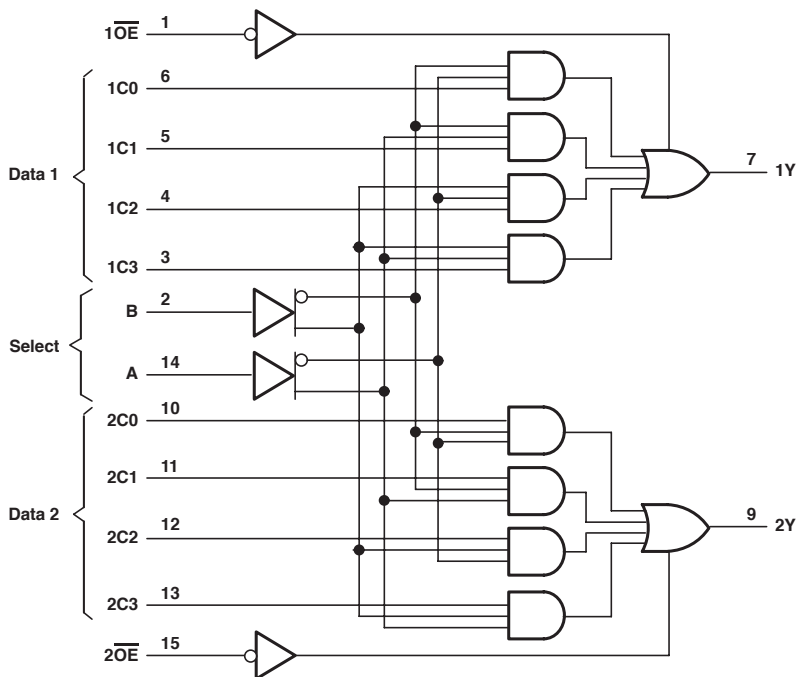
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	ALS	F	SN74 HC	CD74 HC	CD74 HCT	SN74 AC	CD74 AC
t _{PLH}	A, B, C	Y	MAX	45	45	18	18	9.5	51	74	63	18.2	18.2
t _{PHL}				45	45	19.5	24	7.5	51	74	63	18.2	18.2
t _{PLH}	A, B, C	W (CD74: \bar{Y})	MAX	33	33	15	24	12.5	51	74	63	19.6	19.6
t _{PHL}				33	33	13.5	23	9	51	74	63	19.6	19.6
t _{PLH}	ANY D	Y	MAX	28	28	12	10	7	49	53	53	13.5	13.5
t _{PHL}				28	28	12	15	5	49	53	53	13.5	13.5
t _{PLH}	ANY D	W (CD74: \bar{Y})	MAX	15	15	7	15	8	49	53	53	14.9	14.9
t _{PHL}				15	15	7	15	8	49	53	53	14.9	14.9
t _{PZH}	\bar{G}	Y	MAX	27	45	19.5	15	7	36	42	45	13.5	13.5
t _{PZL}				40	40	21	15	6.5	36	42	45	13.5	13.5
t _{PZH}	\bar{G}	W (CD74: \bar{Y})	MAX	27	27	19.5	15	6	36	42	45	13.5	13.5
t _{PZL}				40	40	21	15	4.5	36	42	45	13.5	13.5
t _{PHZ}	\bar{G}	Y	MAX	8	45	8.5	10	8.5	49	42	45	13.5	13.5
t _{PLZ}				23	25	14	10	8	49	42	45	13.5	13.5
t _{PHZ}	\bar{G}	W (CD74: \bar{Y})	MAX	8	55	8.5	10	5.5	49	42	45	13.5	13.5
t _{PLZ}				23	25	14	10	4.5	49	42	45	13.5	13.5

UNIT: ns

DUAL DATA SELECTORS/MULTIPLEXERS

- 3-State Version of '153
- Perform Parallel-to-Serial Conversion

Logic Diagram



FUNCTION TABLE

SELECT INPUTS		DATA INPUTS				OUTPUT CONTROL	OUTPUT
B	A	C0	C1	C2	C3	\bar{G}	Y
X	X	X	X	X	X	H	Z
L	L	L	X	X	X	L	L
L	L	H	X	X	X	L	H
L	H	X	L	X	X	L	L
L	H	X	H	X	X	L	H
H	L	X	X	L	X	L	L
H	L	X	X	H	X	L	H
H	H	X	X	X	L	L	L
H	H	X	X	X	H	L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I _{CC}	MAX	14	14	33	23	0.08	0.16	0.16	0.16	0.16	mA
I _{OH}	MAX	-2.6	-2.6	-15	-3	-6	-6	-4	-24	-24	mA
I _{OL}	MAX	8	24	48	24	6	6	4	24	24	mA

SWITCHING CHARACTERISTICS

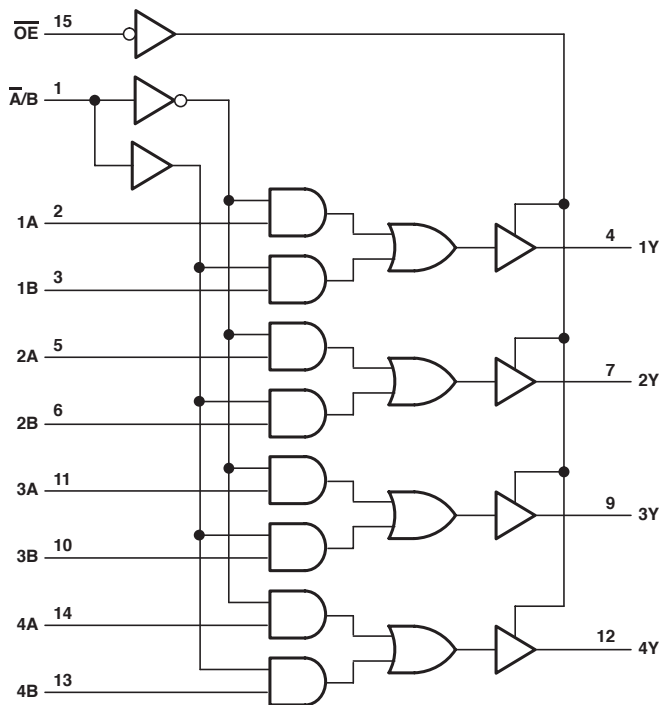
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
t _{PLH}	DATA	Y	MAX	25	10	7.5	8	35	53	57	13.3	18
t _{PHL}				20	14	8	7	35	53	57	13.3	18
t _{PLH}	SELECT	Y	MAX	45	21	13.5	13	38	53	60	20	22
t _{PHL}				32	21	11.5	10	38	53	60	20	22
t _{PZH}	\bar{G}	Y	MAX	28	14	12.5	9	25	33	45	11.5	12.6
t _{PZL}				23	16	11.5	9	25	33	45	11.5	12.6
t _{PHZ}	\bar{G}	Y	MAX	41	10	6	6	38	45	45	11.5	12.6
t _{PLZ}				27	14	7	7	38	45	45	11.5	12.6

UNIT: ns

QUAD DATA SELECTORS/MULTIPLEXERS

- 3-State Outputs Interface Directly with System Bus
- Provides Bus Interface from Multiple Sources in High-Performance Systems

Logic Diagram



FUNCTION TABLE

OUTPUT CONTROL	INPUTS				OUTPUT Y
	SELECT	A	B		
H	X	X	X	X	Z
L	L	L	X	X	L
L	L	H	X	X	H
L	H	X	X	L	L
L	H	X	H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V	UNIT
I _{CC}	MAX	19	87	14	31.9	23	0.08	0.16	0.08	0.16	0.08	0.16	0.08	0.16	0.01	mA
I _{OH}	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-6	-24	-24	-24	-24	-24	mA
I _{OL}	MAX	24	20	24	48	24	6	6	6	6	24	24	24	24	24	mA

SWITCHING CHARACTERISTICS

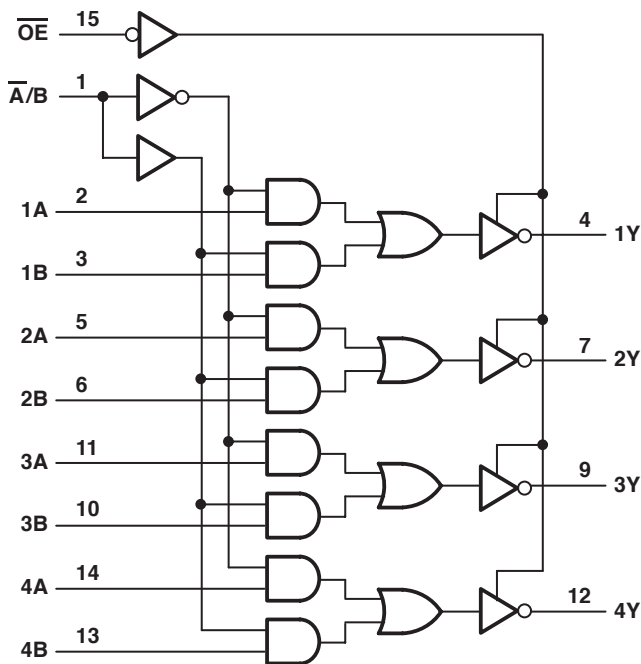
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V
t _{PLH}	DATA	ANY	MAX	13	7.5	10	5.5	7	25	45	38	50	6.4	9.3	6.9	10.7	4.6
				15	6.5	12	6	6.5	25	45	38	50	7.2	9.3	8.7	10.7	4.6
t _{PLH}	SELECT	ANY	MAX	21	15	18	11	15	25	53	38	57	7.2	13.4	8.2	15.4	6.4
				24	15	22	10	9.5	25	53	38	57	7.9	13.4	9.4	15.4	6.4
t _{PZH}	G	Y	MAX	30	19.5	16	7.5	8.5	38	45	38	45	6.5	14.7	7.3	16.1	5.6
t _{PZL}				30	21	18	9.5	8.5	38	45	38	45	8.6	14.7	9.6	16.1	5.6
t _{PHZ}	G	Y	MAX	30	8.5	10	6.5	7	38	45	38	45	7.6	14.7	8.4	16.1	4.3
t _{PLZ}				25	14	15	7	7	38	45	38	45	7.6	14.7	8.5	16.1	4.3

UNIT: ns

QUAD DATA SELECTORS/MULTIPLEXERS

- 3-State Outputs Interface Directly with System Bus
- Provides Bus Interface from Multiple Sources in High-Performance Systems

Logic Diagram



FUNCTION TABLE

OUTPUT CONTROL	INPUTS			OUTPUT
	SELECT	A	B	
H	X	X	X	Z
L	L	L	X	H
L	L	H	X	L
L	H	X	L	H
L	H	X	H	L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 ACT	UNIT
I _{CC}	MAX	16	87	13	25.2	23	0.08	0.16	0.16	0.16	mA
I _{OH}	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-24	mA
I _{OL}	MAX	8	20	24	48	24	6	6	6	24	mA

SWITCHING CHARACTERISTICS

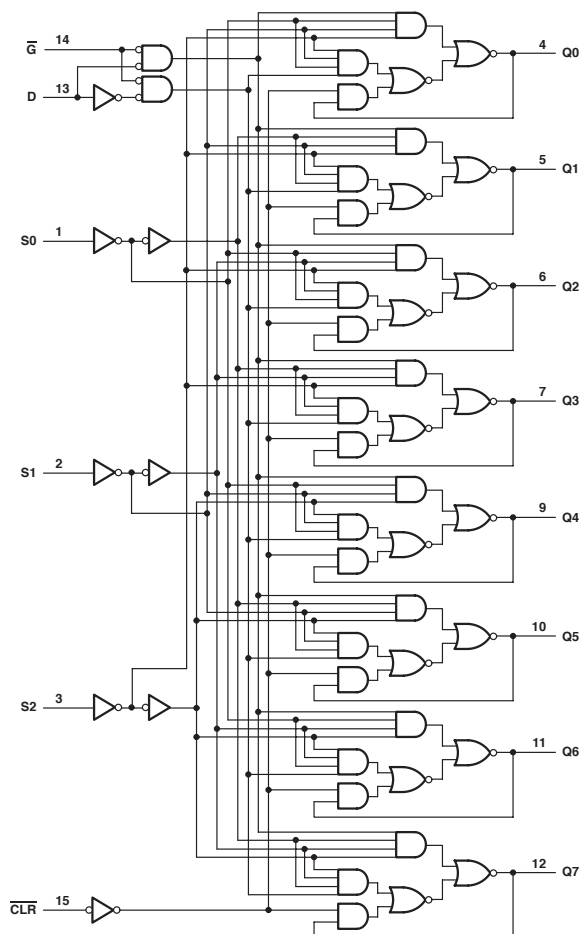
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 ACT
t _{PLH}	DATA	Y	MAX	12	6	8	5	6	25	24	34	10.7
				17	6	7	4	5.5	25	24	34	10.7
t _{PHL}	SELECT	Y	MAX	21	12	25	9.5	9.5	29	35	43	15.4
				24	12	20	10	11	29	35	43	15.4
t _{PZH}	\bar{G}	Y	MAX	30	19.5	18	8	8.5	38	35	35	16.1
				30	21	18	10	8.5	38	35	35	16.1
t _{PHZ}	\bar{G}	Y	MAX	30	8.5	10	6	7	38	38	38	16.1
				25	14	18	6.5	7	38	38	38	16.1

UNIT: ns

8-BIT ADDRESSABLE LATCHES

- 8-Bit Parallel-Out Storage Register Performs Serial-to-Parallel Conversion with Storage
- Asynchronous Parallel Clear
- Active-High Decoder
- Enable/Disable Input Simplifies Expansion
- Expandable for n-Bit Applications
- Four Distinct Functional Modes

Logic Diagram



LATCH SELECTION

SELECT INPUTS			LATCH ADDRESSED
C	B	A	
L	L	L	0
L	L	H	1
L	H	L	2
L	H	H	3
H	L	L	4
H	L	H	5
H	H	L	6
H	H	H	7

FUNCTION TABLE

INPUTS		OUTPUT OF ADDRESSED LATCH	EACH OTHER OUTPUT	FUNCTION
CLR	G			
H	L	D	Q ₀	Addressable latch Memory 8-line demultiplexer Clear
H	H	Q ₀	Q ₀	
L	L	D	L	
L	H	L	L	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	90	36	22	0.08	0.16	0.16	mA
I _{OH}	MAX	16	8	8	4	4	4	mA
I _{OL}	MAX	-0.8	-0.4	-0.4	-4	-4	-4	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	CD74 HCT
t _w	\bar{G}			MIN	15	17	15	20	21	27
	CLR				15	10	10	20	21	27
t _{su}	DATA			MIN	15	20	15	19	24	26
	ADDRESS				5	17	15	19	24	26
t _h	DATA			MIN	0	0	0	5	0	0
	ADDRESS				20	0	0	5	0	0
t _{PLH}	CLR	Any Q	MAX	25	18	12	38	47	59	
t _{PHL}	DATA	Any Q	MAX	24	30	19	33	56	59	
t _{PLH}	ADDRESS	Any Q	MAX	20	20	12	33	56	59	
t _{PHL}				28	27	22	50	56	61	
t _{PLH}				28	20	12	50	56	61	
t _{PHL}				20	24	20	43	51	57	
t _{PHL}	ENABLE	Any Q	MAX	20	24	13	43	51	57	

UNIT: ns

DUAL 5-INPUT POSITIVE-NOR GATES

$$\bullet \quad Y = \overline{A + B + C + D + E}$$

RECOMMENDED OPERATING CONDITIONS

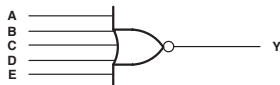
PARAMETER	MAX or MIN	S	F	UNIT
I_{CC}	MAX	45	9.5	mA
I_{OH}	MAX	-1	-1	mA
I_{OL}	MAX	20	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	S	F
t_{PLH}	A, B, C, D, E	Y	MAX	5.5	6.5
t_{PHL}				6	4.5

UNIT: ns

Logic Diagram



QUAD COMPLEMENTARY-OUTPUT ELEMENTS

- $Y = \bar{A}$, $W = A$
- $Y = AB$, $W = \bar{AB}$

ELEMENTS 1 and 4



ELEMENTS 2 and 3



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	34	mA
I_{OH}	MAX	-0.8	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
t_{PLH}	↕	↕	MAX	18
t_{PHL}	Y	Y	MAX	18
t_{PLH}	↕	↕	MAX	18
t_{PHL}	Y	Y	MAX	18
t_{PLH}	↕	↕ with respect Y	MAX	·3
$-t_{PHL}$	Y	↕ with respect Y	MAX	·3
t_{PHL}	↕	↕ with respect Y	MAX	·3
$-t_{PLH}$	Y	↕ with respect Y	MAX	·3

UNIT: ns

QUAD 2-INPUT EXCLUSIVE-NOR GATES WITH OPEN-COLLECTOR OUTPUTS

$$\bullet Y = \overline{A \oplus B}$$

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	HC	UNIT
I_{CC}	MAX	13	0.02	mA
V_{OH}	MAX	5.5	V_{CC}	V
I_{OL}	MAX	8	4	mA

SWITCHING CHARACTERISTICS

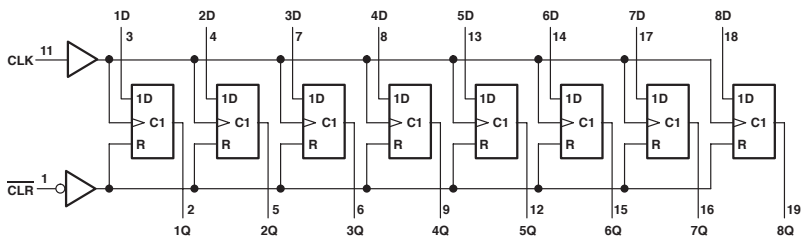
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
t_{PLH}	A or B Other Input Low	Y	MAX	30	31
t_{PHL}	A or B Other Input Low	Y	MAX	30	25
t_{PLH}	A or B Other Input High	Y	MAX	30	31
t_{PHL}	A or B Other Input High	Y	MAX	30	25

UNIT: ns

OCTAL D-TYPE FLIP-FLOPS

- Contain Eight Flip-Flops with Single-Rail Outputs
- Buffered Clock and Direct-Clear Inputs

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT Q
CLEAR	CLOCK	D	
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q ₀

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	LVTH 3V	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	UNIT
I _{CC}	MAX	94	27	29	0.08	0.16	0.08	0.16	30	5	0.16	0.16	0.04	0.04	-	0.02	mA
I _{OH}	MAX	-0.8	-0.4	-2.6	-4	-4	-4	-4	-32	-32	-24	-24	-8	-8	-6	-12	mA
I _{OL}	MAX	16	8	24	4	4	4	4	64	64	24	24	8	8	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	LVTH 3V	CD74 AC	CD74 ACT	AHC
f _{max}			MIN	30	30	35	21	20	16	16	150	150	100	85	70
t _r			MIN	16.5	20	14	20	24	25	30	3.3	3.3	5	6	5
t _{su}	DATA INPUT		MIN	20	20	10	25	18	25	18	2.5	2.3	2	2	4.5
	CLR INACTIVE		MIN	25	25	15	25	-	25	-	2	2.3	-	-	2
t _h			MIN	5	5	0	0	3	0	3	1.2	0	2	2	1
↑P _{HL}	CLEAR	ANY Q	MAX	27	27	18	40	45	42	48	7.4	4.9	13.5	13.5	12
↑P _{LH}				27	27	12	40	45	42	45	6.5	4.8	13.5	13.5	12.5
↑P _{HL}	CLOCK	ANY Q	MAX	27	27	15	40	45	42	45	7.3	4.3	13.5	13.5	12.5

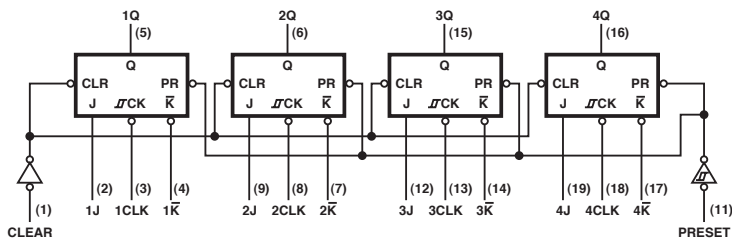
PARAMETER	INPUT	OUTPUT	MAX or MIN	AHCT	LV 3V	LV 5V
f _{max}			MIN	45	45	70
t _r			MIN	6.5	6.5	5
t _{su}	DATA INPUT		MIN	5	6.5	4.5
	CLR INACTIVE		MIN	2.5	2.5	2
t _h			MIN	0	2	1
↑P _{HL}	CLEAR	ANY Q	MAX	12.6	19.5	12
↑P _{LH}				9.8	19.5	12.5
↑P _{HL}	CLOCK	ANY Q	MAX	11	19.5	12.5

UNIT f_{max}: MHz, other: ns

QUAD J-K FLIP-FLOPS

- Separate Negative-Edge-Triggered Clocks
- Fully Buffered Outputs

Logic Diagram



FUNCTION TABLE

COMMON INPUTS		INPUTS			OUTPUT Q
PRESET	CLEAR	CLOCK	J	K	
L	H	X	X	X	H
H	L	X	X	X	L
L	L	X	X	X	H†
H	H	↓	L	H	Q ₀
H	H	↓	H	H	H
H	H	↓	L	L	L
H	H	↓	H	L	TOGGLE
H	H	H	X	X	Q ₀

† The output levels in this configuration are not guaranteed to meet the minimum levels for V_{OH} . Furthermore, this configuration is nonstable; that is, it will not persist when either PRE or CLR returns to its inactive (high) level.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	UNIT
I_{CC}	MAX	81	mA
I_{OH}	MAX	-0.8	mA
I_{OL}	MAX	16	mA

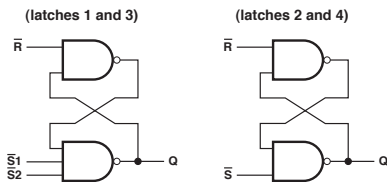
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL
f_{max}			MIN	35
t_w	CLOCK high		MIN	13.5
	CLOCK low		MIN	15
t_{su}	J, K		MIN	3
	CLR, PR		MIN	10
t_h			MIN	10
t_{PLH}	PRESET	Q	MAX	25
t_{PHL}	CLEAR	Q	MAX	30
t_{PLH}	CLOCK ↓	Q	MAX	30
t_{PHL}			MAX	30

UNIT f_{max} : MHz, other : ns

QUAD $\overline{S}\text{-}\overline{R}$ LATCHES

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I_{CC}	MAX	30	7	mA
I_{OH}	MAX	-0.8	-0.4	mA
I_{OL}	MAX	16	8	mA

SWITCHING CHARACTERISTICS

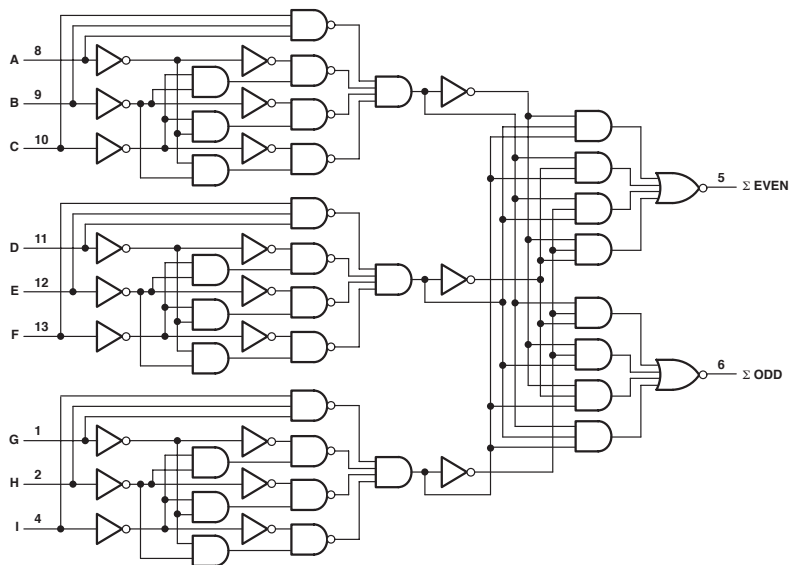
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
t_{\ast}			MIN	20	20
t_{PLH}	\overline{S}	Q	MAX	22	22
t_{PHL}				15	21
t_{PHL}	\overline{R}		MAX	27	27

UNIT: ns

9-BIT ODD/EVEN PARITY GENERATORS/CHECKERS

- Generate Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bit Parity

Logic Diagram



FUNCTION TABLE

NO. OF INPUTS A-1 THAT ARE HIGH	OUTPUTS	
	Σ EVEN	Σ ODD
0, 2, 4, 6, 8	H	L
1, 3, 5, 7, 9	L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I _{CC}	MAX	27	105	16	35	35	0.08	0.16	0.16	0.16	0.16	mA
I _{OH}	MAX	-0.4	-1	-2.6	-2	-1	-4	-4	-4	-24	-24	mA
I _{OL}	MAX	8	20	24	20	20	4	4	4	24	24	mA

SWITCHING CHARACTERISTICS

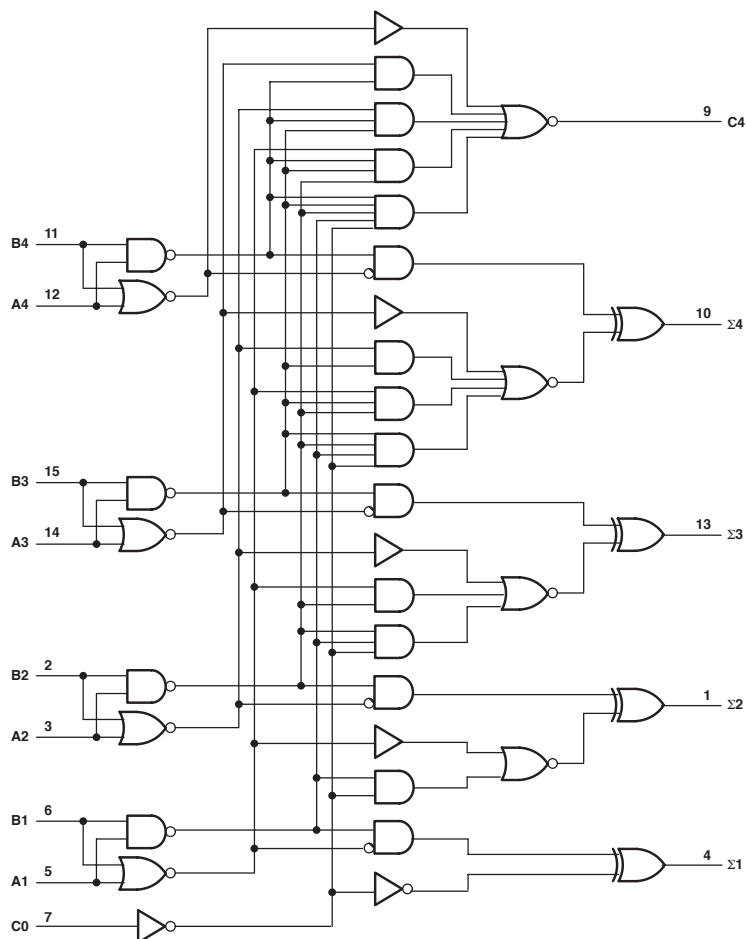
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
t _{PLH}	DATA	S EVEN	MAX	50	21	20	12	10	52	60	63	20	21.6
				45	18	20	11	11	52	60	63	20	21.6
t _{PLH}	DATA	S ODD	MAX	35	21	20	12	10	52	60	68	21	21.6
				50	18	22	11.5	11	52	60	68	21	21.6

UNIT: ns

4-BIT BINARY FULL ADDERS

- Full-Carry Look-Ahead Across the Four Bits

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUTS							
				WHEN C0 = L				WHEN C0 = H			
				WHEN C2 = L				WHEN C2 = H			
A1	B1	A2	B2	$\Sigma 1$	$\Sigma 2$	C2	$\Sigma 1$	$\Sigma 2$	C2		
A3	B3	A4	B4	$\Sigma 3$	$\Sigma 4$	C4	$\Sigma 3$	$\Sigma 4$	C4		
L	L	L	L	L	L	L	H	L	L		
H	L	L	L	L	H	L	L	L	H	L	
L	H	L	L	L	H	L	L	L	H	L	
H	H	L	L	L	L	H	L	H	H	L	
L	L	H	L	L	L	H	L	H	H	L	
H	L	H	L	L	H	H	L	L	L	H	
L	H	H	L	L	H	H	L	L	L	H	
H	L	H	L	L	L	L	H	H	L	H	
L	L	L	H	L	L	L	L	H	L	H	
H	L	L	H	H	H	L	L	H	L	H	
L	H	L	H	H	H	L	L	L	L	H	
H	H	L	H	L	L	L	H	H	L	H	
L	L	H	H	L	L	L	H	H	L	H	
H	L	H	H	H	L	H	L	H	H	H	
L	H	H	H	H	L	H	L	H	H	H	
H	H	H	H	L	H	H	H	H	H	H	

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	TTL	LS	S	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT
I _{CC}		MAX	110	39	160	55	0.16	0.16	0.16	0.16	mA
I _{OH}	Any output except C4	MAX	-0.8	-0.4	-1	-1	-4	-4	-24	-24	mA
	C4	MAX	-0.4	-0.4	-0.5	-1	-4	-4	-24	-24	
I _{OL}	Any output except C4	MAX	16	8	20	20	4	4	24	24	mA
	C4	MAX	8	8	10	20	4	4	24	24	

SWITCHING CHARACTERISTICS

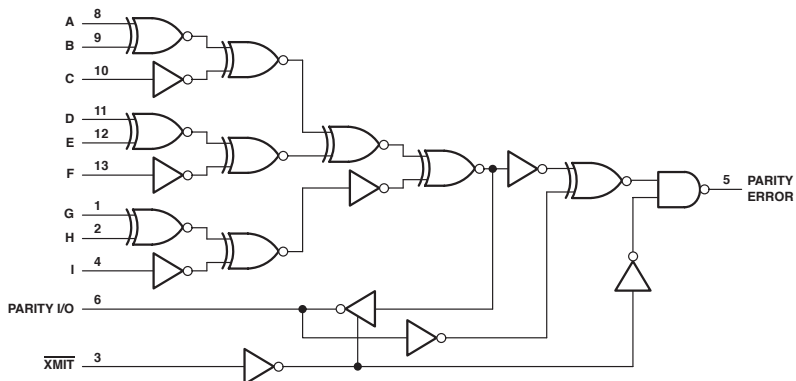
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	S	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
I _{PLH}	C0	S	MAX	21	24	18	10.5	69	47	17.6	17.6
			MIN	21	24	18	10.5	69	47	17.6	17.6
I _{PHL}	A _i or B _i	S _i	MAX	24	24	18	10.5	63	69	18.2	18.2
			MIN	24	24	18	10.5	63	69	18.2	18.2
I _{PLH}	C0	C4	MAX	14	17	11	8.5	59	80	17.6	17.6
			MIN	16	22	11	8	59	80	17.6	17.6
I _{PHL}	A _i or B _i	C4	MAX	14	17	12	8.5	59	72	17.6	17.6
			MIN	16	17	12	8	59	72	17.6	17.6

UNIT: ns

9-BIT PARITY GENERATOR/CHECKER WITH BUS DRIVER PARITY I/O PORT

- Generate Either Odd or Even Parity for Nine Data Lines
- Cascadable for n-Bit Parity
- Direct Bus Connection for Parity Generation or Checking by Using the Parity I/O Port
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

NUMBER OF INPUTS (A-I) THAT ARE HIGH	$\overline{\text{XMIT}}$	PARITY I/O	PARITY ERROR
0, 2, 4, 6, 8	l	H	H
1, 3, 5, 7, 9	l	L	H
0, 2, 4, 6, 8	h	h	H
	h	l	L
1, 3, 5, 7, 9	h	h	L
	h	l	H

h = high input level l = low input level
H = high output level L = low output level

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	AS	AC 11	ACT 11	UNIT
I _{CC}		MAX	50	0.08	0.08	mA
I _{OH}	Parity error	MAX	-2	-24	-24	mA
	Parity I/O	MAX	-15	-24	-24	mA
I _{OL}	Parity error	MAX	20	24	24	mA
	Parity I/O	MAX	48	24	24	mA

SWITCHING CHARACTERISTICS

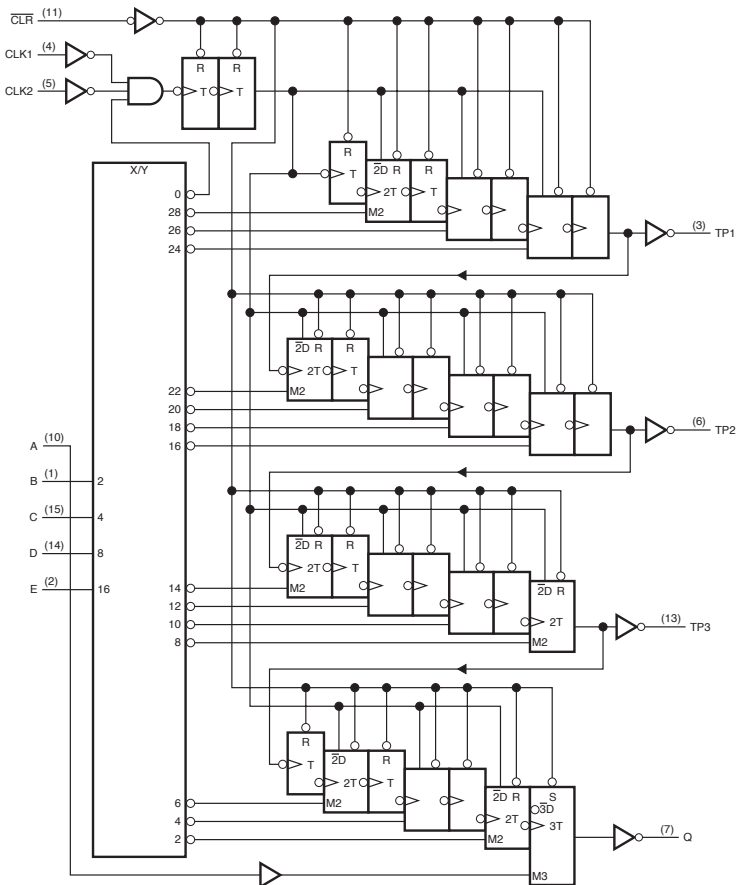
PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	AC 11	ACT 11	
I _{PLH}	A to l	Parity I/O	MAX		15	9	10.4
					14	10.7	12
I _{PHL}	A to l	Parity error	MAX		16.5	10	11.3
					16.5	12	12.9
I _{PLH}	Parity I/O	Parity error	MAX		9	6.2	7.7
					9	7.9	9.1
I _{PZH}	$\overline{\text{XMIT}}$	Parity I/O	MAX		13	5.3	7.3
					16	8.9	11.4
I _{PHZ}	$\overline{\text{XMIT}}$	Parity I/O	MAX		11.5	6.5	8.5
					10	6.3	7.8

UNIT: ns

PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMER

- Digitally Programmable from 2^2 to 2^{31}
- Easily Expandable
- Applications:
 Frequency Division
 Digital Timing

Logic Diagram



FUNCTION TABLE

CLEAR	CLK 1	CLK 2	Q OUTPUT MODE
L	X	X	Cleared to L
H	ns	L	Count
H	L	ns	Count
H	H	X	Inhibit
H	X	H	Inhibit

RECOMMENDED OPERATING CONDITIONS

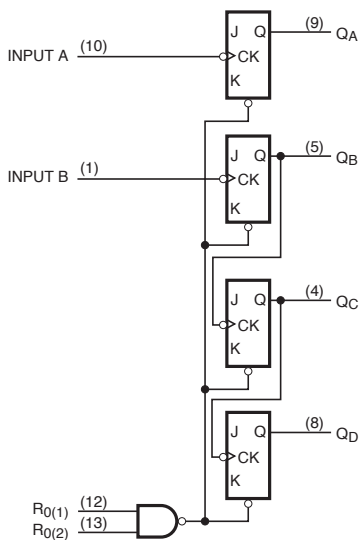
PARAMETER	MAX or MIN	LS	UNIT
I _{CC}	MAX	75	mA
I _{OH} (Q only)	MAX	-1.2	V
I _{OL} (Q only)	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
f _{max}	CLK		MIN	30
t _{PLH}	CLK	Q	MAX	90
t _{PHL}	CLK	Q	MAX	120
t _{PHL}	CLR	Q	MAX	65

 UNIT f_{max} : ns, Hz, other : ns

Logic Diagram



COUNT SEQUENCE

COUNT	OUTPUTS			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

NOTE: Output Q_A is connected to input B.

RESET/COUNT FUNCTION TABLE

RESET INPUTS		OUTPUTS			
R ₀ (1)	R ₀ (2)	Q _D	Q _C	Q _B	Q _A
H	H	L	L	L	L
L	X	COUNT			
X	L	COUNT			

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	UNIT
I _{CC}	MAX	39	15	mA
I _{DH}	MAX	-0.8	-0.4	mA
I _{OL}	MAX	16	8	mA

SWITCHING CHARACTERISTICS

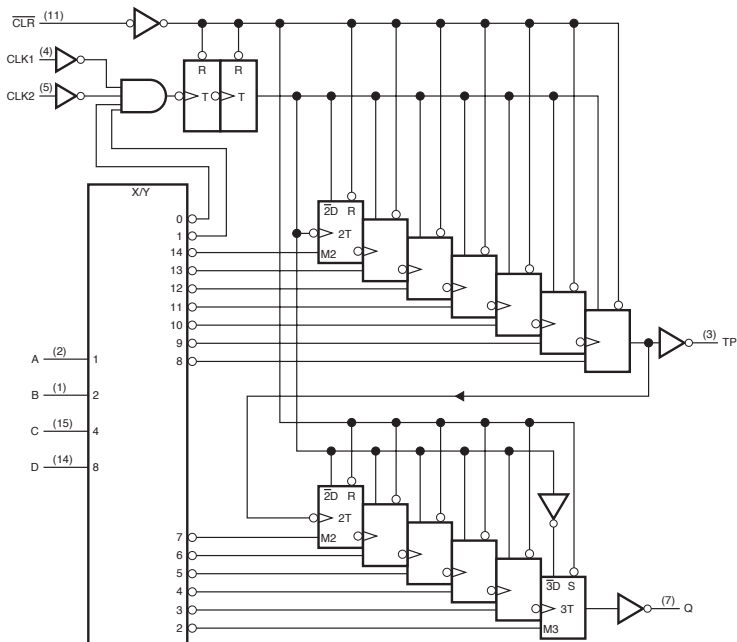
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS
f _{max}	A	Q _A	MIN	32	32
	B	Q _B	MIN	16	16
t _w	A	A, B	MIN	15	15
	B			30	30
	Reset			15	15
t _{SU}			MIN	25	25
t _{PLH}	A	Q _A	MAX	16	16
t _{PHL}				18	18
t _{PLH}	A	Q _B	MAX	70	70
t _{PHL}				70	70
t _{PLH}	B	Q _B	MAX	16	16
t _{PHL}				21	21
t _{PLH}	B	Q _C	MAX	32	32
t _{PHL}				35	35
t _{PLH}	B	Q _D	MAX	51	51
t _{PHL}				51	51

UNIT f_{max} : ■Hz, other : ns

PROGRAMMABLE FREQUENCY DIVIDER/DIGITAL TIMER

- Digitally Programmable from 2^2 to 2^{15}
- Easily Expandable
- Applications
 - Frequency Division
 - Digital Timing

Logic Diagram



FUNCTION TABLE

PROGRAMMING INPUTS				FREQUENCY DIVISION			
				Q		TP	
D	C	B	A	BINARY	DECIMAL	BINARY	DECIMAL
L	L	L	L	Inhibit	Inhibit	Inhibit	Inhibit
L	L	L	H	Inhibit	Inhibit	Inhibit	Inhibit
L	L	H	L	2 ²	4	2 ⁹	512
L	L	H	H	2 ³	8	2 ⁹	512
L	H	L	L	2 ⁴	16	2 ⁹	512
L	H	L	H	2 ⁵	32	2 ⁹	512
L	H	H	L	2 ⁶	64	2 ⁹	512
L	H	H	H	2 ⁷	128	Disabled Low	
H	L	L	L	2 ⁸	256	2 ²	4
H	L	L	H	2 ⁹	512	2 ³	8
H	L	H	L	2 ¹⁰	1024	2 ⁴	16
H	L	H	H	2 ¹¹	2048	2 ⁵	32
H	H	L	L	2 ¹²	4096	2 ⁶	64
H	H	L	H	2 ¹³	8192	2 ⁷	128
H	H	H	L	2 ¹⁴	16384	2 ⁸	256
H	H	H	H	2 ¹⁵	32768	2 ⁹	512

RECOMMENDED OPERATING CONDITIONS

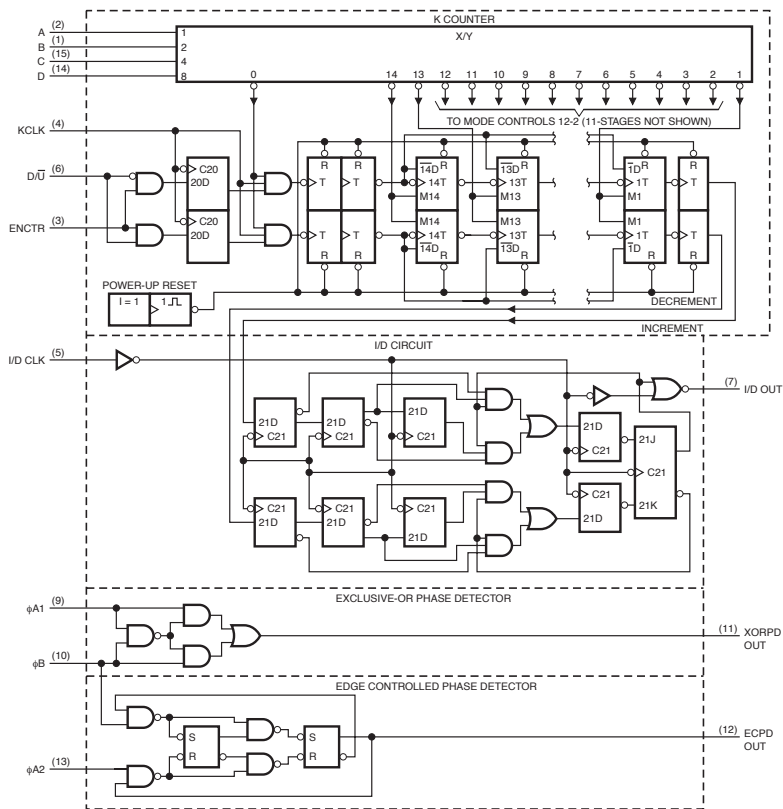
PARAMETER	MAX or MIN	LS	UNIT
I _{CC}	MAX	50	mA
I _{OH}	MAX	-1.2	V
I _{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
f _{max}	CLK		MIN	30
t _w	CLK 1 or 2		MIN	16
	CLR		MIN	35
t _{PLH}	CLK 1 or 2	Q	MAX	90
t _{PHL}		Q	MAX	120
t _{PLH}	$\overline{\text{CLR}}$	$\overline{\text{Q}}$	MAX	65

 UNIT f_{max} : ■Hz, other : ns

Logic Diagram



FUNCTION TABLES

**K COUNTER FUNCTION TABLE
(DIGITAL CONTROL)**

D	C	B	A	MODULO (K)
L	L	L	L	Inhibited
L	L	L	H	2 ²
L	L	H	L	2 ⁴
L	L	H	H	2 ⁵
L	H	L	L	2 ⁶
L	H	L	H	2 ⁷
L	H	H	L	2 ⁸
L	H	H	H	2 ⁹
H	L	L	L	2 ¹⁰
H	L	L	H	2 ¹¹
H	L	H	L	2 ¹²
H	L	H	H	2 ¹³
H	H	L	L	2 ¹⁴
H	H	L	H	2 ¹⁵
H	H	H	L	2 ¹⁶
H	H	H	H	2 ¹⁷

EXCLUSIVE OR PHASE DETECTOR

$\phi A1$	ϕB	XORPD OUT
L	L	L
L	H	H
H	L	H
H	H	L

EDGE-CONTROLLED PHASE DETECTOR

$\phi A2$	ϕB	ECPD OUT
H or L	↓	H
↓	H or L	L
H or L	↑	No change
↑	H or L	No change

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	CD74 ACT	UNIT
I _{CC}	MAX	120	0.16	0.16	0.08	mA
I _{OH} (I/D OUT)	MAX	-1	-6	-4	-24	mA
I _{OL} (XOR, ECPD)	MAX	-0.4	-6	-4	-24	mA
I _{OL} (I/D OUT)	MAX	24	6	4	24	mA
I _{OL} (XOR, ECPD)	MAX	8	6	4	24	mA

SWITCHING CHARACTERISTICS

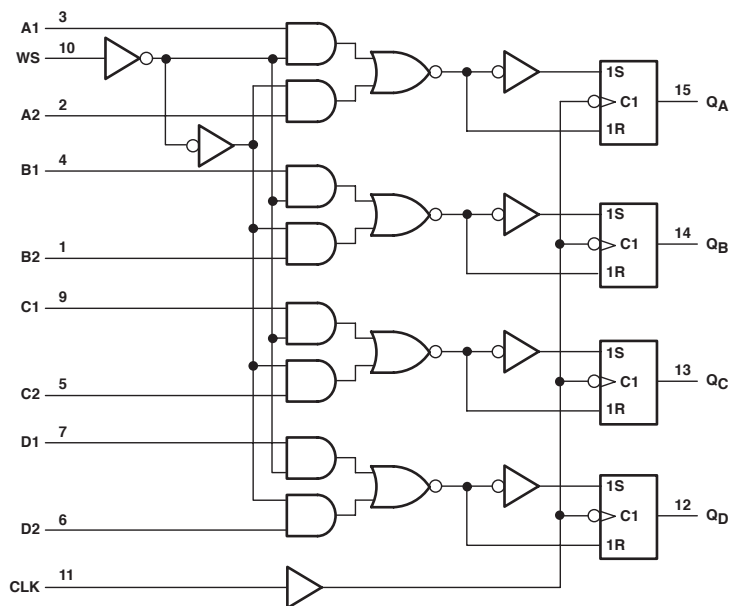
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT	CD74 ACT
f _{max}	K CLK	I/D OUT	MIN	32	20	20	45
	I/D CLK	I/D OUT		16	13	13	35
t _w	K CLK		MIN	16	24	24	8
	I/D CLK			33	38	38	9
t _{su}	D/ \bar{U}		MIN	30	30	30	17
	ENCLR			31	30	30	16
t _h	D/ \bar{U}		MIN	0	0	0	7
	ENCLR			0	0	0	6
t _{PLH}	I/D CLK *	I/D OUT	MAX	25	53	53	24
t _{PHL}				35	53	53	24
t _{PLH}	; A1 or ; B	other input low	MAX	15	45	45	22
t _{PHL}		other input high		25	45	45	22
t _{PLH}	; A1 or ; B	other input low	MAX	25	45	45	22
t _{PHL}		other input high		25	45	45	22
t _{PLH}	; B ,	ECPD OUT	MAX	30	60	60	30
t _{PHL}		ECPD OUT		30	60	60	30

UNIT f_{max} : MHz, other : ns

QUAD 2-INPUT MULTIPLEXERS WITH STORAGE

- Outputs Storage Register

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q _A	Q _B	Q _C	Q _D
L	↓	A1	B1	C1	D1
H	↓	A2	B2	C2	D2
X	H	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}

† a1, a2, etc. = the level of steady-state input at A1, A2, etc.
 Q_{A0}, Q_{B0}, etc. = the level of Q_A, Q_B, etc. entered
 on the most recent 0 transition of CLK

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	AS	SN74 HC	UNIT
I _{CC}	MAX	65	21	36	0.08	mA
I _{OL}	MAX	16	8	20	4	mA
I _{OH}	MAX	-0.8	-0.4	-2	-4	mA

SWITCHING CHARACTERISTICS

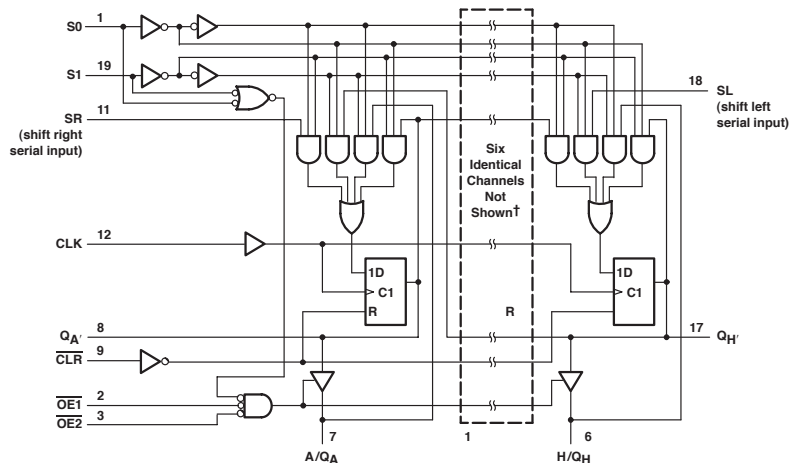
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	AS	SN74 HC	
t _r			MIN	20	20	8	27	
t _{su}			Data	MIN	15	15	4.5	21
			Word Select	MIN	25	25	13	21
t _h			Data	MIN	5	5	3.5	0
			Word Select	MIN	0	0	1	0
t _{PLH}			CLK	GA to GD	MAX	27	27	9
t _{PHL}	32	32				11	31	

UNIT: ns

8-BIT BIDIRECTIONAL UNIVERSAL SHIFT/STORAGE REGISTERS

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation:
 - Hold (Store)
 - Shift Right
 - Shift Left
 - Load Data
- Operate with Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for n-Bit Word Lengths

Logic Diagram



† I/O ports not shown: B/QB (13), C/QC (6), D/QD (14), E/QE (5), F/QF (15), and G/QG (4).

FUNCTION TABLE

MODE	INPUTS								I/O PORTS								OUTPUTS	
	CLR	S1	S0	OE1†	OE2†	CLK	SL	SR	A/Q _A	B/Q _B	C/Q _C	D/Q _D	E/Q _E	F/Q _F	G/Q _G	H/Q _H	Q _A †	Q _H †
Clear	L	X	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
Hold	H	L	L	L	L	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}
	H	X	X	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{E0}	Q _{F0}	Q _{G0}	Q _{H0}	Q _{A0}	Q _{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	H	Q _{Gn}
	H	L	H	L	L	↑	X	L	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	L	Q _{Gn}
Shift Left	H	H	L	L	L	↑	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	H	Q _{Bn}	H
	H	H	L	L	L	↑	X	X	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{En}	Q _{Fn}	Q _{Gn}	Q _{Hn}	L	Q _{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

NOTE: a...h—the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.
 † When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation clearing of the register is not affected.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT	UNIT	
											I _{CC}
I _{OH}	Q _A thru Q _H	MAX	-2.6	-6.5	-2.6	-3	-6	-4	-24	-24	mA
	Q _A † or Q _H †	MAX	-0.4	-0.5	-0.4	-1	-4	-4	-24	-24	mA
I _{OL}	Q _A thru Q _H	MAX	24	20	24	24	6	4	24	24	mA
	Q _A † or Q _H †	MAX	8	6	8	20	4	4	24	24	mA

SWITCHING CHARACTERISTICS

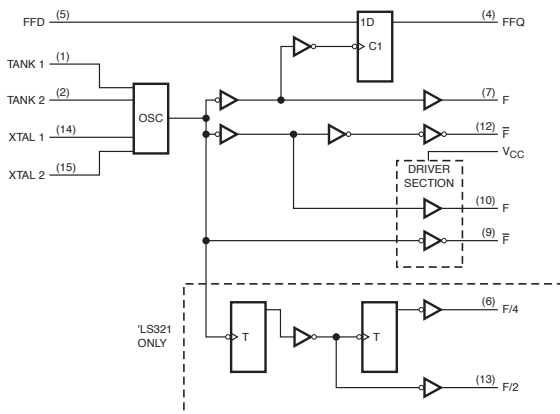
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	F	CD74 HC	CD74 HCT	CD74 AC	CD74 ACT
t _v	CLK high		MIN	30	10	16.5	7	24	30	5.2	5.5
				10	10	16.5	7	24	30	5.2	5.5
				20	10	10	7	15	22	5	5
t _{su}	DATA 'H'		MIN	20	7	16	5.5	36	30	4.5	4.5
				20	5	6	5.5	36	30	4.5	4.5
				35	15	20	8.5	36	41	9	9
				20	10	15	7	-	-	-	-
t _h	DATA		MIN	0	5	0	2	0	0	0	0
				10	5	0	0	0	0	0	0
				10	5	0	0	0	0	0	0
†P _{LH}	CLK	Q _A or Q _B	MAX	33	20	15	10	60	68	12.9	12.9
†P _{HL}				39	20	18	9.5	60	68	12.9	12.9
†P _{LH}	CLK	Q _A thru Q _H	MAX	25	21	13	10	60	68	13.5	14.5
†P _{HL}				39	21	19	12	60	68	13.5	14.5
†P _{HL}	CLR	Q _A † or Q _H †	MAX	40	21	22	10.5	60	69	11.2	12.2
†P _{HL}	CLR	Q _A thru Q _H		40	24	22	15	60	69	13.9	18.6
†P _{ZH}	OE1, OE2	Q _A thru Q _H	MAX	21	18	16	9	47	48	14.9	14.9
†P _{ZL}	OE1, OE2			30	18	22	11	39	45	14.9	14.9
†P _{PHZ}	OE1, OE2	Q _A thru Q _H	MAX	20	12	8	7	56	56	14.9	14.9
†P _{PLZ}				15	12	15	6.5	47	48	14.9	14.9

UNIT f_{max} : MHz, other : ns

CRYSTAL-CONTROLLED OSCILLATOR

- Crystal-Controlled Oscillator Operation from 1MHz to 20MHz
- Complementary Outputs

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I _{CC}		MAX	75	mA
I _{OH}	F' or F'	MAX	-24	mA
	F, F', F/2, F/4	MAX	-0.4	mA
I _{OL}	F' or F'	MAX	24	mA
	F, F', F/2, F/4	MAX	8	mA

SWITCHING CHARACTERISTICS

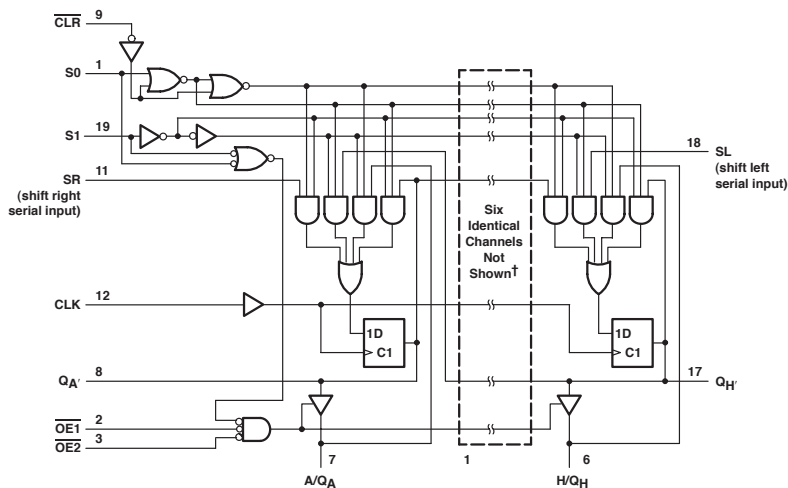
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
f _{max}		F/2	MIN	10
		F/4	MAX	5
		ANY	MIN	20
t _r		F', F'	MAX	14
		ANY	MAX	40
t _f		F', F'	MAX	10
	ANY	MAX	20	

UNIT f_{max} : MHz, other : ns

8-BIT BIDIRECTIONAL SHIFT/STORAGE REGISTERS

- Multiplexed I/O Ports Provide Improved Bit Density
- Four Modes of Operation:
 - Hold (Store)
 - Shift Right
 - Shift Left
 - Load Data
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for n-Bit Word Lengths

Logic Diagram



† I/O ports not shown: B/Q_B (13), C/Q_C (6), D/Q_D (14), E/Q_E (5), F/Q_F (15), and G/Q_G (4).

FUNCTION TABLE

MODE	INPUTS						I/O BORD										OUTPUTS			
	CLR	SELECT		OUTPUT CONTROL		CLK	SREAL												Q _A '	Q _H '
		S1	S0	OE1	OE2		SL	SR	A/Q _A	B/Q _B	C/Q _C	C/Q _D	C/Q _E	C/Q _F	C/Q _G	H/Q _H				
Clear	L L	X L	L X	L L	L L	↑ ↑	X X	X X	L L	L L	L L	L L	L L	L L	L L	L L	L L	L L	L L	L L
Hold	H H	L X	L X	L L	L L	X L	X X	X X	Q _{A0} Q _{A0}	Q _{B0} Q _{B0}	Q _{C0} Q _{C0}	Q _{D0} Q _{D0}	Q _{E0} Q _{E0}	Q _{F0} Q _{F0}	Q _{G0} Q _{G0}	Q _{H0} Q _{H0}	Q _{A0} Q _{A0}	Q _{H0} Q _{H0}	L L	L L
Shift Right	H H	L L	H H	L L	L L	↑ ↑	X X	H L	H L	Q _{An} Q _{An}	Q _{Bn} Q _{Bn}	Q _{Cn} Q _{Cn}	Q _{Dn} Q _{Dn}	Q _{En} Q _{En}	Q _{Fn} Q _{Fn}	Q _{Gn} Q _{Gn}	H L	Q _{Gn} Q _{Gn}	L L	L L
Shift Left	H H	H L	L L	L L	L L	↑ ↑	H L	X X	Q _{Bn} Q _{Bn}	Q _{Cn} Q _{Cn}	Q _{Dn} Q _{Dn}	Q _{En} Q _{En}	Q _{Fn} Q _{Fn}	Q _{Gn} Q _{Gn}	Q _{Hn} Q _{Hn}	H L	Q _{Bn} Q _{Bn}	L L	L L	L L
Load	H H	H H	H H	X X	X X	↑ ↑	X X	X X	a a	b b	c c	d d	e e	f f	g g	h h	a a	h h	L L	L L

† a...h at the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	CD74 AC	CD74 ACT	UNIT
I _{CC}	MAX	225	40	0.16	0.16	mA
I _{OH}	Q _A or Q _H '	-0.5	-0.4	-24	-24	mA
	Q _A thru Q _H	-6.5	-2.6	-24	-24	mA
I _{OL}	Q _A ' or Q _H	6	8	24	24	mA
	Q _A thru Q _H	20	24	24	24	mA

SWITCHING CHARACTERISTICS

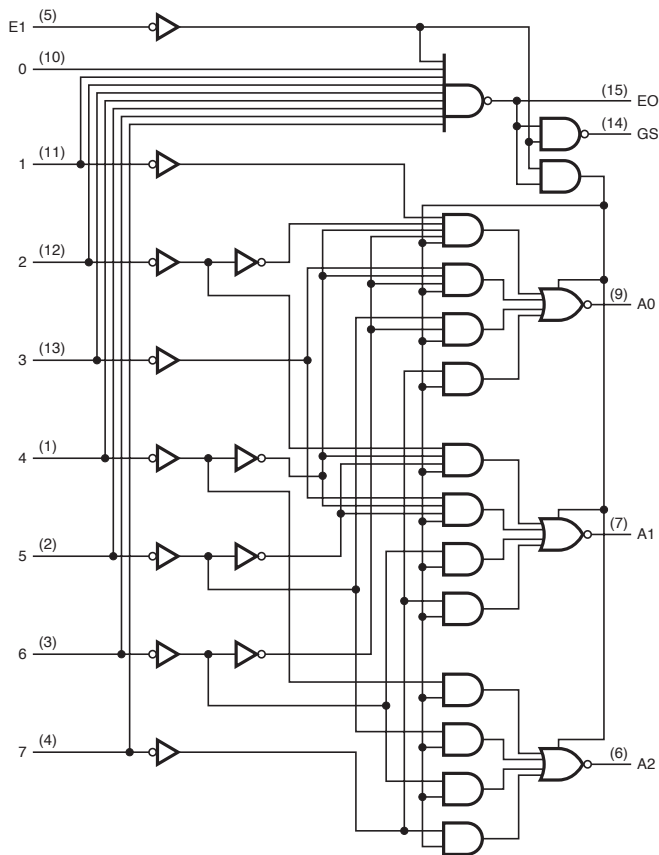
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	CD74 AC	CD74 ACT
f _{max}			MIN	25	17	95	90
t _w	CLK		MIN	30	16.5	5.2	5.5
	CLR			20	-	5	5
t _{su}	DATA H		MIN	20	16	4.5	4.5
	DATA L			20	6	4.5	4.5
	SELECT			-	20	9	9
	CLR			-	20	5.5	5.5
t _h	SELECT		MIN	-	0	0	0
	DATA			0	0	0	0
t _{PLH}	CLK	Q _A ' or Q _B	MAX	33	15	12.9	12.9
t _{PHL}				39	18	12.9	12.9
t _{PLH}	CLK	Q _A thru Q _H	MAX	25	13	13.5	14.5
t _{PHL}				39	19	13.5	14.5
t _{PZH}	$\overline{OE1}$	Q _A thru Q _H	MAX	21	16	14.9	14.9
t _{PZL}				30	22	14.9	14.9
t _{PHZ}	$\overline{OE1}$	Q _A thru Q _H	MAX	20	8	14.9	14.9
t _{PLZ}				15	15	14.9	14.9
t _{PZH}	$\overline{OE2}$	Q _A thru Q _H	MAX	21	16	14.9	14.9
t _{PZL}				30	22	14.9	14.9
t _{PHZ}	$\overline{OE2}$	Q _A thru Q _H	MAX	20	8	14.9	14.9
t _{PLZ}				15	15	14.9	14.9

UNIT f_{max}: MHz, other: ns

8-LINE TO 3-LINE PRIORITY ENCODER

- 3-State Outputs Drive Bus Lines Directly
- Encodes 8 Data Lines to 3-Line Binary (Octal)

Logic Diagram



FUNCTION TABLE

		INPUTS							OUTPUTS					
E1		0	1	2	3	4	5	6	7	A2	A1	A0	GS	E0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	H	H
L	H	H	H	H	H	H	H	H	H	Z	Z	Z	H	L
L	X	X	X	X	X	X	L	H	L	L	L	L	L	H
L	X	X	X	X	X	L	H	H	L	L	L	H	L	H
L	X	X	X	X	L	H	H	H	L	H	H	L	L	H
L	X	X	X	L	H	H	H	H	H	L	L	L	L	H
L	X	X	L	H	H	H	H	H	H	L	L	L	L	H
L	X	L	H	H	H	H	H	H	H	L	L	L	L	H
L	L	H	H	H	H	H	H	H	H	H	H	L	L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
Icc		MAX	25	mA
I _{DH}	A0, A1, A2	MAX	-2.6	mA
	E0, ES	MAX	-0.4	mA
I _{OL}	A0, A1, A2	MAX	24	mA
	E0, ES	MAX	8	mA

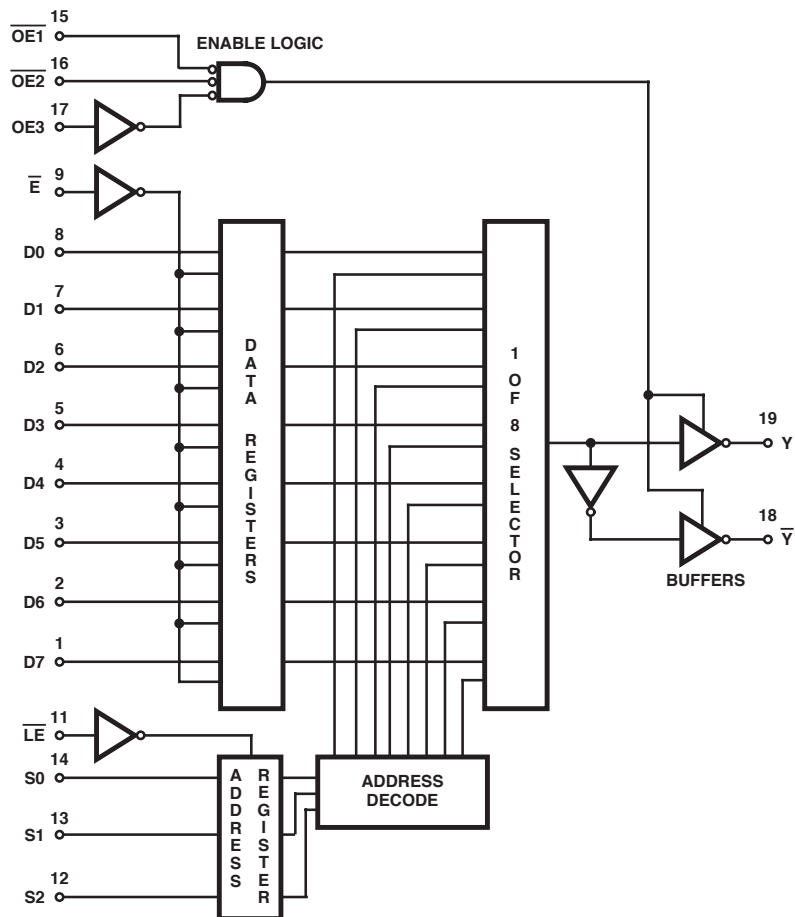
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t _{PLH}	1 to 7	A0, A1, A2	MAX	35
			MAX	35
t _{PLH}	0 to 7	E0	MAX	18
			MAX	40
t _{PLH}	0 to 7	GS	MAX	55
			MAX	21

UNIT: ns

8-INPUT MULTIPLEXER/REGISTER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE (SN74)

SELECT†			INPUTS			OUTPUTS		
S2	S1	S0	\overline{DC}	OUTPUT ENABLES			W	Y
			$\overline{G1}$	$\overline{G2}$	$\overline{G3}$			
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	L	L	L	H	D0 _n	D0 _n
L	L	L	H	L	L	H	D1 _n	D1 _n
L	L	H	L	L	L	H	D2 _n	D2 _n
L	L	H	H	L	L	H	D3 _n	D3 _n
L	H	L	L	L	L	H	D4 _n	D4 _n
L	H	L	H	L	L	H	D5 _n	D5 _n
L	H	H	L	L	L	H	D6 _n	D6 _n
L	H	H	H	L	L	H	D7 _n	D7 _n

NOTES:

H = High Voltage Level (Steady State), L = Low Voltage Level (Steady State), X = Don't Care, Z = High Impedance State (Off State), D0_n ... D7_n = the level of steady-state inputs D0 through D7, respectively, before the most recent low-to-high transition of data control.

† This column shows the input address setup with \overline{LE} low.

TRUTH TABLE

SELECT (NOTE 3)			ENABLE DATA			OUTPUT ENABLES			OUTPUTS	
S2	S1	S0	\overline{E}	$\overline{OE1}$	$\overline{OE2}$	$\overline{OE3}$	\overline{Y}	Y		
X	X	X	X	H	X	X	Z	Z		
X	X	X	X	X	X	H	X	Z		
X	X	X	X	X	X	L	Z	Z		
L	L	L	L	L	L	H	D0	D0		
L	L	L	L	L	L	H	D1	D1		
L	L	L	L	L	L	H	D2	D2		
L	L	L	L	L	L	H	D3	D3		
L	L	L	L	L	L	H	D4	D4		
L	L	L	L	L	L	H	D5	D5		
L	L	L	L	L	L	H	D6	D6		
L	L	L	L	L	L	H	D7	D7		
L	L	L	L	L	L	H	D0 _n	D0 _n		
L	L	L	L	L	L	H	D1 _n	D1 _n		
L	L	L	L	L	L	H	D2 _n	D2 _n		
L	L	L	L	L	L	H	D3 _n	D3 _n		
L	L	L	L	L	L	H	D4 _n	D4 _n		
L	L	L	L	L	L	H	D5 _n	D5 _n		
L	L	L	L	L	L	H	D6 _n	D6 _n		
L	L	L	L	L	L	H	D7 _n	D7 _n		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	CD74 HC	SN74 HCT	UNIT
I _{CC}	MAX	46	0.08	0.16	0.16	mA
I _{OH}	MAX	-2.6	-6	-6	-4	mA
I _{OL}	MAX	24	6	6	4	mA

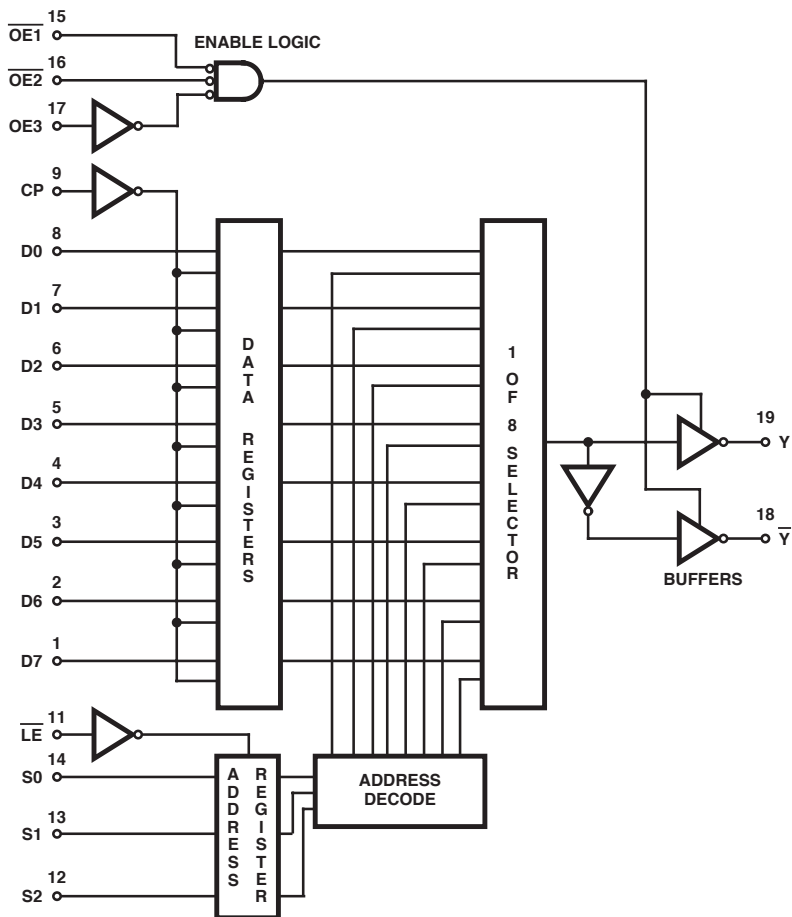
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC	CD74 HC	SN74 HCT
t _{su}			MAX	15	19	15	15
t _h			MAX	15	5	14	14
t _{PLH}	D0 thru D7	Y	MAX	36	59	63	71
t _{PHL}			MAX	35	59	63	71
t _{PLH}	D0 thru D7	W (CD74: \overline{Y})	MAX	27	59	63	71
t _{PHL}			MAX	44	59	63	71
t _{PLH}	\overline{DC} (CD74: \overline{E})	Y	MAX	42	68	75	81
t _{PHL}			MAX	39	68	75	81
t _{PLH}	\overline{DC} (CD74: \overline{E})	W (CD74: \overline{Y})	MAX	33	68	75	81
t _{PHL}			MAX	50	68	75	81

UNIT:ns

SYNCHRONOUS UP/DOWN DECADE COUNTER

Logic Diagram



FUNCTION TABLE (SN74)

INPUTS			OUTPUT ENABLES			OUTPUTS		
SELECT†	CLK		$\overline{G1}$	$\overline{G2}$	$\overline{G3}$	W	Y	
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	H	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	Hor L	L	L	H	$\overline{D0n}$	D0n
L	L	H	↑	L	L	H	$\overline{D1}$	D1
L	L	H	Hor L	L	L	H	$\overline{D1n}$	D1n
L	H	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	Hor L	L	L	H	$\overline{D2n}$	D2n
L	H	H	↑	L	L	H	$\overline{D3}$	D3
L	H	H	Hor L	L	L	H	$\overline{D3n}$	D3n
H	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	Hor L	L	L	H	$\overline{D4n}$	D4n
H	L	H	↑	L	L	H	$\overline{D5}$	D5
H	L	H	Hor L	L	L	H	$\overline{D5n}$	D5n
H	H	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	Hor L	L	L	H	$\overline{D6n}$	D6n
H	H	H	↑	L	L	H	$\overline{D7}$	D7
H	H	H	Hor L	L	L	H	$\overline{D7n}$	D7n

NOTES:

H = High Voltage Level (Steady State), L = Low Voltage Level (Steady State), ↑ = Transition from Low to High Level, X = Don't Care, Z = High Impedance State (Off State), $\overline{D0n} \dots \overline{D7n}$ = the level of steady-state inputs $\overline{D0}$ through $\overline{D7}$, respectively, before the most recent low-to-high transition of data control.

† This column shows the input address setup with \overline{LE} low.

TRUTH TABLE

INPUTS							OUTPUTS	
SELECT (NOTE 3)			CLOCK	OUTPUT ENABLES			\overline{Y}	Y
S2	S1	S0	CP	$\overline{OE1}$	$\overline{OE2}$	$\overline{OE3}$	\overline{Y}	Y
X	X	X	X	H	X	X	Z	Z
X	X	X	X	X	X	X	Z	Z
X	X	X	X	X	X	L	Z	Z
L	L	L	↑	L	L	H	$\overline{D0}$	D0
L	L	L	Hor L	L	L	H	$\overline{D0n}$	D0n
L	L	H	↑	L	L	H	$\overline{D1}$	D1
L	L	H	Hor L	L	L	H	$\overline{D1n}$	D1n
L	H	L	↑	L	L	H	$\overline{D2}$	D2
L	H	L	Hor L	L	L	H	$\overline{D2n}$	D2n
L	H	H	↑	L	L	H	$\overline{D3}$	D3
L	H	H	Hor L	L	L	H	$\overline{D3n}$	D3n
H	L	L	↑	L	L	H	$\overline{D4}$	D4
H	L	L	Hor L	L	L	H	$\overline{D4n}$	D4n
H	L	H	↑	L	L	H	$\overline{D5}$	D5
H	L	H	Hor L	L	L	H	$\overline{D5n}$	D5n
H	H	L	↑	L	L	H	$\overline{D6}$	D6
H	H	L	Hor L	L	L	H	$\overline{D6n}$	D6n
H	H	H	↑	L	L	H	$\overline{D7}$	D7
H	H	H	Hor L	L	L	H	$\overline{D7n}$	D7n

RECOMMENDED OPERATING CONDITIONS

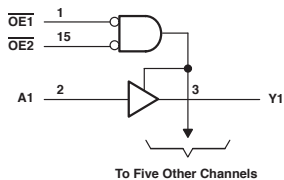
PARAMETER	MAX or MIN	LS	SN74 HC	CD74 HCT	UNIT
I_{CC}	MAX	46	0.08	0.16	mA
I_{OH}	MAX	-2.6	-6	-4	mA
I_{OL}	MAX	24	6	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC	CD74 HCT
t_{su}	D0 thru D7		MIN	15	19	11
t_h	D0 thru D7		MIN	0	5	14
t_{PLH}	CLK	Y	MAX	27	64	77
t_{PHL}				50	64	77
t_{PLH}	CLK	W (CD74: \overline{Y})	MAX	36	64	77
t_{PHL}				27	64	77
t_{PLH}	S0, S1, S2	Y	MAX	45	71	89
t_{PHL}				48	71	89
t_{PLH}	S0, S1, S2	W (CD74: \overline{Y})	MAX	54	71	89
t_{PHL}				45	71	89

UNIT: ns

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

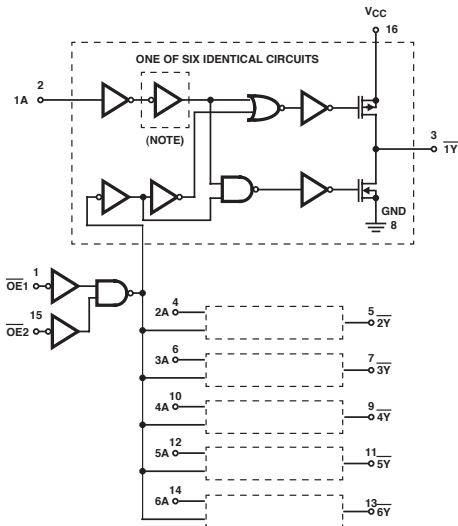
PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	85	24	0.08	0.16	0.16	mA
I_{OH}	MAX	-5.2	-2.6	-6	-6	-4	mA
I_{OL}	MAX	32	24	6	6	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A	Y	MAX	16	15	24	32	38
t_{PHL}			MAX	22	18	24	32	38
t_{PZH}	\bar{G}	Y	MAX	35	35	48	45	53
t_{PZL}			MAX	37	45	48	45	53
t_{PHZ}	\bar{G}	Y	MAX	11	32	48	45	53
t_{PLZ}			MAX	27	35	48	45	53

UNIT: ns

Logic Diagram



NOTE: Inverter not included in HC/HCT365.

FIGURE 1. LOGIC DIAGRAM FOR THE HC/HCT365 AND HC366 (OUTPUTS FOR HC/HCT365 ARE COMPLEMENTS OF THOSE SHOWN, I.E., 1Y, 2Y, ETC.)

FUNCTION TABLE

INPUTS			OUTPUT
$\overline{G1}$	$\overline{G2}$	A	Y
L	L	L	H
L	L	H	L
X	H	X	Z
H	X	X	Z

NOTES:

H = High Voltage Level
L = Low Voltage Level
X = Don't Care
Z = High Impedance (OFF) State

RECOMMENDED OPERATING CONDITIONS

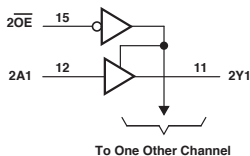
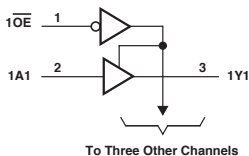
PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	UNIT
I_{CC}	MAX	77	21	0.08	160	mA
I_{OH}	MAX	-5.2	-2.6	-6	-6	mA
I_{OL}	MAX	32	24	6	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC
t_{PLH}	A	Y (CD74 : \overline{Y})	MAX	17	15	24	33
t_{PHL}			MAX	16	18	24	33
t_{PZH}	\overline{G} (CD74 : OE)	Y (CD74 : \overline{Y})	MAX	35	35	48	45
t_{PZL}			MAX	37	45	48	45
t_{PHZ}	\overline{G} (CD74 : OE)	Y (CD74 : \overline{Y})	MAX	11	32	48	45
t_{PLZ}			MAX	27	35	48	45

UNIT:ns

HEX BUS DRIVERS



RECOMMENDED OPERATING CONDITIONS

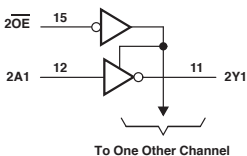
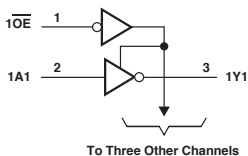
PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V	UNIT
I _{CC}	MAX	85	24	0.08	0.16	0.16	0.04	0.04	-	0.02	mA
I _{OH}	MAX	-5.2	-2.6	-6	-6	-4	-8	-8	-8	-16	mA
I _{OL}	MAX	32	24	6	6	4	8	8	8	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	AHC	AHCT	LV 3V	LV 5V
t _{PLH}	A	Y	MAX	16	16	24	32	38	9	6.5	13.5	9
			MAX	22	22	24	32	38	9	6.5	13.5	9
t _{PZH}	\bar{G}	Y	MAX	35	35	48	45	53	10.5	9.5	16	10.5
			MAX	47	40	48	45	53	10.5	8.5	16	10.5
t _{PHZ}	\bar{G}	Y	MAX	11	30	48	45	53	10.5	9.5	15.5	10.5
			MAX	27	35	48	45	53	10.5	8.5	15.5	10.5

UNIT: ns

HEX BUS DRIVERS



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	77	21	0.08	0.16	0.16	mA
I _{OH}	MAX	-5.2	-2.6	-6	-6	-4	mA
I _{OL}	MAX	32	24	6	6	4	mA

SWITCHING CHARACTERISTICS

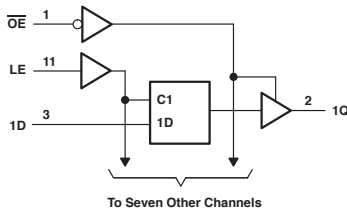
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
t _{PLH}	A	Y	MAX	17	15	24	32	45
			MAX	16	18	24	32	45
t _{PZH}	\bar{G}	Y	MAX	35	35	48	45	53
			MAX	37	45	48	45	53
t _{PHZ}	\bar{G}	Y	MAX	11	32	48	45	53
			MAX	27	35	48	45	53

UNIT: ns

OCTAL D-TYPE LATCHES

- 3-State Bus-Driving True Outputs
- Buffered Control Inputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

OUTPUT CONTROL	INPUTS		OUTPUT Q
	LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH	UNIT
I _{CC}	MAX	40	190	27	100	55	0.08	0.16	0.08	0.16	60	30	5	mA
I _{OH}	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-32	mA
I _{OL}	MAX	24	20	24	48	24	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVCH 3V	UNIT
I _{CC}	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.02	mA
I _{OH}	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	mA
I _{OL}	MAX	24	24	24	24	24	24	8	8	8	16	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT		OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH
	High	Low														
t _w	High	D	Q	MIN	15	6	10	4.5	6	20	24	25	24	7.5	3.3	3
	Low			MIN	15	7.3	-	-	-	-	-	-	-	-	-	-
t _{su}		D	Q	MIN	5	0	10	2	2	13	15	13	20	2	1.9	1.1
				MIN	20	10	7	3	3	12	5	10	15	5.5	1	1.4
t _{PHL}	D	Q	MAX	18	12	12	6	8	38	45	44	48	9.3	5.9	3.9	
t _{PHL}			MAX	18	12	16	6	6	38	45	44	48	9.5	6.2	3.9	
t _{PLH}	LE	Q	MAX	30	14	22	11.5	13	44	53	44	53	9.3	6.6	4.2	
t _{PHL}			MAX	30	18	23	7.5	8	44	53	44	53	8.8	7.2	4.2	
t _{PZH}	\overline{OE}	Q	MAX	28	15	18	6.5	12	38	45	44	53	11.8	5.2	4.8	
t _{PZL}			MAX	36	18	20	9.5	8.5	38	45	44	53	12	6.7	4.8	
t _{PHZ}	\overline{OE}	Q	MAX	25	9	10	6.5	7.5	38	45	44	53	7	6.9	4.6	
t _{PLZ}			MAX	20	12	12	7	6	38	45	44	53	7.4	6.5	4.5	

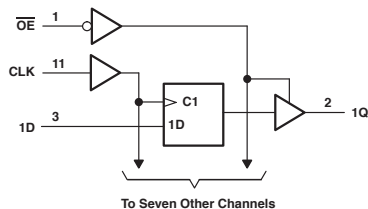
PARAMETER	INPUT		OUTPUT	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVCH 3V
	High	Low														
t _w	High	D	Q	MIN	4	4.5	4	5	8	4	5	6.5	5	5	3.3	3.3
	Low			MIN	-	-	4	-	-	4	-	-	-	-	-	-
t _{su}		D	Q	MIN	3.5	4.5	2	3.5	8	2	4	1.5	4	4	2	0.5
				MIN	2	1	3	3.5	1	3	1	3.5	1	1	1.5	1.2
t _{PHL}	D	Q	MAX	10.3	10.5	8.5	11.8	11.5	10.4	10.5	10.5	17	10.5	6.8	3.6	
t _{PHL}			MAX	8.4	10.5	8.5	10	11.5	10.4	10.5	10.5	17	10.5	6.8	3.6	
t _{PLH}	LE	Q	MAX	11.3	10.5	12	13	11.5	12.5	10.5	14.5	16.5	10.5	7.6	3.3	
t _{PHL}			MAX	10.2	10.5	12	12.2	11.5	12.5	10.5	14.5	16.5	10.5	7.6	3.3	
t _{PZH}	\overline{OE}	Q	MAX	10.8	9.5	10.5	12.5	10.5	13.5	11.5	13.5	17	11.5	7.7	4.8	
t _{PZL}			MAX	9.7	9.5	10.5	12	10.5	13.5	11.5	13.5	17	11.5	7.7	4.8	
t _{PHZ}	\overline{OE}	Q	MAX	11.1	12.5	11.5	12.2	12.5	12.5	10.5	12	15	10.5	7	4.4	
t _{PLZ}			MAX	8.7	10	11.5	10.1	10	12.5	10.5	12	15	10.5	7	4.4	

UNIT f_{max}: MHz, other: ns

OCTAL D-TYPE FLIP-FLOPS

- Buffered Control Inputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

OUTPUT CONTROL	INPUTS		OUTPUT Q
	CLK	D	
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	UNIT
I _{CC}	MAX	40	160	31	128	86	0.08	0.16	0.08	0.16	60	30	5	mA
I _{OH}	MAX	-2.6	-6.5	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-32	mA
I _{OL}	MAX	24	20	24	48	24	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVCH 3V	UNIT
I _{CC}	MAX	0.08	0.04	0.16	0.08	0.04	0.16	0.04	0.04	-	0.02	0.01	0.01	mA
I _{OH}	MAX	-24	-24	-24	-24	-24	-24	-8	-8	-8	-16	-24	-24	mA
I _{OL}	MAX	24	24	24	24	24	24	8	8	8	16	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	S	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	
f _{max}			MIN	35	75	35	125	70	24	20	25	20	70	150	150	
t _w	High		MIN	15	6	14	4	7	20	24	20	24	20	7	3.3	3.3
			MIN	15	7.3	14	3	6	20	24	20	24	-	3.3	3.3	
t _{su}			MIN	20	5	10	2	2	25	18	25	18	6.5	1.9	1.5	
			MIN	0	2	0	2	2	5	5	10	5	0	2.1	0.8	
t _h			MIN	0	2	0	2	2	5	5	10	5	0	2.1	0.8	
t _{PH}	CLK	Q	MAX	28	15	12	8	10	45	50	45	50	10.6	6.2	4.5	
t _{PHL}			MAX	28	17	16	9	10	45	50	45	50	10	7.1	4.2	
t _{PZH}	\overline{OE}	Q	MAX	26	15	17	6	12.5	38	45	38	42	12.3	5.2	4.7	
t _{PZL}			MAX	28	18	18	10	8.5	38	45	38	42	12.7	6.7	4.7	
t _{PHZ}	\overline{OE}	Q	MAX	28	9	10	6	8	38	41	38	45	6.8	6.7	4.6	
t _{PLZ}			MAX	20	12	18	6	6.5	38	41	38	45	6.8	6.5	4.5	

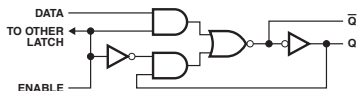
PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	ALVCH 3V
f _{max}			MIN	95	100	12.5	55	90	110	75	75	50	75	100	150
t _w	High		MIN	5	4.5	4	9	5	4.5	5	6.5	5.5	5	3.3	3.3
			MIN	5	4.5	4	9	5	4.5	5	6.5	5.5	5	3.3	3.3
t _{su}			MIN	2.5	4.5	2	3	5.5	2	3	2.5	4.5	3	2	1.8
			MIN	3.5	1.5	2	5.5	1.5	3	2	2.5	2	2	1.5	0.5
t _h			MIN	3.5	1.5	2	5.5	1.5	3	2	2.5	2	2	1.5	0.5
t _{PH}	CLK	Q	MAX	10.2	10.5	10.8	12.4	11.5	11.2	11.5	11.5	18.5	11.5	7	3.6
t _{PHL}			MAX	10.1	10	10.8	13	11	11.2	11.5	11.5	18.5	11.5	7	3.6
t _{PZH}	\overline{OE}	Q	MAX	9.1	9.5	14.5	12.3	10.5	14.5	11	12.5	16.5	11	7.5	5.2
t _{PZL}			MAX	9.4	9.5	14.5	12.3	10.5	14.5	11	12.5	16.5	11	7.5	5.2
t _{PHZ}	\overline{OE}	Q	MAX	11.2	12.5	14.5	13.2	12.5	14.5	10	12	16	10	6.5	4.5
t _{PLZ}			MAX	9.2	10	14.5	10.8	10	14.5	10	12	16	10	6.5	4.5

UNIT f_{max}: MHz, other: ns

4-BIT BISTABLE LATCHES

- Complementary Outputs (Q , \bar{Q})

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUTS	
D	C	Q	
L	H	L	H
H	H	H	L
X	L	Q_0	\bar{Q}_0

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	UNIT
I_{CC}	MAX	12	0.04	mA
I_{OH}	MAX	-0.4	-4	mA
I_{OL}	MAX	8	4	mA

SWITCHING CHARACTERISTICS

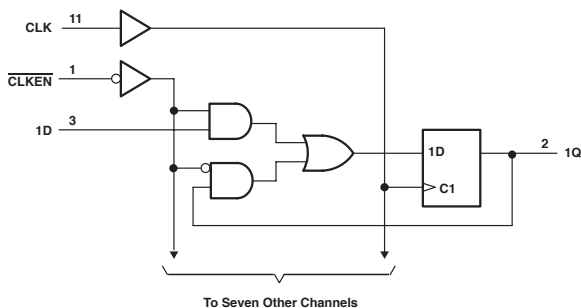
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
t_W			MIN	20	20
t_{SU}			MIN	20	25
t_H			MIN	0	5
t_{PLH}	D	Q	MAX	27	30
t_{PHL}			MAX	17	30
t_{PLH}	D	\bar{Q}	MAX	20	30
t_{PHL}			MAX	15	30
t_{PLH}	C	Q	MAX	27	33
t_{PHL}			MAX	25	33
t_{PLH}	C	\bar{Q}	MAX	30	33
t_{PHL}			MAX	15	33

UNIT: ns

OCTAL D-TYPE FLIP-FLOPS

- Individual Data Input to Each Flip-Flop
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
CLKEN	CLOCK	DATA	Q	\bar{Q}
H	X	X	Q_0	\bar{Q}_0
L	1	H	H	L
L	1	L	L	H
X	L	X	Q_0	\bar{Q}_0

RECOMMENDED OPERATING CONDITIONS

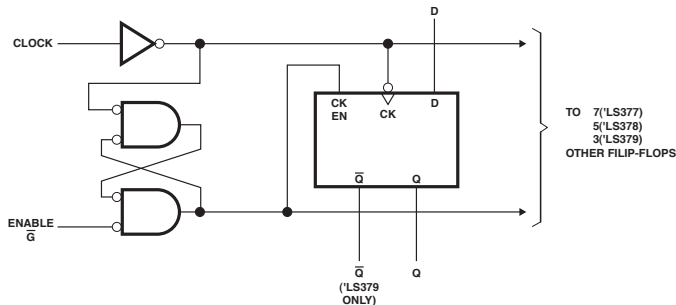
PARAMETER	MAX or MIN	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	UNIT
I_{CC}	MAX	28	90	0.08	0.16	0.08	0.16	30	0.08	mA
I_{OH}	MAX	-0.4	-1	-4	-4	-4	-4	-32	-24	mA
I_{OL}	MAX	8	20	4	4	4	4	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11
f_{max}			MIN	30	110	20	20	17	16	150	100
t_w			MIN	20	5	25	24	25	30	3.3	5
t_{su}	DATA		MIN	20	2	25	18	15	18	2.5	4
		CLKEN ACTIVE	MIN	25	2.5	25	-	15	-	3	6
		CLKEN INACTIVE	MIN	10	4.5	25	18	15	18	3	6
			MIN	5	1	5	3	3	3	1.8	0
t_{PLH}	CLK	Q	MAX	27	10	40	53	45	57	6.5	11.3
t_{PHL}	CLK	Q	MAX	27	10.5	40	53	45	57	7.3	12.9

UNIT f_{max} : MHz; other: ns

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
\bar{G}	CLOCK	DATA	Q	\bar{Q}
H	X	X	Q ₀	\bar{Q}_0
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q ₀	\bar{Q}_0

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	F	SN74 HC	UNIT
I _{CC}	MAX	22	45	0.08	mA
I _{OH}	MAX	-0.4	-1	-4	mA
I _{OL}	MAX	8	20	4	mA

SWITCHING CHARACTERISTICS

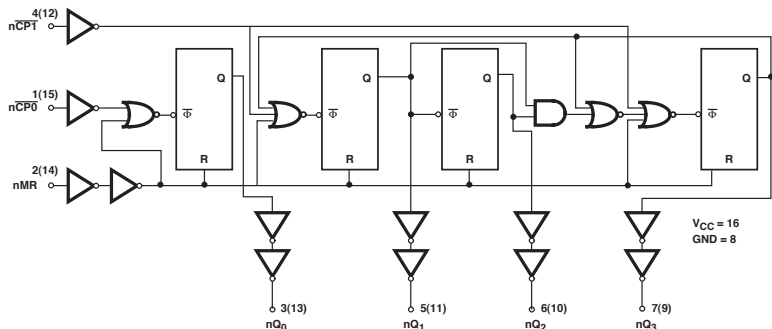
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	F	SN74 HC
f _{max}			MIN	30	110	20
t _w	CLK H		MIN	20	4	25
	CLK L		MIN	20	6	25
t _{su}	DATA		MIN	20	5	25
	\bar{G} ACTIVE		MIN	25	3.5	25
	\bar{G} INACTIVE		MIN	10	5	25
			MIN	5	0	5
t _h			MIN	5	0	5
↑P _{LH}	CLK	Q	MAX	27	6.7	40
↑P _{LH}			MAX	27	6.1	40

UNIT f_{max}: MHz, other: ns

DUAL DECADE COUNTERS

- Individual Clock for A and B Flip-Flops Provide Dual + 2 and + 5 Counters
- All Have Direct Clear for Each 4-Bit Counter
- Typical maximum Count Frequency: 35MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

Logic Diagram



FUNCTION TABLE

BCD COUNT SEQUENCE

COUNT	OUTPUTS			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H

BI-QUINARY

COUNT	OUTPUTS			
	Q _A	Q _D	Q _C	Q _B
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	H	L	L	L
6	H	L	L	H
7	H	L	H	L
8	H	L	H	H
9	H	H	L	L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	69	26	0.08	0.16	0.16	mA
I _{OH}	MAX	-0.8	-0.4	-4	-4	-4	mA
I _{OL}	MAX	16	8	4	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT
f _{max}	A	Q _A	MIN	25	25	25	20	18
	B	Q _B	MIN	20	12.5	25	20	18
t _w	A	Q _A	MIN	20	20	20	24	29
			MIN	25	40	20	24	29
			MIN	20	20	20	15	20
t _{SU}	A	Q _A	MIN	25	25	5	-	-
			MAX	20	20	30	53	60
t _{PLH}	A	Q _A	MAX	20	20	30	53	60
			MAX	60	60	72	-	126
t _{PHL}	A	Q _C	MAX	60	60	72	-	126
			MAX	21	21	33	56	65
t _{PLH}	B	Q _B	MAX	21	21	33	56	65
			MAX	39	39	46	74	83
t _{PHL}	B	Q _C	MAX	39	39	46	74	83
			MAX	21	21	33	54	63
t _{PLH}	B	Q _D	MAX	21	21	33	54	63
			MAX	39	39	41	57	63
t _{PHL}	CLR	Q	MAX	39	39	41	57	63

UNIT f_{max} : MHz, other : ns

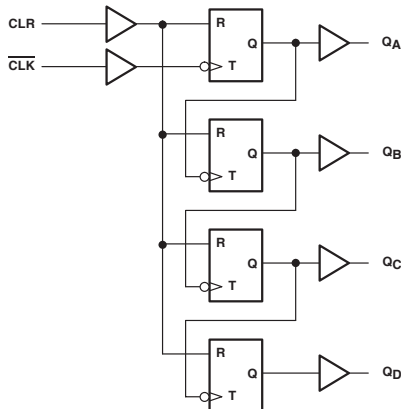
DUAL 4-BIT BINARY COUNTERS

- Dual 4-Bit Binary Counter with Individual Clock
- All Have Direct Clear for Each 4-Bit Counter
- Typical maximum Count Frequency: 35MHz
- Buffered Outputs Reduce Possibility of Collector Commutation

FUNCTION TABLE

COUNT	INPUTS			
	Q _D	Q _C	Q _B	Q _A
0	L	L	L	L
1	L	L	L	H
2	L	L	H	L
3	L	L	H	H
4	L	H	L	L
5	L	H	L	H
6	L	H	H	L
7	L	H	H	H
8	H	L	L	L
9	H	L	L	H
10	H	L	H	L
11	H	L	H	H
12	H	H	L	L
13	H	H	L	H
14	H	H	H	L
15	H	H	H	H

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I _{CC}	MAX	64	26	0.08	0.16	0.16	-	0.02	mA
I _{OH}	MAX	-0.8	-0.4	-4	-4	-4	-6	-12	mA
I _{OL}	MAX	16	8	4	4	4	6	12	mA

SWITCHING CHARACTERISTICS

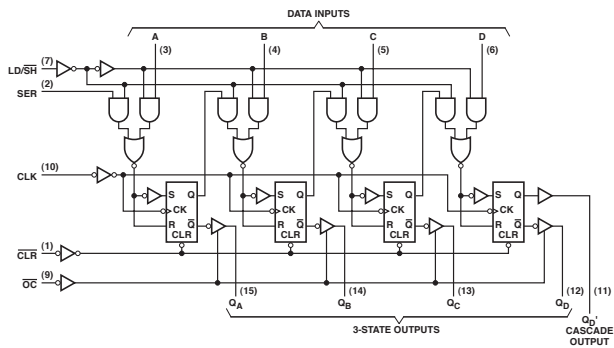
PARAMETER	INPUT	OUTPUT	MAX or MIN	TTL	LS	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
t _{max}			MIN	25	25	25	20	18	35	75
t _w	A		MIN	20	20	20	24	29	5	5
			MIN	25	40	20	24	29	5	5
			MIN	20	20	20	24	24	5	5
			MIN	25	25	5	-	-	5	4
t _{PHL}	A	Q _A	MAX	20	20	30	59	48	19	12
			MAX	20	20	30	59	48	19	12
t _{PLH}	B	Q _D	MAX	60	60	72	86	93	26.5	16.5
			MAX	60	60	72	86	93	26.5	16.5
t _{PHL}	CLR	Q	MAX	39	39	41	41	48	18	11.5

UNIT f_{max}: MHz, other: ns

CASCADABLE UNIVERSAL SHIFT REGISTERS

- 3-State Outputs
- Parallel-In, Parallel-Out Registers
- Low Power Dissipation: 75mW Typical (Enable)

Logic Diagram



FUNCTION TABLE

CLEAR	INPUTS				3-STATE OUTPUTS				CASCADE			
	LOAD/SHIFT CONTROL	CLOCK	SERIAL	PARALLEL			Q _A	Q _B	Q _C	Q _D	OUTPUT Q _D	
				A	B	C						D
L	X	X	X	X	X	X	X	L	L	L	L	L
H	H	H	X	X	X	X	X	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}	Q _{D0}
H	H	↓	X	a	b	c	d	a	b	c	d	d
H	L	H	X	X	X	X	X	Q _{A0}	Q _{Bn}	Q _{Cn}	Q _{Dn}	Q _{D0}
H	L	↓	H	X	X	X	X	H	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Cn}
H	L	↓	L	X	X	X	X	L	Q _{An}	Q _{Bn}	Q _{Cn}	Q _{Cn}

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I _{CC}	MAX	34	mA
I _{OH}	Q _A , Q _B , Q _C , Q _D	MAX	-2.6 mA
	Q _D '	MAX	-0.4 mA
I _{OL}	Q _A , Q _B , Q _C , Q _D	MAX	24 mA
	Q _D '	MAX	8 mA

SWITCHING CHARACTERISTICS

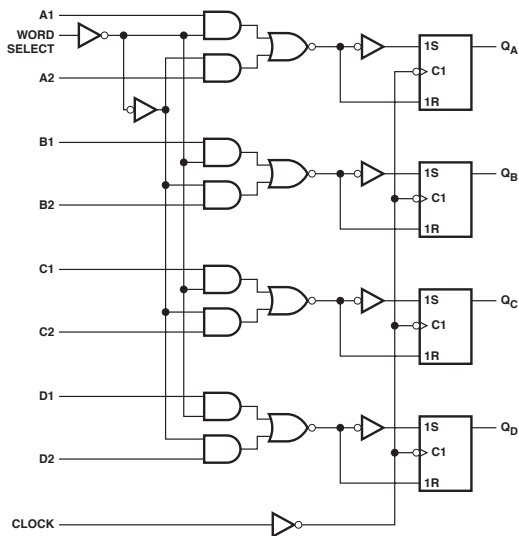
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	
f _{max}			MIN	30	
t _w			MIN	16	
t _{su}			LD/SH	MIN	40
			OTHER	MIN	20
t _h			MIN	10	
t _{PH}	CLK	Q	MAX	30	
			MAX	30	

 UNIT f_{max} : MHz, other : ns

QUAD 2-INPUT MULTIPLEXER WITH STORAGE

- Single-Rail Outputs (Q , \bar{Q})
- Select One of Two 4-Bit Data Sources and Stores Data Synchronously with System Clock

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUTS			
WORD SELECT	CLOCK	Q _A	Q _B	Q _C	Q _D
L	↑	A ₁	B ₁	C ₁	D ₁
H	↑	A ₂	B ₂	C ₂	D ₂
X	L	Q _{A0}	Q _{B0}	Q _{C0}	Q _{D0}

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I _{CC}	MAX	13	mA
I _{OH}	MAX	-0.4	mA
I _{OL}	MAX	8	mA

SWITCHING CHARACTERISTICS

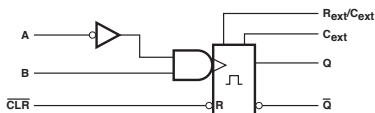
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t _w			MIN	20
t _{su}	DATA		MIN	25
	WORD SELECT		MIN	45
t _h	DATA		MIN	0
	WORD SELECT		MIN	0
t _{PLH}	CLK	Q	MAX	27
t _{PHL}			MAX	32

UNIT: ns

RE-TRIGGERABLE MONO-STABLE MULTIVIBRATOR

- Will Not Trigger from Clear

Logic Diagram



FUNCTION TABLE

CLR	INPUTS		OUTPUTS	
	A	B	Q	\bar{Q}
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	↑		
H	↓	H		

RECOMMENDED OPERATING CONDITIONS

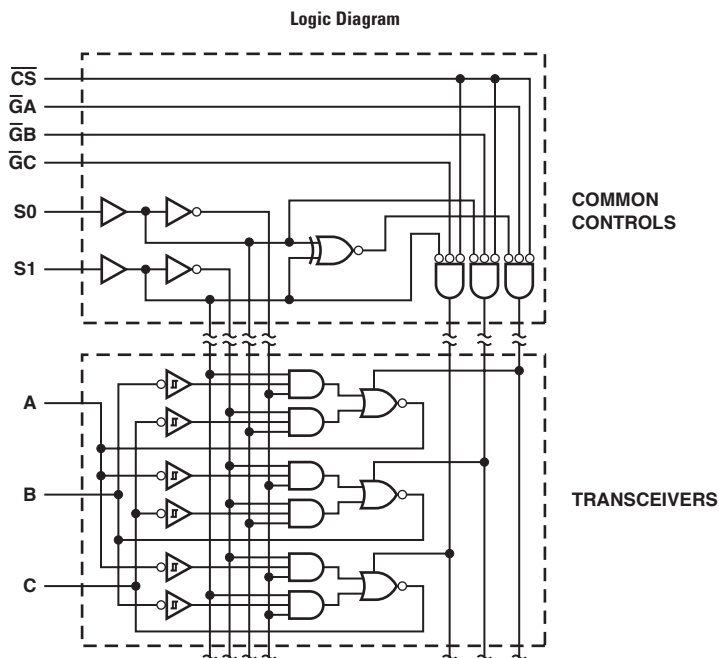
PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	20	0.16	0.16	mA
I_{DH}	MAX	-0.4	-4	-4	mA
I_{OL}	MAX	8	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT
t_d			MIN	40	30	30
t_{PLH}	A	Q	MAX	33	90	-
	B			44	90	-
t_{PHL}	A	\bar{Q}	MAX	45	96	-
	B			56	96	-
t_{PLH}	CLR	Q	MAX	27	65	-
		\bar{Q}	MAX	45	65	-

UNIT: ns

QUADRUPLE TRIDIRECTIONAL BUS TRANSCEIVERS



FUNCTION TABLE

INPUTS						TRANSFERS
CS	S1	S0	GA	GB	GC	BUSES
H	X	X	X	X	X	None
X	H	H	X	X	X	None
X	X	X	H	H	H	None
X	L	L	X	H	H	None
X	L	H	H	X	H	None
X	H	L	H	H	X	None
L	L	L	X	L	L	A → B, A → C
L	L	H	L	X	L	B → C, B → A
L	H	L	L	L	X	C → A, C → B
L	L	L	X	L	H	A → B
L	L	H	H	X	L	B → C
L	H	L	L	H	X	C → A
L	L	L	X	H	L	A → C
L	L	H	L	X	H	B → A
L	H	L	H	L	X	C → B

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I _{CC}	MAX	95	mA
I _{OH}	MAX	-15	mA
I _{OL}	MAX	24	mA

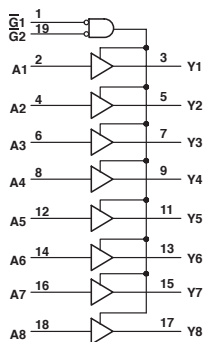
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t _{PLH}	A	B or C	MAX	14
	B	A or C		
	C	A or B		
t _{PHL}	A	B or C	MAX	20
	B	A or C		
	C	A or B		
t _{PZL}	Any \bar{C}	A, B, C	MAX	33
	S0, S1			42
	CS			36
t _{PZH}	\bar{C} , S, \bar{CS}	A, B, C	MAX	32
t _{PLZ}	\bar{C} , S, \bar{CS}	A, B, C	MAX	35
t _{PHZ}	\bar{C} , S, \bar{CS}	A, B, C	MAX	25

UNIT:ns

OCTAL BUFFERS 3-STATE OUTPUTS

Logic Diagram



† These symbols are in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	UNIT
I _{CC}	MAX	37	33	mA
I _{DH}	MAX	-2.6	-15	mA
I _{OL}	MAX	24	24	mA

SWITCHING CHARACTERISTICS

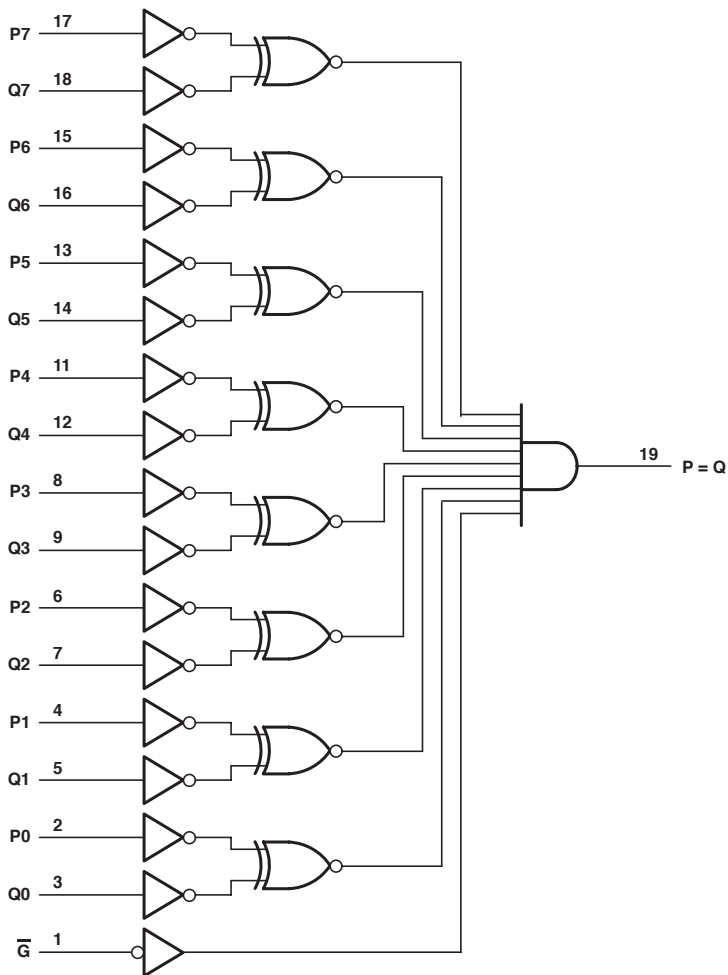
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS
t _{PLH}	A	Y	MAX	15	13
t _{PHL}				18	12
t _{PZH}	\bar{G}	Y	MAX	40	23
t _{PZL}				45	25
t _{PHZ}	\bar{G}		MAX	40	10
t _{PLZ}				45	18

UNIT:ns

8-BIT IDENTITY COMPARATOR

- Open-Collector Outputs
- 20-k Ω Pullup Resistors on Q Inputs

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE G	P = Q
P = Q	L	H
P > Q	L	L
P < Q	L	L
X	H	L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I _{CC}	MAX	17	mA
I _{OL}	MAX	24	mA
V _{OH}	MAX	5.5	V

SWITCHING CHARACTERISTICS

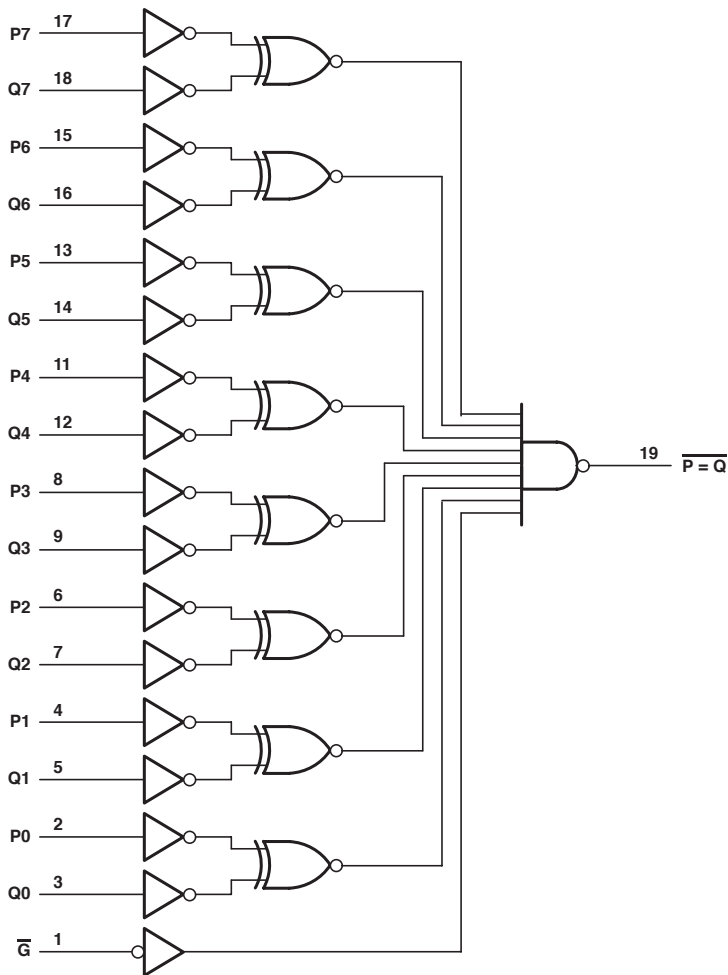
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t _{PLH}	P or Q	P = Q	MAX	33
t _{PHL}				15
t _{PLH}	\bar{G}	P = Q	MAX	33
t _{PHL}				15

UNIT: ns

8-BIT IDENTITY COMPARATOR

- 20-k Ω Pullup Resistors on Q Inputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE OE	$\overline{P} = \overline{Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	F	AC 11	UNIT
I _{CC}	MAX	19	32	8	mA
I _{DH}	MAX	-2.6	-1	-24	mA
I _{OL}	MAX	24	20	24	mA

SWITCHING CHARACTERISTICS

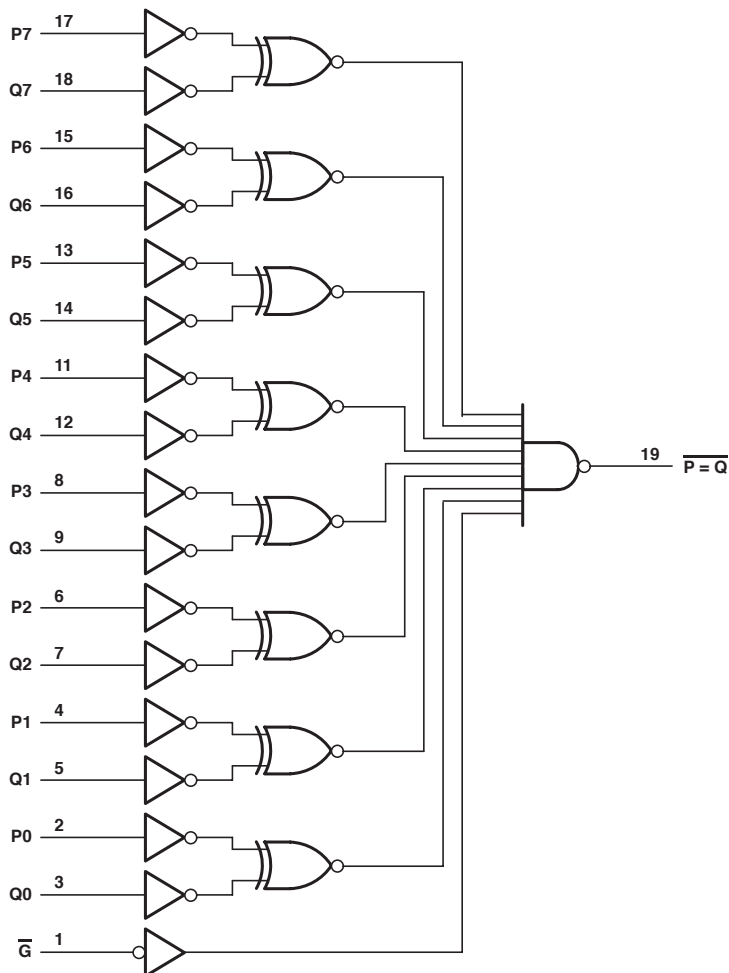
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	F	AC 11
I _{PLH}	P or Q	$\overline{P} = \overline{Q}$	MAX	12	8.7	12.6
				20	10.3	11.3
I _{PHL}	\overline{OE}	$\overline{P} = \overline{Q}$	MAX	12	6.4	7.4
				22	10.4	7.8

UNIT: ns

8-BIT IDENTITY COMPARATOR

● 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
DATA P, Q	ENABLE \overline{G}	$\overline{P = Q}$
P = Q	L	L
P > Q	L	H
P < Q	L	H
X	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	F	AC 11	UNIT
I _{CC}	MAX	19	32	0.08	mA
I _{OH}	MAX	-2.6	-1	-24	mA
I _{OL}	MAX	24	20	24	mA

SWITCHING CHARACTERISTICS

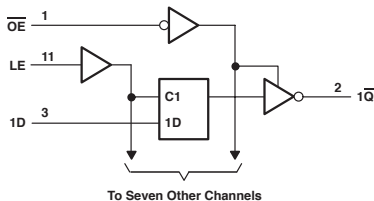
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	F	AC 11
t _{PLH}	P or Q	$\overline{P = Q}$	MAX	12	11	13
				20	11	11.4
t _{PHL}	\overline{G}	$\overline{P = Q}$	MAX	12	7.5	7.9
				22	10	8.1

UNIT: ns

OCTAL D-TYPE TRANSPARENT LATCHES

- 3-State Bus-Driving Inverting Outputs
- Functionally Equivalent to '373, Except for Having Inverted Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
\overline{OC}	ENABLE C	D	
L	H	H	L
L	H	L	H
L	L	X	$\overline{Q_0}$
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	ACT 11	SN74 ACT	UNIT
I_{CC}	MAX	28	110	0.08	0.16	0.08	0.16	30	0.08	0.04	0.08	0.04	mA
I_{OH}	MAX	-2.6	-15	-6	-6	-6	-6	-32	-24	-24	-24	-24	mA
I_{OL}	MAX	24	48	6	6	6	6	64	24	24	24	24	mA

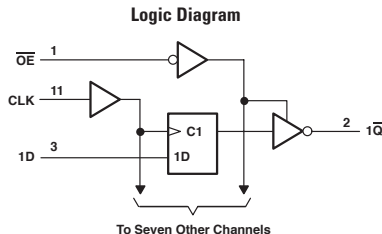
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	ACT 11	SN74 ACT
t_{pL}			MIN	15	2	20	24	25	24	3.3	4	5	5	6
t_{su}			MIN	15	2	13	15	13	15	2.1	3.5	4.5	3.5	4
t_{h}			MIN	7	3	5	11	5	12	2.1	2	1	3.5	2.5
t_{PLH}	D	\overline{Q}	MAX	19	7.5	38	50	44	51	6.4	9.8	11	11.3	11.5
t_{PHL}				13	7	38	50	44	51	6.6	8	10.5	9.5	11
t_{PLH}	LE (CD74: \overline{LE})	\overline{Q}	MAX	23	9	44	53	44	57	7.3	11.3	11.5	13	11.5
t_{PHL}				18	8	44	53	44	57	7.3	10.3	11	12.2	11.5
t_{PZH}	\overline{OE}	\overline{Q}	MAX	17	6.5	38	45	44	53	5.7	10.8	10.5	12.5	11
t_{PZL}				18	9.5	38	45	44	53	6.7	9.7	10.5	12	11
t_{PHZ}	\overline{OE}	\overline{Q}	MAX	10	6.5	38	45	44	45	6.9	11.4	11	12.8	11
t_{PLZ}				16	7	38	45	44	45	6.5	8.9	11	10.3	11

UNIT: ns

OCTAL D-TYPE EDEG-TRIGGERED FLIP-FLOPS

- 3-State Bus-Driving Inverting Outputs
- '534 Have Inverted Outputs, But Otherwise Are Functionally Equivalent to '374
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



FUNCTION TABLE

INPUTS			OUTPUT
\overline{OE}	CLK	D	\overline{Q}
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	CD74 AC	ACT 11	SN74 ACT	UNIT
I_{CC}	MAX	31	128	0.08	0.16	0.08	0.16	30	0.08	0.04	0.16	0.08	0.04	mA
I_{OH}	MAX	-2.6	-15	-6	-6	-6	-6	-32	-24	-24	-24	-24	-24	mA
I_{OL}	MAX	24	48	6	6	6	6	64	24	24	24	24	24	mA

SWITCHING CHARACTERISTICS

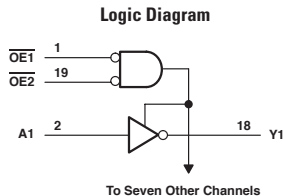
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	ABT	AC 11	SN74 AC	CD74 AC
t_{max}			MIN	35	125	25	20	25	16	125	75	140	125
t_w	CLK "H" CLK "L"		MIN	14	4	20	24	20	30	3.5	6.5	4	4
				14	3	20	24	20	30	3.5	6.5	4	4
t_{su}			MIN	10	2	25	18	25	30	1.6	3.5	4	2
t_h				0	2	5	5	5	5	2	4.5	1.5	2
t_{PLH}	CLK (CD74: CP)	\overline{Q}	MAX	12	8	45	50	45	53	6.7	11.7	12	11.3
t_{PHL}				16	9	45	50	45	53	7.6	12.1	11	11.3
t_{PZH}	\overline{OE}	\overline{Q}	MAX	17	6	38	45	37	53	5	10.4	11.5	14.5
t_{PZL}				18	10	38	45	37	53	6.8	10.4	11.5	14.5
t_{PHZ}	\overline{OE}	\overline{Q}	MAX	10	6	38	45	37	45	7.3	11.6	12.5	14.5
t_{PLZ}				14	6	38	45	37	45	6.5	9.2	11	14.5

PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT 11	SN74 ACT
t_{max}			MIN	55	120
t_w	CLK "H" CLK "L"		MIN	9	3.5
				9	3.5
t_{su}			MIN	3	4
t_h				5.5	1.5
t_{PLH}	CLK (CD74: CP)	\overline{Q}	MAX	14.5	12.5
t_{PHL}				15	12
t_{PZH}	\overline{OE}	\overline{Q}	MAX	13.3	12.5
t_{PZL}				13.5	11.5
t_{PHZ}	\overline{OE}	\overline{Q}	MAX	13.5	13.5
t_{PLZ}				12	10.5

UNIT f_{max} : MHz, other: ns

OCTAL BUFFERS AND LINE DRIVERS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Schmitt-Triggerred Inputs (SN74LS540)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	CD74 AC	CD74 ACT	AHC	AHCT	UNIT
I _{CC}	MAX	52	22	22	0.08	0.16	0.08	0.16	71	30	5	0.16	0.16	0.04	0.04	mA
I _{OH}	MAX	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	-24	-24	-8	-8	mA
I _{OL}	MAX	24	24	48	6	6	6	6	64	64	64	24	24	8	8	mA

PARAMETER	MAX or MIN	LV 3V	LV 5V	LVC 3V	UNIT
I _{CC}	MAX	-	0.02	0.01	mA
I _{OH}	MAX	-8	-16	-24	mA
I _{OL}	MAX	8	16	24	mA

SWITCHING CHARACTERISTICS

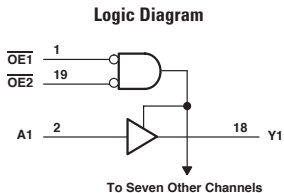
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V
t _{PLH}	A	Y (CD74: \bar{Y})	MAX	15	12	12	25	33	25	36	6.9	4.8	3.8
t _{PHL}				15	9	9	25	33	25	36	4	4.8	3.8
t _{PDZ}	\overline{OE}	Y (CD74: \bar{Y})	MAX	25	15	15	38	48	38	53	10.1	5.9	5.2
t _{PZL}				38	20	20	38	48	38	53	11.3	6.4	5.3
t _{PHZ}	\overline{OE}	Y (CD74: \bar{Y})	MAX	25	10	10	38	48	38	53	9	7.3	5.6
t _{PLZ}				18	12	12	38	48	38	53	8.5	6.2	5

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t _{PLH}	A	Y (CD74: \bar{Y})	MAX	68	7.2	8	10	12	8	5.3
t _{PHL}				68	7.2	8	10	12	8	5.3
t _{PDZ}	\overline{OE}	Y (CD74: \bar{Y})	MAX	12	13.4	10.5	12	16	10.5	6.6
t _{PZL}				12	13.4	10.5	12	16	10.5	6.6
t _{PHZ}	\overline{OE}	Y (CD74: \bar{Y})	MAX	12	13.4	10	12	17.5	10	7.4
t _{PLZ}				12	13.4	10	12	17.5	10	7.4

UNIT: ns

OCTAL BUFFERS AND LINE DRIVERS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- P-N-P Inputs Reduce D-C Loading
- Schmitt-Triggered Inputs (SN74LS541)



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	CD74 AC	CD74 ACT	AHC	UNIT
I _{CC}	MAX	55	25	25	75	0.08	0.16	0.08	0.16	72	30	5	0.16	0.16	0.04	mA
I _{OH}	MAX	-15	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	-24	-24	-8	mA
I _{OL}	MAX	24	24	48	64	6	6	6	6	64	64	64	24	24	8	mA

PARAMETER	MAX or MIN	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I _{CC}	MAX	0.04	-	0.02	0.01	mA
I _{OH}	MAX	-8	-8	-16	-24	mA
I _{OL}	MAX	8	8	16	24	mA

SWITCHING CHARACTERISTICS

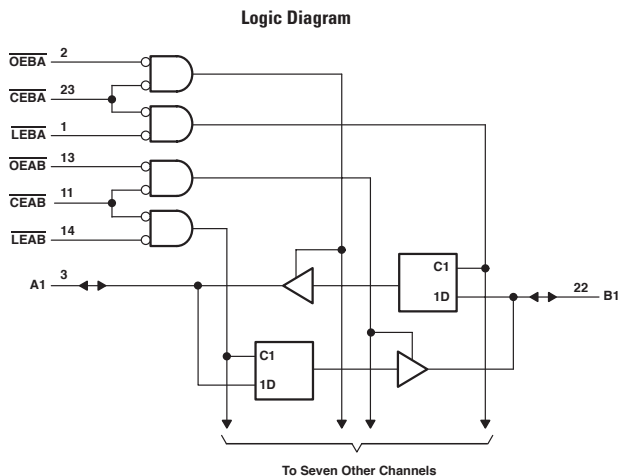
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT
t _{PLH}	A	Y	MAX	15	14	14	6	29	35	29	42	6	3.6
t _{PHL}				18	10	10	6	29	35	29	42	8.2	3.9
t _{PZH}	\overline{OE}	Y	MAX	32	15	15	9.5	38	48	38	53	10.7	4
t _{PZL}				38	20	20	9.5	38	48	38	53	11.5	5.9
t _{PHZ}	\overline{OE}	Y	MAX	29	10	10	6.5	38	48	38	53	8.6	5.8
t _{PLZ}				18	12	12	6	38	48	38	53	8.6	4.4

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	CD74 AC	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
t _{PLH}	A	Y	MAX	3.5	7.8	8.2	8	9.5	12	8	5.1
t _{PHL}				3.5	7.8	8.2	8	9.5	12	8	5.1
t _{PZH}	\overline{OE}	Y	MAX	5.2	12	13.4	10.5	12	16	10.5	7
t _{PZL}				5.3	12	13.4	10.5	12	16	10.5	7
t _{PHZ}	\overline{OE}	Y	MAX	5.6	12	13.4	10	12	17.5	10	7
t _{PLZ}				5	12	13.4	10	12	17.5	10	7

UNIT: ns

OCTAL REGISTERED TRANSCEIVERS

- Back-to-Back Registers for Storage
- 3-State True Outputs
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



FUNCTION TABLE†

INPUTS				OUTPUT B
CEAB	LEAB	OEAB	A	
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ₀ ‡
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

‡ Output level before the indicated steady-state input conditions were established

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	F	SN74 BCT	ABT	LVTH 3V	ACT 11	LVC 3V	UNIT
ICCH		MAX	100	8	0.25	0.19	0.08	0.01	mA
ICCL		MAX	125	71	30	5	0.08	0.01	mA
ICCZ		MAX	125	15	0.25	0.19	0.08	0.01	mA
IOH	A	MAX	-3	-15	-32	-32	-24	-24	mA
	B	MAX	-15	-15	-32	-32	-24	-24	mA
IOL	A	MAX	24	64	64	64	24	24	mA
	B	MAX	64	64	64	64	24	24	mA

SWITCHING CHARACTERISTICS

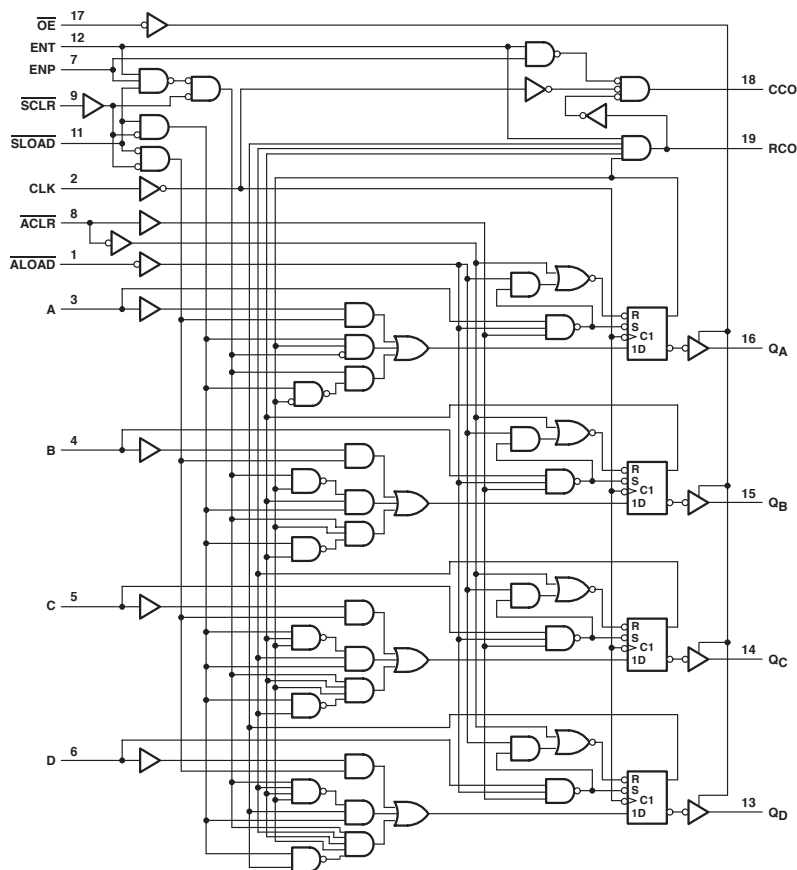
PARAMETER		INPUT	OUTPUT	MAX or MIN	F	SN74 BCT	ABT	LVTH 3V	ACT 11	LVC 3V
t _r				MIN	5	7	3.5	3.3	4	3.3
tsu	LE ' before 'H'			MIN	3.5	4.5	3.5	0.4	2.5	1.6
	LE ' before 'L'				3.5	4.5	3	1	2.5	1.6
	CE ' before 'H'				-	-	3.5	0.2	3	1.6
	CE ' before 'L'				-	-	3	0.7	3	1.6
th	LE ' after 'H'			MIN	3.5	1.5	0.5	1.5	2	2.1
	LE ' after 'L'				3.5	1.5	0.5	1.3	2	2.1
	CE ' after 'H'				-	-	0.5	1.6	1.5	2.1
	CE ' after 'L'				-	-	0.5	1.4	1.5	2.1
IPLH		A or B	B or A	MAX	8.5	8.8	6.9	3.7	10.2	7
IPLH				MAX	7.5	9.6	6.9	3.7	12.1	7
IPLH		LEBA	A	MAX	12.5	12.9	6.6	4.7	11.2	8.5
IPLH				MAX	12.5	12.7	7.1	4.7	13.2	8.5
IPLH		LEAB	B	MAX	12.5	12.9	6.6	4.7	11.2	8.5
IPLH				MAX	12.5	12.7	7.1	4.7	13.2	8.5
IPLH				MAX	10	10.7	6.4	4.9	11.5	7.7
IPLH				MAX	12	12.3	7.5	4.9	15.3	7.7
IPLH				MAX	9	8.1	8.4	5.3	10.4	7
IPLH				MAX	8.5	7.2	8	5.3	10.5	7
IPLH				MAX	10	12	6.4	5.3	12.2	8
IPLH				MAX	12	13.5	7.5	5.3	16	8
IPLH				MAX	9	8.5	8.4	5.4	11	7
IPLH				MAX	8.5	7.6	8	5.4	11.1	7

UNIT: ns

SYNCHRONOUS 4-BIT COUNTER

- 3-State Outputs
- Choice of Asynchronous or Synchronous Clearing and Loading
- Internal Look-Ahead Circuitry for Fast Cascading

Logic Diagram



FUNCTION TABLE

INPUTS								OPERATION
OE	ACL	ALOAD	SCLR	SLOAD	ENT	ENP	CLK	
H	X	X	X	X	X	X	X	Q outputs disabled
L	L	X	X	X	X	X	X	Asynchronous clear
L	H	L	X	X	X	X	X	Asynchronous load
L	H	H	L	X	X	X	↑	Synchronous clear
L	H	H	H	L	X	X	↑	Synchronous load
L	H	H	H	H	H	H	↑	Count
L	H	H	H	H	L	X	X	Inhibit counting
L	H	H	H	H	X	L	X	Inhibit counting

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
Icc		MAX	36	mA
Ioh	OUTPUT Q	MAX	-2.6	mA
	CCO & RCO	MAX	-0.4	mA
Iol	OUTPUT Q	MAX	24	mA
	CCO & RCO	MAX	8	mA

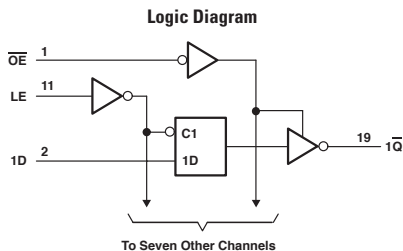
SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS
fmax				MIN	30
tw	CLK "H"			MIN	16.5
	CLK "L"				16.5
tsu	ENP or ENT	H			20
		L			20
	A, B, C, D				20
	SCLR	L			15
		H			30
	SLOAD	L			15
		H			30
th			MIN	0	
tpLH	CLK		Q	MAX	12
tpHL	CLK		Q	MAX	18
tpLH	CLK		RCO	MAX	29
tpHL	CLK		RCO	MAX	24
tpLH	ALOAD		Q	MAX	35
tpHL	ALOAD		Q	MAX	23
tpLH	ALOAD		CCO	MAX	55
tpHL	ALOAD		CCO	MAX	33
tpLH	ENT		RCO	MAX	16
tpHL	ENT		RCO	MAX	14
tpHL	ACL		Q	MAX	22

UNIT fmax : MHz, other : ns

OCTAL D-TYPE TRANSPARENT LATCHES WITH INVERTED OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout



FUNCTION TABLE

INPUTS			OUTPUT \bar{Q}
\overline{OE}	ENABLE LE	D	
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT	UNIT
I_{CC}	MAX	29	0.08	0.16	0.08	0.16	0.08	0.16	0.04	mA
I_{OH}	MAX	-2.6	-6	-6	-6	-6	-24	-24	-24	mA
I_{OL}	MAX	24	6	6	6	6	24	24	24	mA

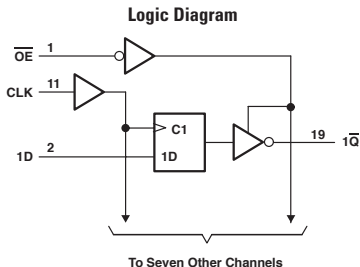
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	CD74 AC	SN74 ACT
t_r			MIN	15	20	24	25	24	5	4	3
t_{su}				10	13	15	13	15	2.5	2	4.5
t_h				10	5	4	10	5	2	3	0
t_{PLH}	D	\bar{Q}	MAX	18	44	45	44	45	11.5	10.5	12.5
t_{PHL}				14	44	45	44	45	11	10.5	11
t_{PLH}	LE	\bar{Q}	MAX	22	44	50	44	53	11	12	11.5
t_{PHL}	(CD74: LE)			21	44	50	44	53	9.5	12	10.5
t_{PZH}	\overline{OE}	\bar{Q}	MAX	18	38	45	44	53	10	10.5	10
t_{PZL}				18	38	45	44	53	9.5	10.5	9.5
t_{PHZ}	\overline{OE}	\bar{Q}	MAX	10	38	45	44	53	12	11.5	11.5
t_{PLZ}				15	38	45	44	53	9	11.5	8.5

UNIT: ns

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout



FUNCTION TABLE

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	L
L	↑	L	H
L	L	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	SN74 ACT	UNIT
I _{CC}	MAX	30	0.08	0.16	0.08	0.16	0.04	0.04	mA
I _{DH}	MAX	-2.6	-6	-6	-6	-6	-24	-24	mA
I _{OL}	MAX	24	6	6	6	6	24	24	mA

SWITCHING CHARACTERISTICS

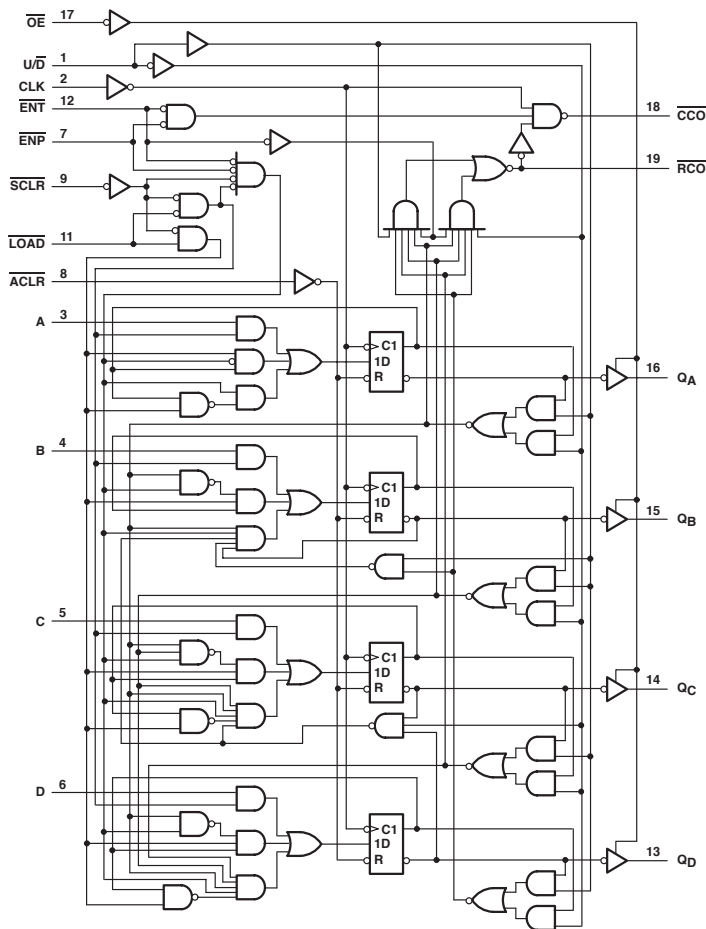
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 AC	SN74 ACT
t _{max}			MIN	30	25	20	25	16	85	75
t _w	CLK H		MIN	14	20	24	20	30	5	3.5
				14	20	24	20	30	5	3.5
CLK L	15	25		18	25	30	2.5	3		
	0	5		5	5	3	2	1		
t _{su}	CLK *									
t _h	CLK *									
t _{PHL}	CLK	\bar{Q}	MAX	14	45	50	45	53	11.5	11.5
t _{PHL}				14	45	50	45	53	10.5	10.5
t _{PZH}	\bar{OE}	\bar{Q}	MAX	18	38	45	38	53	9.5	9.5
t _{PZL}				18	38	45	38	53	9.5	9.5
t _{PHZ}	\bar{OE}	\bar{Q}	MAX	10	38	41	38	45	11.5	11.5
t _{PLZ}				15	38	41	38	45	9	8.5

UNIT f_{max} : MHz, other : ns

SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

- 3-State Q Outputs Drive Bus Lines Directly
- Fully Synchronous Clear, Count, and Load
- Asynchronous Clear Is Also Provided
- Fully Cascadable

Logic Diagram



FUNCTION TABLE

INPUTS									OPERATION
OE	ACLR	SCLR	LOAD	ENT	ENP	U/D	CLK		
H	X	X	X	X	X	X	X	X	Q outputs disabled
L	L	X	X	X	X	X	X	X	Asynchronous clear
L	H	L	X	X	X	X	X	↑	Synchronous clear
L	H	H	L	X	X	X	X	↑	Load
L	H	H	H	L	L	L	H	↑	Count up
L	H	H	H	L	L	L	L	↑	Count down
L	H	H	H	H	X	X	X	X	Inhibit count
L	H	H	H	X	H	X	X	X	Inhibit count

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I _{CC}		MAX	32	mA
I _{OH}	OUTPUT Q	MAX	-2.6	mA
	CCO & RCO		-0.4	mA
I _{OL}	OUTPUT Q	MAX	24	mA
	CCO & RCO		8	mA

SWITCHING CHARACTERISTICS

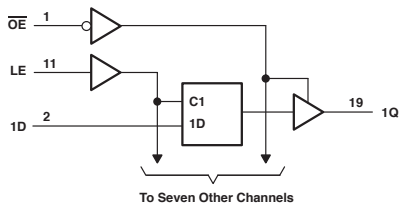
PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS
t _{max}				MIN	30
t _w	ACLR, LOAD			MIN	15
	CLK 'H'				16.5
	CLK 'L'				16.5
t _{su}	Data at A, B, C, D			MIN	20
	ENP, ENT	High			30
		Low			20
	SCLR	High			15
		Low			30
	LOAD	High			15
		Low			30
	U/D				30
	ACLR				10
	t _h				MIN
t _{PLH}		CLK	ANY Q	MAX	13
t _{PHL}					16
t _{PLH}		CLK	\overline{RCO}	MAX	28
t _{PHL}					19
t _{PLH}		\overline{ENT}	\overline{RCO}	MAX	15
t _{PHL}					13
t _{PHL}		\overline{ACLR}	Q	MAX	20
t _{PZH}		\overline{OE}	Q	MAX	18
t _{PZL}					24
t _{PHZ}		\overline{OE}	Q	MAX	10
t _{PLZ}					13

 UNIT f_{max} : MHz, other : ns

OCTAL D-TYPE TRANSPARENT LATCHES

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT Q
\overline{OE}	ENABLE LE	D	
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	SN74 AC	CD74 AC	SN74 ACT	UNIT
I_{CC}	MAX	27	106	55	0.08	0.16	0.08	0.16	62	30	5	0.04	0.16	0.04	mA
I_{OH}	MAX	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-32	-24	-24	-24	mA
I_{OL}	MAX	24	48	24	6	6	6	6	64	64	64	24	24	24	mA

PARAMETER	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I_{CC}	MAX	0.16	0.04	0.04	-	0.02	0.01	mA
I_{OH}	MAX	-24	-8	-8	-8	-16	-24	mA
I_{OL}	MAX	24	8	8	8	16	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V
				t _r	t _{su}	t _h	t _r	t _{su}	t _h	t _r	t _{su}	t _h	t _r
t _r	LE		MIN	10	4.5	6	20	24	25	24	4	3.3	3.3
				10	2	2	13	15	13	20	1	1.9	0.7
				7	3	3	5	12	5	15	4	1.8	1.5
t _{PLH}	D	Q	MAX	14	8	8	44	53	44	53	8.4	5.9	3.9
				14	7	6	44	53	44	53	9.6	6.2	3.9
t _{PHL}	LE	Q	MAX	20	13	13	44	53	44	53	8.1	6.6	4.2
				19	7.5	8	44	53	44	53	7.8	7.2	4.2
t _{PZH}	\overline{OE}	Q	MAX	18	6.5	12	38	45	44	53	10.4	5.2	5.1
				18	9.5	8.5	38	45	44	53	11	6.7	5.1
t _{PHZ}	\overline{OE}	Q	MAX	10	6.5	7.5	38	45	44	53	6	7.1	4.9
				15	7	6	38	45	44	53	6	6.5	4.6

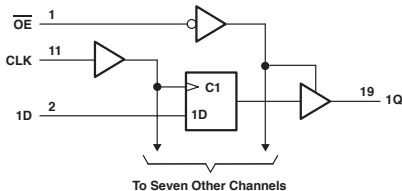
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT	AHC	AHCT	LV 5V	LV 3V	LVC 3V
				t _r	t _{su}	t _h	t _r	t _{su}	t _h	t _r	t _{su}	t _h
t _r	LE		MIN	5	4	4	4	5	5	5	5	3.3
				3.5	2	3.5	2	3.5	3.5	3.5	3.5	2
				2	3	0	3	1.5	1.5	1.5	1.5	1.5
t _{PLH}	D	Q	MAX	11.5	8.5	12	10.4	10	7.5	10	16.5	6.9
				11	8.5	12	10.4	10	10	10	16.5	6.9
t _{PHL}	LE (CD74AC/ACT: LE)	Q	MAX	11	12	12	12.5	11	8.5	11	17.5	7.7
				10	12	10.5	12.5	11	10	11	17.5	7.7
t _{PZH}	\overline{OE}	Q	MAX	10	10.5	11	13.5	11	8	11	17	7.5
				9.5	10.5	10.5	13.5	11	11	11	17	7.5
t _{PHZ}	\overline{OE}	Q	MAX	12	11.5	12.5	12.5	11	12	11	16.5	6.5
				9	11.5	9.5	12.5	11	10.5	11	16.5	6.5

UNIT: ns

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- 3-State Buffer-Type Noninverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	↑	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V	SN74 AC	CD74 AC	SN74 ACT	UNIT
I _{CC}	MAX	28	134	86	0.08	0.16	0.08	0.16	62	30	5	0.04	0.16	0.04	mA
I _{OH}	MAX	-2.6	-15	-3	-6	-6	-6	-6	-15	-32	-24	-24	-24	-24	mA
I _{OL}	MAX	24	48	24	6	6	6	6	64	64	24	24	24	24	mA

PARAMETER	MAX or MIN	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V	UNIT
I _{CC}	MAX	0.16	0.04	0.04	-	0.02	0.01	mA
I _{OH}	MAX	-24	-8	-8	-8	-16	-24	mA
I _{OL}	MAX	24	8	8	8	16	24	mA

SWITCHING CHARACTERISTICS

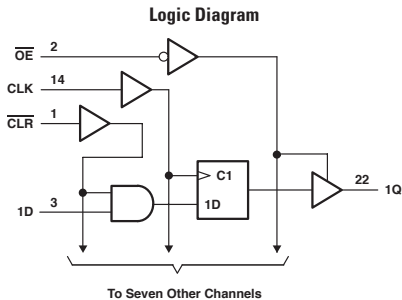
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	F	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	LVTH 3V
f _{max}			MIN	35	125	100	24	20	24	20	77	150	150
t _w			MIN	14	5.5	7	20	24	20	24	6.5	3.3	3.3
t _{SU}			MIN	15	5.5	2	25	18	25	18	6	1.5	2
t _H			MIN	0	0	2	5	5	5	0	1.8	0.3	
t _{PLH}	CLK	Q	MAX	14	8	10	45	50	45	50	10	6.8	4.5
t _{PHL}				14	9	10	45	50	45	50	8.9	7.1	4.5
t _{PZH}	OE	Q	MAX	18	6	12.5	38	45	38	45	10.4	5.1	4.8
t _{PZL}				18	10	8.5	38	45	38	45	10.9	6.7	4.8
t _{PHZ}	OE	Q	MAX	10	6	8	38	41	38	42	7.5	7	4.8
t _{PLZ}				12	6	6.5	38	41	38	42	6.4	6.5	4.4

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 AC	CD74 AC	SN74 ACT	CD74 ACT	AHC	AHCT	LV 3V	LV 5V	LVC 3V
f _{max}			MIN	85	125	85	110	75	75	45	75	100
t _w			MIN	5	4	4	4.5	5	5.5	5	5	3.3
t _{SU}			MIN	2	2	2.5	2	3	3.5	3.5	3.5	2
t _H			MIN	1.5	2	0	3	1.5	1.5	1.5	1.5	1.5
t _{PLH}	CLK	Q	MAX	11	10.8	12	11.2	12	12	19	12	7
t _{PHL}				9.5	10.8	11	11.2	12	12	19	12	7
t _{PZH}	OE	Q	MAX	9	14.5	10	14.5	12.5	12.5	18.5	12.5	7.5
t _{PZL}				9	14.5	10	14.5	12.5	12.5	18.5	12.5	7.5
t _{PHZ}	OE	Q	MAX	10.5	14.5	11.5	14.5	11.5	11.5	17	11.5	6.4
t _{PLZ}				8.5	14.5	9	14.5	11.5	11.5	17	11.5	6.4

UNIT f_{max}: MHz, other: ns

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- 3-State Buffer-Type Noninverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Synchronous Clear



FUNCTION TABLE

INPUTS				OUTPUT
OE	CLR	CLK	D	Q
L	L	↑	X	L
L	H	↑	H	H
L	H	↑	L	L
L	H	L	X	Q ₀
H	X	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I _{CC}	MAX	30	142	mA
I _{OH}	MAX	-2.6	-15	mA
I _{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

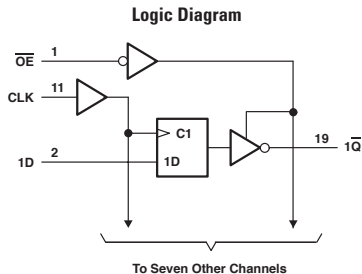
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
f _{max}			MIN	30	90
t _w	CLK	H	MIN	16.5	5.5
	CLK	L			5.5
t _{su}	DATA			15	5.5
	CLR	L			6.5
t _h	DATA			0	3
	CLR				0
t _{PLH}	CLK	Q	MAX	14	8
t _{PHL}				14	9
t _{PZH}	OC	Q	MAX	18	6
t _{PZL}				18	10
t _{PHZ}	OC	Q	MAX	10	6
t _{PLZ}				13	6

UNIT f_{max} : MHz, other : ns

576

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Functionally Equivalent to '576, Except for Having Inverted Outputs



FUNCTION TABLE

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	L
L	↑	L	H
L	L	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I _{CC}	MAX	30	135	mA
I _{OH}	MAX	-2.6	-15	mA
I _{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

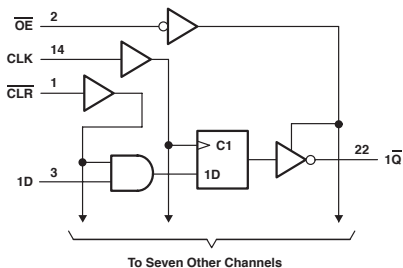
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
f _{max}			MIN	30	125
t _w	H		MIN	16.5	4
	L				2
t _{su}	DATA			15	2
t _h	DATA			0	2
t _{PLH}	CLK	Q̄	MAX	14	8
t _{PHL}				14	9
t _{PZH}	OE	Q̄	MAX	18	6
t _{PZL}				18	10
t _{PHZ}	OE	Q̄	MAX	10	6
t _{PLZ}				15	6

UNIT f_{max} : MHz, other : ns

OCTAL D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- 3-State Buffer-Type Inverting Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Synchronous Clear

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE	CLR	CLK	D	\bar{Q}
L	L	↑	X	H
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	\bar{Q}_0
H	X	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	30	142	mA
I_{OH}	MAX	-2.6	-15	mA
I_{OL}	MAX	24	48	mA

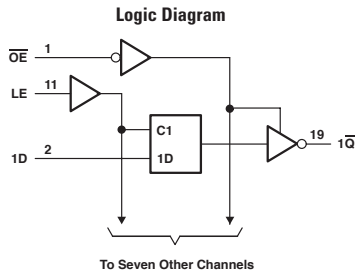
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
f_{max}			MIN	30	125
t_r			MIN	16.5	4
t_{su}	DATA			15	2
t_h	CLR			0	2
t_{PLH}	CLK	\bar{Q}	MAX	14	8
t_{PHL}				14	9
t_{PZH}	\overline{OE}	\bar{Q}	MAX	18	6
t_{PZL}				18	10
t_{PHZ}	\overline{OE}	\bar{Q}	MAX	10	6
t_{PLZ}				15	6

UNIT f_{max} : MHz, other : ns

OCTAL D-TYPE TRANSPARENT LATCHES WITH INVERTED OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Inverting-Logic Outputs
- Bus-Structured Pinout



FUNCTION TABLE

INPUTS			OUTPUT Q
$\overline{\text{OE}}$	ENABLE LE	D	
L	H	H	L
L	H	L	H
L	L	X	$\overline{\text{Q}}_0$
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	29	115	mA
I_{OH}	MAX	-2.6	-15	mA
I_{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

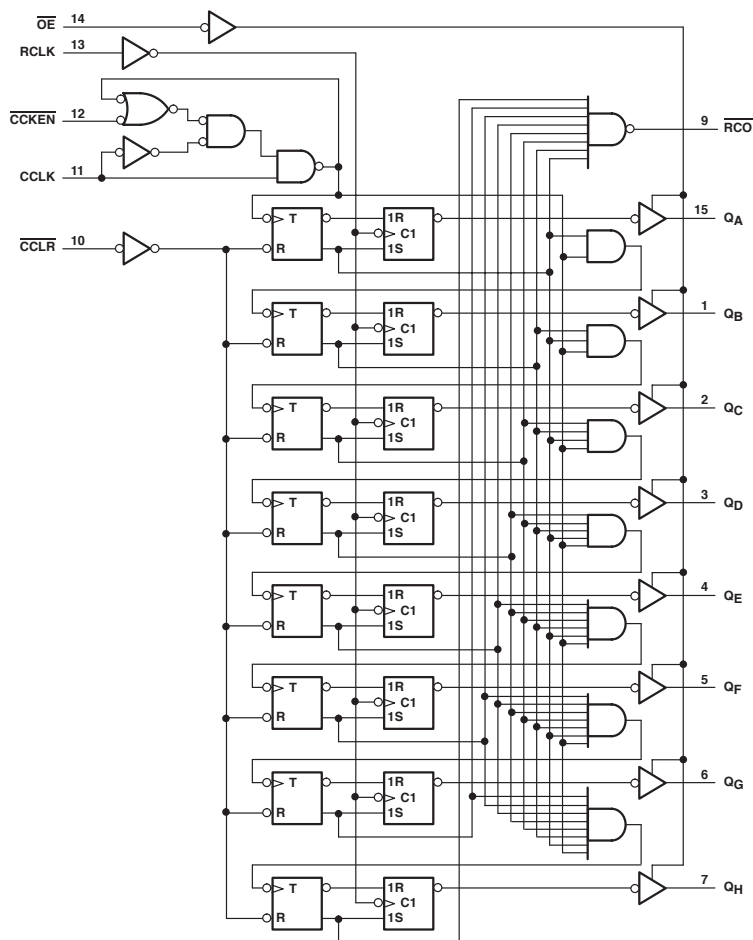
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t_c	C			15	2
t_{SU}	C		MIN	10	2
t_{H}	C			10	3
t_{PLH}	D	$\overline{\text{Q}}$	MAX	18	7.5
t_{PHL}				14	7
t_{PLH}	LE	$\overline{\text{Q}}$	MAX	22	9
t_{PHL}				21	8
t_{PZH}	$\overline{\text{OE}}$	$\overline{\text{Q}}$	MAX	18	6.5
t_{PZL}				18	9.5
t_{PHZ}	$\overline{\text{OE}}$	$\overline{\text{Q}}$	MAX	10	6.5
t_{PLZ}				15	7

UNIT: ns

8-BIT BINARY COUNTER WITH OUTPUT REGISTER

- Parallel Register Outputs
- Counter Has Direct Clear
- 3-State Outputs
- Guaranteed Counter Frequency: DC to 20MHz

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	SN74 HC	UNIT
I _{CC}		MAX	65	0.08	mA
I _{OH}	\overline{RCO}	MAX	-1	-4	mA
	Q	MAX	-2.6	-6	mA
I _{OL}	\overline{RCO}	MAX	16	4	mA
	Q	MAX	24	6	mA

SWITCHING CHARACTERISTICS

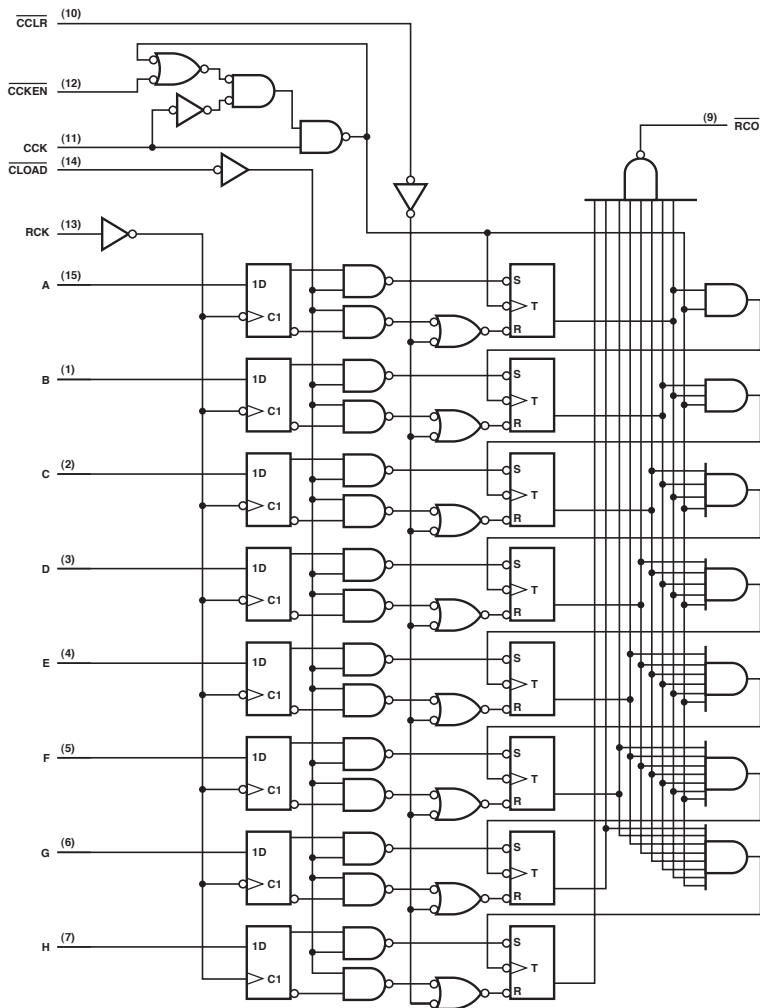
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
f _{max}		CCK	\overline{RCO}	MIN	20	13
t _w	CCK			MIN	25	31
	\overline{CCLR}				20	25
	RCK				20	31
t _{su}	\overline{CCLR} ' before CCK '			MIN	20	25
	CCK ' before RCK '				40	25
t _{PLH}		CCK '	\overline{RCO}	MAX	22	45
t _{PHL}					30	45
t _{PLH}		\overline{CCLR} '	\overline{RCO}	MAX	45	39
t _{PLH}		RCK '	Q	MAX	18	42
t _{PHL}					33	42
t _{PZH}		\overline{G} '	Q	MAX	38	37
t _{PZL}					45	37
t _{PHZ}		\overline{G} '	Q	MAX	30	37
t _{PLZ}					38	37

UNIT f_{max} : MHz, other : ns

8-BIT BINARY COUNTER WITH INPUT REGISTER

- Parallel Register Inputs
- Counter Has Directly Overriding Load and Clear
- Accurate Counter Frequency: DC to 20MHz

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I _{CC}	MAX	60	mA
I _{OH}	MAX	-1	mA
I _{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

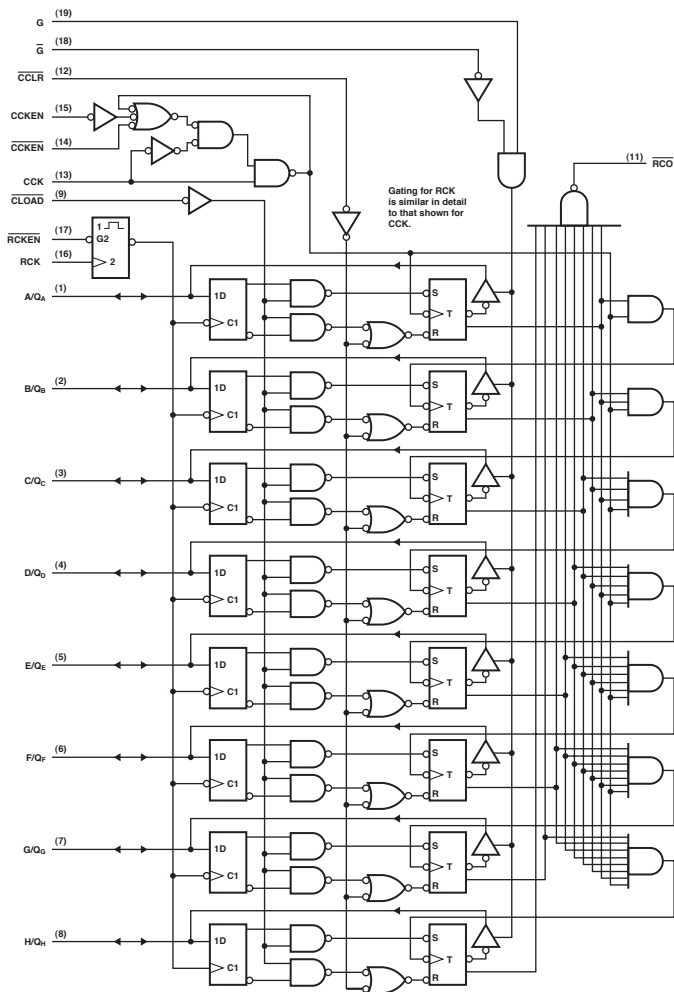
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
f _{max}	CCK	\overline{RCO}	MIN	20
t _w	CCK		MIN	25
	\overline{CCLR}			20
	RCK			20
	\overline{CLOAD}			40
t _{su}	\overline{CCLR} * before CCK *		MIN	20
	\overline{CLOAD} * before CCK *			20
	RCK * before \overline{CLOAD} *			30
	A to H before RCK			20
t _h			MIN	0
t _{PLH}	CCK *	\overline{RCO}	MAX	23
t _{PHL}				30
t _{PLH}	\overline{CLOAD} ,	\overline{RCO}	MAX	47
t _{PHL}				17
t _{PLH}	\overline{CCLR} ,	\overline{RCO}	MAX	45
t _{PLH}	RCK *	\overline{RCO} Q	MAX	53
t _{PHL}				45

UNIT f_{max} : MHz, other : ns

8-BIT BINARY COUNTER WITH INPUT REGISTER

- Parallel 3-State I/O: Register Inputs/Counter Outputs
- Counter Has Directly Overriding Load and Clear
- Accurate Counter Frequency: DC to 20MHz
- 74ACT1xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	ACT 11	UNIT
I _{CC}		MAX	85	0.08	mA
I _{OH}	\overline{RCO}	MAX	-1	-24	mA
	Q	MAX	-2.6	-24	mA
I _{OL}	\overline{RCO}	MAX	16	24	mA
	Q	MAX	24	24	mA

SWITCHING CHARACTERISTICS

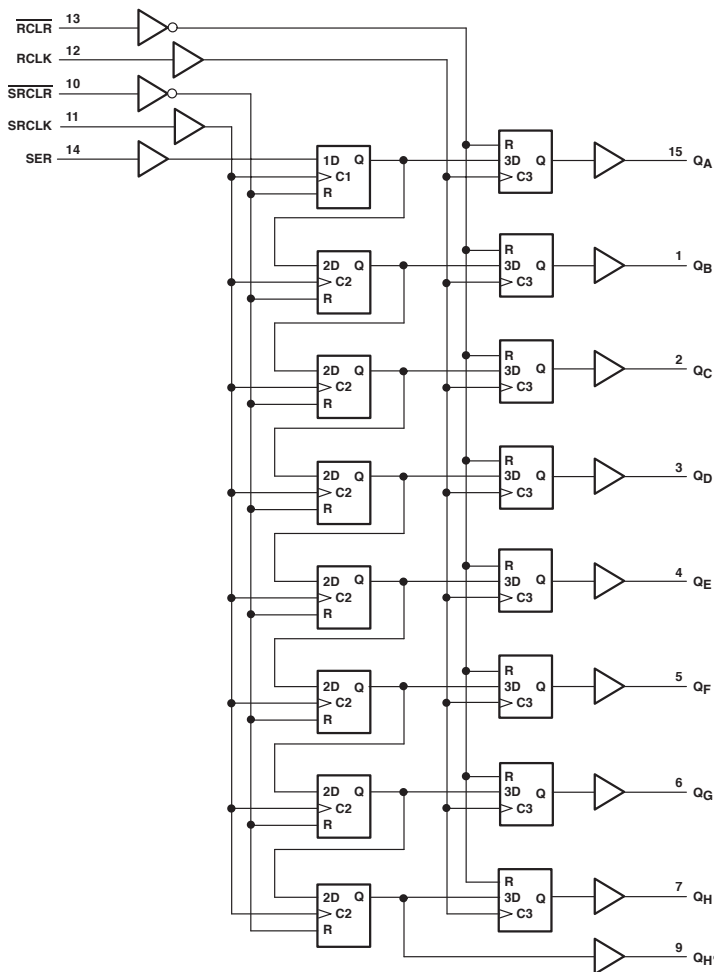
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	ACT 11
f _{max}		CCK	\overline{RCO}	MIN	20	52
t _w	CCK			MIN	25	9.6
	\overline{CCLR}				20	7.6
	RCK				20	5.8
	\overline{CLOAD}				40	6.2
t _{su}	\overline{CCLR} * before CCK *			MIN	20	1.2
	\overline{CLOAD} * before CCK *				20	5.1
	RCK * before \overline{CLOAD} *				30	7.4
	A to H before RCK				20	2.4
t _h				MIN	0	0.8
t _{PLH}	CCK *	Q	MAX	21	15.1	
t _{PHL}				39	15	
t _{PLH}	\overline{CLOAD} ,	Q	MAX	51	19.1	
t _{PHL}				42	21.7	
t _{PHL}	\overline{CCLR} ,	Q	MAX	38	16	

UNIT f_{max} : MHz, other : ns

8-BIT SHIFT REGISTER WITH OUTPUT LATCHES

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Shift and Storage Registers
- Guaranteed Shift Frequency: DC to 20MHz

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	SN74 HC	AHC	AHCT	LV 3V	LV 5V	UNIT
I _{CC}		MAX	65	0.08	0.04	0.02	-	0.02	mA
I _{OH}	QH'	MAX	-1	-4	-8	-8	-6	-12	mA
	Q	MAX	-2.6	-6	-8	-8	-6	-12	mA
I _{OL}	QH'	MAX	16	4	8	8	6	12	mA
	QA to QH	MAX	24	6	8	8	6	12	mA

SWITCHING CHARACTERISTICS

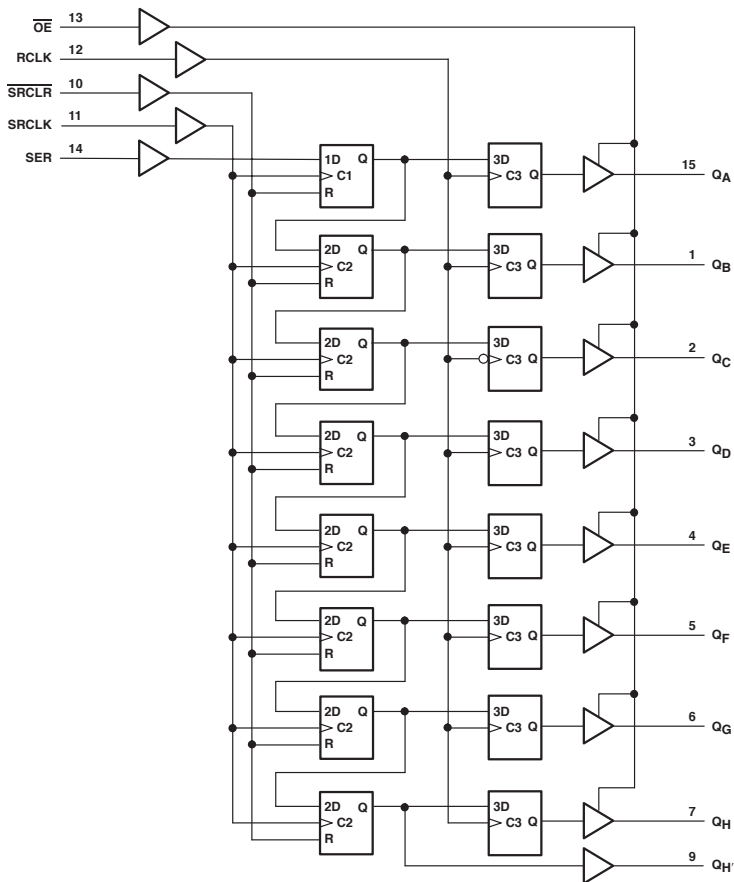
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	SN74 HC	AHC	AHCT	LV 3V	LV 5V	
t _w	SRCK			MIN	25	20	5	5.5	5.5	5	
	RCK				20	20	5	5.5	5.5	5	
t _{su}	SRCLR ' to SRCK '			MIN	20	10	3.3	3.3	4.8	3.3	
	SER to SRCK '				20	22	3	3	3.5	3	
	SRCK ' to RCK '				40	22	5	5	8.5	5	
	SRCLR , to RCK '				40	13	5	5	9	5	
	RCLR ' to RCK '				20	5	3.7	3.8	5.3	3.7	
	RCLR , to RCK '										
t _h					MIN	0	5	2	2	1.5	2
t _{PLH}	SRCK '			QH'	MAX	18	37	9.1	9.1	12.4	9.1
t _{PHL}		23	37			10.1	10.1	13.9	10.1		
t _{PLH}	RCK '	QA to QH	MAX	18	37	8.3	8.3	11.1	8.3		
t _{PHL}				30	37	9.7	9.7	13.1	9.7		
t _{PHL}	SRCLR ,	QH'	MAX	33	37	10.7	10.1	14	10.1		
t _{PHL}	RCLR ,	QA to QH		57	31	10.1	10.7	14.4	10.7		

UNIT: ns

8-BIT SHIFT REGISTER WITH OUTPUT LATCHES

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- 3-State Outputs
- Shift Register Has Direct Clear
- Accurate Shift Frequency: DC to 20MHz

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	SN74 HC	AHC	AHCT	LV 3V	LV 5V	UNIT
I _{CC}		MAX	65	0.08	0.04	0.04	-	0.02	mA
I _{OH}	QH'	MAX	-1	-4	-8	-8	-8	-16	mA
	QA to QH	MAX	-26	-6	-8	-8	-8	-16	mA
I _{OL}	QH'	MAX	16	4	8	8	8	16	mA
	QA to QH	MAX	24	6	8	8	8	16	mA

SWITCHING CHARACTERISTICS

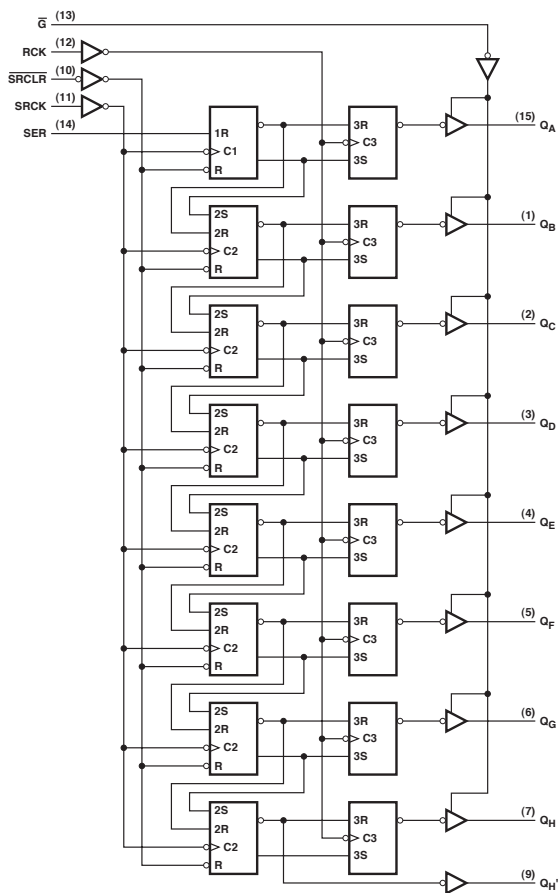
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	HC	AHC	AHCT	LV 3V	LV 5V
t _w	SRCK			MIN	25	20	5	5.5	5.5	5
	RCK				20	20	5	5.5	5.5	5
t _{su}	SRCLR ' to SRCK '			MIN	20	12	2.5	3.8	3	2.5
	SER to SRCK '				20	25	3	3	3.5	3
	SRCK ' to RCK '				40	19	5	5	8.5	5
	SRCLR , to RCK '				40	13	5	5	9	5
t _h				MIN	0	0	2	2	1.5	2
t _{PLH}		SRCK '	QH'	MAX	18	40	11.4	11.4	18.5	11.4
t _{PHL}					25	40	11.4	11.4	18.5	11.4
t _{PLH}		RCK '	QA to QH	MAX	18	37	10.5	10.5	17	10.5
t _{PHL}					35	37	10.5	10.5	17	10.5
t _{PHL}		SRCLR ,	QH'	MAX	35	44	11.1	11.1	17.2	11.1

UNIT: ns

8-BIT SHIFT REGISTER WITH OUTPUT LATCHES

- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Open-Collector Parallel Outputs
- Shift Register Has Direct Clear
- Accurate Shift Frequency: DC to 20MHz

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I _{CC}		MAX	55	mA
I _{OH}	Q _H '	MAX	16	mA
	Q	MAX	24	mA
I _{OL}	Q _H '	MAX	-1	mA
V _{OH}	Q _A to Q _H	MAX	5.5	V

SWITCHING CHARACTERISTICS

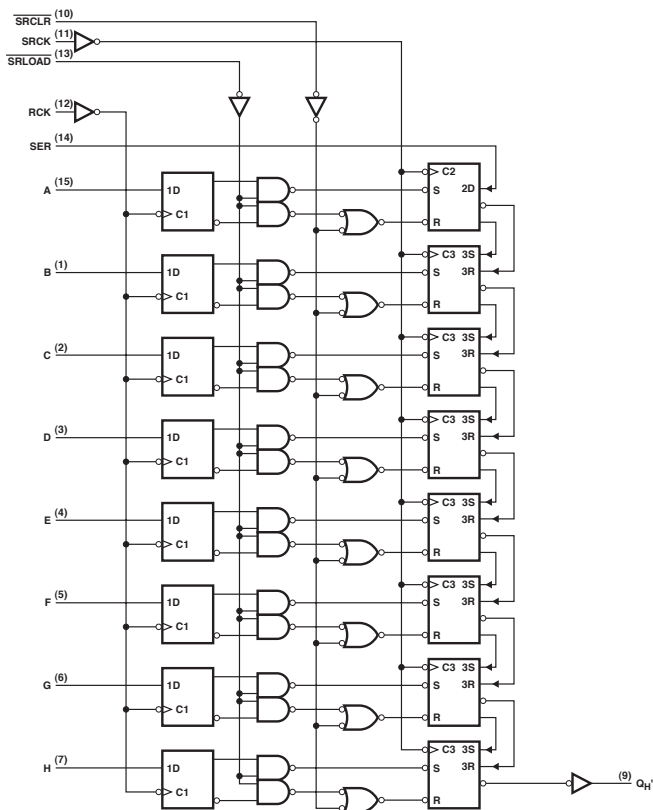
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
t _w	SRCK			MIN	25
	RCK				20
t _{su}	SRCLR ' to SRCK '			MIN	20
	SER to SRCK '				20
	SRCK ' to RCK '				40
	SRCLR , to RCK '				40
t _h				MIN	0
t _{PLH}		SRCK '	Q _H '	MAX	21
t _{PHL}					30
t _{PLH}		RCK '	Q _A to Q _H	MAX	42
t _{PHL}					35
t _{PHL}		SRCLR ,	Q _H '	MAX	35

UNIT: ns

8-BIT SHIFT REGISTER WITH INPUT LATCHES

- 8-Bit Parallel Storage Registers Inputs
- Shift Register Has Direct Overriding Load and Clear
- Accurate Shift Frequency: DC to 20MHz

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

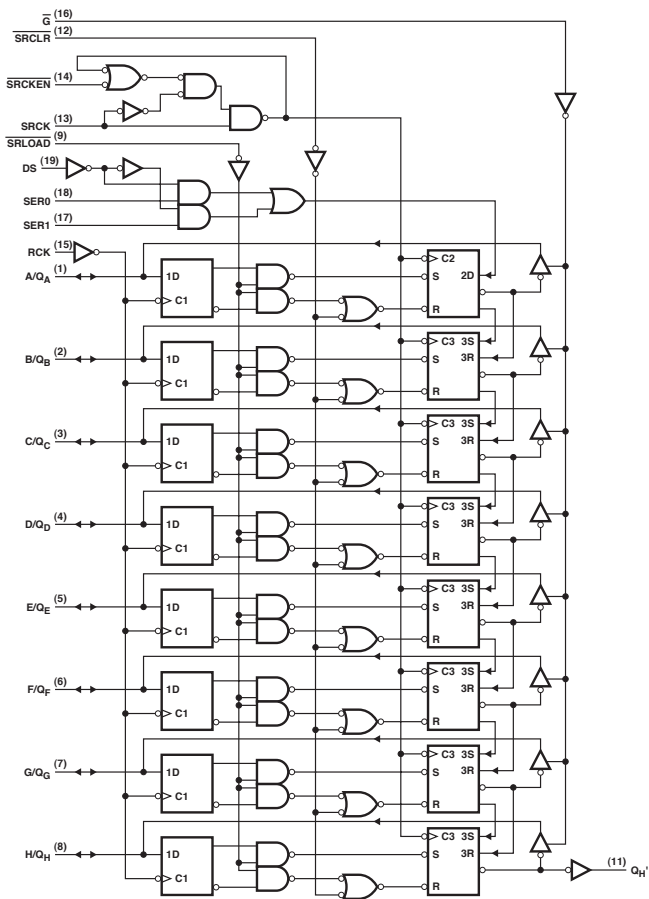
PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	53	0.16	0.16	mA
I _{OH}	MAX	-1	-4	-4	mA
I _{OL}	MAX	16	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT
f _{max}		SRCK			20	20	16
t _w	SRCK			MIN	35	24	30
	RCK			20	18	20	
	SRCLR			20	24	27	
	SRLOAD			40	21	24	
t _{su}	SRCLR ' to SRCK '			MIN	25	-	-
	SRLOAD ' to SRCK '			30	-	-	
	RCK ' to SRLOAD '			MIN	40	-	-
	SER to SRCK '			20	15	15	
	DATA to RCK '			MIN	20	15	15
				MIN	0	3	3
t _{PLH}	SRCK ' ,	QH'	MAX	23	53	57	
t _{PHL}				30	53	57	
t _{PLH}	SRLOAD ,	QH'	MAX	57	60	72	
t _{PHL}				44	60	72	
t _{PLH}	SRCLR ,	QH'	MAX	36	53	66	
t _{PHL}				60	72	84	
t _{PLH}	RCK ' ,	QH'	MAX	60	72	84	
t _{PHL}				48	72	84	

UNIT f_{max} : MHz, other : ns

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I _{CC}	MAX	85	mA
I _{DH}	MAX	-2.6	mA
I _{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

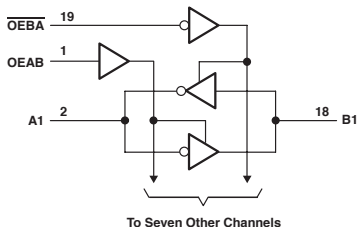
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
f _{max}	SRCK		MIN	20
t _{PLH}	SRCK ' 0	QH'	MAX	17
t _{PHL}				23
t _{PLH}	SRLOAD ,	QH'	MAX	42
t _{PHL}				30
t _{PHL}	SRCLR ,	QH'	MAX	27
t _{PLH}	RCK ' 0	QH'	MAX	48
t _{PHL}				36
t _{PLH}	SRCK ' 0	Q	MAX	18
t _{PHL}				28
t _{PLH}	SRLOAD ,	Q	MAX	48
t _{PHL}				40
t _{PHL}	SRCLR ,	Q	MAX	38
t _{PZH}	Ḡ ,	Q	MAX	31
t _{PZL}				43
t _{PHZ}	Ḡ ' 0	Q	MAX	38
t _{PLZ}				30

UNIT f_{max} : MHz, other : ns

OCTAL BUS TRANSCEIVERS

- Local Bus-Latch Capability
- 3-State Inverting Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

ENABLE INPUTS		OPERATION
OEBA	OEAB	
L	L	B data to Abus
H	H	A data to B bus
H	L	Isolation
L	H	B data to Abus A data to B bus

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 BCT	ABT	AC 11	ACT 11	UNIT
I _{CCZ}	MAX	95	47	77	0.08	10	0.25	0.08	0.008	mA
I _{CCL}	MAX	90	44	122	0.08	84	30	0.08	0.008	mA
I _{OH} (A port)	MAX	-15	-15	-15	-6	-3	-32	-24	-24	mA
I _{OH} (B port)	MAX	-15	-15	-15	-6	-15	-32	-24	-24	mA
I _{OL} (A port)	MAX	24	24	64	6	24	64	24	24	mA
I _{OL} (B port)	MAX	24	24	64	6	64	64	24	24	mA
I _{OL*}	MAX	-	48	-	-	-	-	-	-	mA

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SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 BCT	ABT	AC 11	ACT 11
t _{PLH}	A	B	MAX	10	10	7	26	5.8	4.8	7.4	9.4
				15	10	6	26	3.6	4.8	7.1	8.6
t _{PHL}	B	A	MAX	10	10	7	26	6.9	4.8	7.4	9.4
				15	10	6	26	3.9	4.8	7.1	8.6
t _{PZH}	OEBA	A	MAX	40	17	8	53	10.6	5.5	8.9	10.3
				40	25	9	53	11.1	7.1	8.5	10.1
t _{PHZ}	OEBA	A	MAX	25	12	6	38	10	7	8.1	10.4
				25	18	12	38	7.8	5.8	8.7	10.9
t _{PZH}	OEAB	B	MAX	40	18	8	53	7.4	6.8	8.8	11.3
				40	25	9	53	9	6.4	8.8	11
t _{PHZ}	OEAB	B	MAX	25	12	6	38	8.1	6.5	8.2	9.4
				25	18	13	38	5.9	5.6	8.6	9.6

UNIT: ns

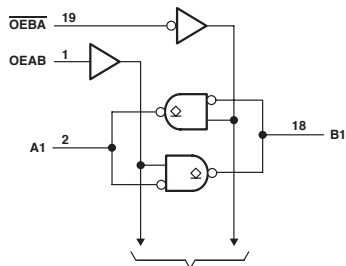
OCTAL BUS TRANSCEIVERS

- Local Bus-Latch Capability
- Open-Collector True Outputs
- Schmitt-Triggered Inputs (SN74LS621)

FUNCTION TABLE

ENABLE INPUTS		OPERATION
OEBA	OEAB	
L	L	B data to Abus
H	H	A data to B bus
H	L	Isolation
L	H	B data to Abus A data to B bus

Logic Diagram



To Seven Other Transceivers

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	ALS A-1	AS	UNIT
I_{CC}	MAX	90	48	48	189	mA
V_{OH}	MAX	5.5	5.5	5.5	5.5	V
I_{OL}	MAX	24	24	48	64	mA

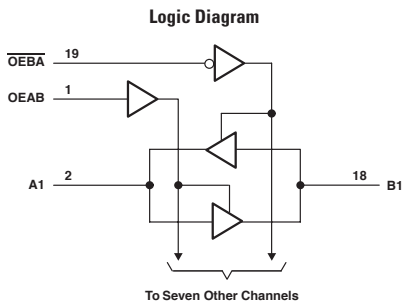
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	ALS A-1	AS
t_{PLH}	A	B	MAX	25	33	33	24
t_{PHL}				25	20	20	21
t_{PLH}	B	A	MAX	25	33	33	7.5
t_{PHL}				25	20	20	7.5
t_{PLH}	OEBA	A	MAX	40	39	39	21
t_{PHL}				50	35	35	9
t_{PLH}	OEAB	B	MAX	40	39	39	22
t_{PHL}				50	35	35	10

UNIT: ns

OCTAL BUS TRANSCEIVERS

- Local Bus-Latch Capability
- 3-State True Outputs
- Schmitt-Triggered Inputs (SN74LS623)
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)



FUNCTION TABLE

ENABLE INPUTS		OPERATION
OEBA	OEAB	
L	L	B data to Abus
H	H	A data to B bus
H	L	Isolation
L	H	B data to Abus A data to B bus

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	F	SN74 HC	SN74 HCT	SN74 BCT	ABT	AC 11	ACT 11	CD74 AC	CD74 ACT	UNIT
I _{CCZ}	MAX	95	55	116	130	0.08	0.08	11	0.25	0.08	0.04	0.16	0.16	mA
I _{CCL}	MAX	90	50	189	140	0.08	0.08	92	30	0.08	0.04	0.16	0.16	mA
I _{OH} (A port)	MAX	-15	-15	-15	-3	-6	-6	-3	-32	-24	-24	-24	-24	mA
I _{OH} (B port)	MAX	-15	-15	-15	-15	-6	-6	-15	-32	-24	-24	-24	-24	mA
I _{OL} (A port)	MAX	24	24	64	24	6	6	24	64	24	24	24	24	mA
I _{OL} (B port)	MAX	24	24	64	64	6	6	64	64	24	24	24	24	mA

SWITCHING CHARACTERISTICS

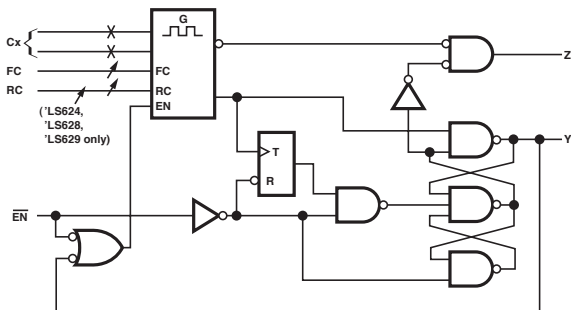
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	F	SN74 HC	SN74 HCT	SN74 BCT	ABT	AC 11	ACT 11	CD74 AC	CD74 ACT
t _{PLH}	A	B	MAX	15	13	9	6.5	26	28	5.2	4.6	7.8	8.5	9.6	10.6
				15	11	8	7.5	26	28	7.4	4.6	7.1	7.9	9.6	10.6
t _{PLH}	B	A	MAX	15	13	9	6.5	26	28	6.7	4.6	7.8	8.5	9.6	10.6
				15	11	8.5	7.5	26	28	8	4.6	7.1	7.9	9.6	10.6
t _{PZH}	OEBA	A	MAX	40	22	11	12	53	53	10.6	7.5	9	9.7	13.4	14.4
				40	22	10	10	53	53	10.7	7.5	9.1	10	13.4	14.4
t _{PHZ}	OEBA	A	MAX	25	16	7.5	7.5	38	38	9.8	7.5	8.3	10.9	13.4	14.4
				25	19	11.5	7	38	38	7.8	7.5	8.8	11.5	13.4	14.4
t _{PZH}	OEAB	B	MAX	40	22	11.5	11.5	53	53	7.6	7.5	9.2	10.7	13.4	14.4
				40	22	11	9.5	53	53	8.9	7.5	9.4	10.9	13.4	14.4
t _{PHZ}	OEAB	B	MAX	25	16	7	10	38	38	7.7	7.5	8.3	9.5	13.4	14.4
				25	19	9	10	38	38	7.1	7.5	8.8	10	13.4	14.4

UNIT: ns

VOLTAGE-CONTROLLED OSCILLATOR

- This Voltage Oscillators (VCOs) is Improved Versions of The Original VCO Family: SN74124, 324, 325, 326, 327
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Outputs Circuitry
- Highly Stable Operation over Specified Temperature and / or Supply Voltage Ranges

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	35	mA
I_{OL}	MAX	24	mA
I_{OH}	MAX	-1.2	mA

SWITCHING CHARACTERISTICS

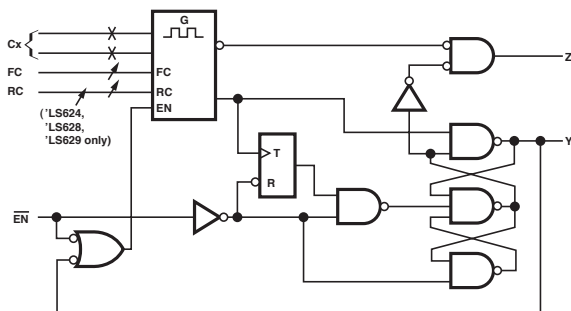
PARAMETER	MAX or MIN	LS
f_o	MAX	25

UNIT: MHz

VOLTAGE-CONTROLLED OSCILLATOR

- This Voltage Oscillators (VCOs) is Improved Versions of The Original VCO Family: SN74124, 324, 325, 326, 327
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Outputs Circuitry
- Highly Stable Operation over Specified Temperature and / or Supply Voltage Ranges
- Two Rexternal Pins Can Offer More Precise Temperature Compensation

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	35	mA
I_{OH}	MAX	-1.2	mA
I_{OL}	MAX	24	mA

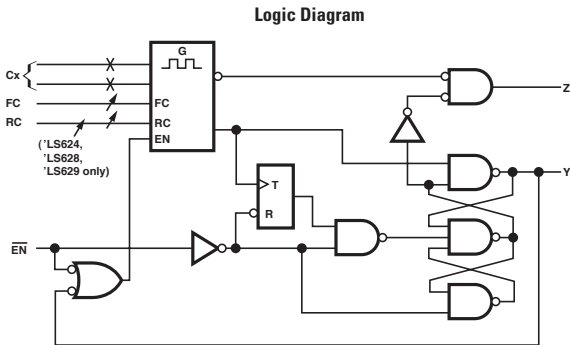
SWITCHING CHARACTERISTICS

PARAMETER	MAX or MIN	LS
f_o	MAX	25

UNIT: MHz

VOLTAGE-CONTROLLED OSCILLATOR

- This Voltage Oscillators (VCOs) is Improved Versions of The Original VCO Family: SN74124, 324, 325, 326, 327
- Separate Supply Voltage Pins for Isolation of Frequency Control Inputs and Oscillators from Outputs Circuitry
- Highly Stable Operation over Specified Temperature and / or Supply Voltage Ranges



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I_{CC}	MAX	55	mA
I_{OH}	MAX	-1.2	mA
I_{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

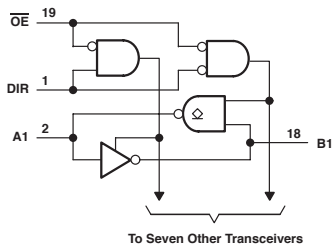
PARAMETER	MAX or MIN	LS
f_o	MAX	25

UNIT: MHz

OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Transceivers
- Inverting Logic
- Outputs A-Bus: Open-Collector 3-State
- Schmitt-Triggerred Inputs (SN74LS638)

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	UNIT
I _{CCZ}	MAX	95	30	61	mA
I _{CCD}	MAX	90	41	122	mA
I _{OH} (B)	MAX	-15	-15	-15	mA
V _{OH} (A)	MAX	5.5	5.5	5.5	V
I _{OL}	MAX	24	24	64	mA
I _{OL*}	MAX	-	48	-	mA

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SWITCHING CHARACTERISTICS

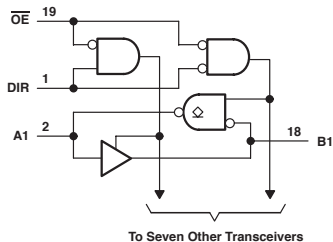
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS
t _{PLH}	A	B	MAX	10	12	7
t _{PHL}				15	12	6.5
t _{PLH}	B	A	MAX	25	25	20
t _{PHL}				25	30	7
t _{PLH}	$\overline{\text{OE}}$	A	MAX	40	25	19
t _{PHL}				60	45	9
t _{PLZ}	$\overline{\text{OE}}$	B	MAX	40	20	8
t _{PZL}				40	22	10
t _{PHZ}	$\overline{\text{OE}}$	B	MAX	25	10	7
t _{PLZ}				25	15	10

UNIT: ns

OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Transceivers
- True Logic
- Outputs A-Bus: Open-Collector 3-State
- Schmitt-Triggerred Inputs (SN74LS638)

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	UNIT
I _{CCZ}	MAX	95	54	100	mA
I _{CCL}	MAX	90	50	154	mA
I _{DH} (B)	MAX	-15	-15	-15	mA
V _{OH} (A)	MAX	5.5	5.5	5.5	V
I _{OL}	MAX	24	24	64	mA
I _{OL*}	MAX	-	48	-	mA

*639-1

SWITCHING CHARACTERISTICS

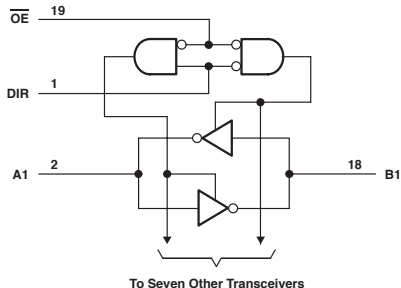
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS
t _{PLH}	A	B	MAX	15	12	9.5
t _{PHL}				15	12	9
t _{PLH}	B	A	MAX	25	30	22
t _{PHL}				25	22	9
t _{PLH}	OE	A	MAX	40	30	21.5
t _{PHL}				50	35	11.5
t _{PSH}	OE	B	MAX	40	21	10.5
t _{PZL}				40	25	10.5
t _{PHZ}	OE	B	MAX	25	10	7
t _{PLZ}				25	16	10.5

UNIT: ns

OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Transceivers
- Inverting Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS640, 640-1)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION
OE	DIR	
L	L	\bar{B} data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	ACT 11	UNIT
I _{CCZ}	MAX	95	50	80	0.08	0.16	0.08	0.16	11	0.25	0.08	mA
I _{CCL}	MAX	90	55	123	0.08	0.16	0.08	0.16	94	30	0.08	mA
I _{OH} (A port)	MAX	-15	-15	-15	-6	-6	-6	-6	-3	-32	-24	mA
I _{OH} (B port)	MAX	-15	-15	-15	-6	-6	-6	-6	-15	-32	-24	mA
I _{OL} (A port)	MAX	24	24	64	6	6	6	6	24	64	24	mA
I _{OL} (B port)	MAX	24	24	64	6	6	6	6	64	64	24	mA
I _{OL*}	MAX	48	48	-	-	-	-	-	-	-	-	mA

*640-1

SWITCHING CHARACTERISTICS

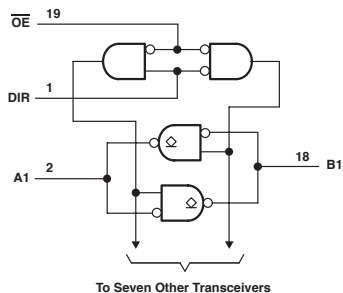
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	ACT 11
t _{PLH}	A	B	MAX	10	11	7	26	27	28	33	6.5	4.9	10.5
t _{PHL}				15	10	6	26	27	28	33	3.7	4.9	9.5
t _{PLH}	B	A	MAX	10	11	7	26	27	28	33	6.5	4.9	10.5
t _{PHL}				15	10	6	26	27	28	33	3.7	4.9	9.5
t _{PZL}	\overline{OE}	A	MAX	40	21	8	58	45	58	45	10.2	5.8	13.4
t _{PZL}				40	24	10	58	45	58	45	10.7	7.3	13.6
t _{PHZ}	\overline{OE}	A	MAX	25	10	8	38	45	50	45	10.2	6.8	13.9
t _{PLZ}				25	15	13	38	45	50	45	7.8	5.5	14.2
t _{PZH}	\overline{OE}	B	MAX	40	21	8	58	45	58	45	10.2	5.8	13.4
t _{PZL}				40	24	10	58	45	58	45	10.7	7.3	13.6
t _{PHZ}	\overline{OE}	B	MAX	25	10	8	38	45	50	45	10.2	6.8	13.9
t _{PLZ}				25	15	13	38	45	50	45	7.8	5.5	14.2

UNIT: ns

OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Transceivers
- True Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS641)

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION
\overline{G}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	UNIT
I_{CCZ}	MAX	95	-	-	mA
I_{CCL}	MAX	90	47	136	mA
V_{OH}	MAX	5.5	5.5	5.5	V
I_{OL}	MAX	24	24	64	mA
I_{OL}^*	MAX	48	48	-	mA

*641-1

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS
t_{PLH}	A	B	MAX	25	25	21
t_{PHL}				25	18	7.5
t_{PLH}	B	A	MAX	25	25	21
t_{PHL}				25	18	7.5
t_{PLH}	\overline{OE}	A, B	MAX	40	30	21
t_{PHL}				50	30	9
t_{PLH}	DIR	A, B	MAX	40	32	22
t_{PHL}				50	32	10

UNIT: ns

OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Transceivers
- Inverting Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS642)

FUNCTION TABLE

CONTROL INPUTS		OPERATION
OE	DIR	
L	L	\overline{B} data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	UNIT
I_{CCZ}	MAX	95	-	-	mA
I_{CCL}	MAX	90	28	104	mA
V_{OH}	MAX	5.5	5.5	5.5	V
I_{OL}	MAX	24	24	64	mA
I_{OL}^*	MAX	48	48	-	mA

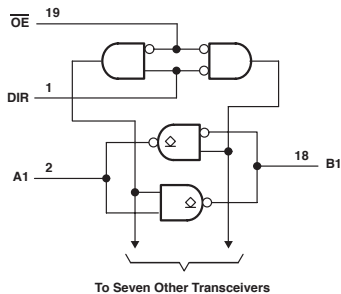
*642-1

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS
t_{PLH}	A	B	MAX	25	30	24
t_{PHL}				25	22	7.5
t_{PLH}	B	A	MAX	25	30	24
t_{PHL}				25	22	7.5
t_{PLH}	\overline{OE}, DIR	A	MAX	40	30	23.5
t_{PHL}				60	38	11.5
t_{PLH}	\overline{OE}, DIR	B	MAX	40	30	23.5
t_{PHL}				60	38	11.5

UNIT: ns

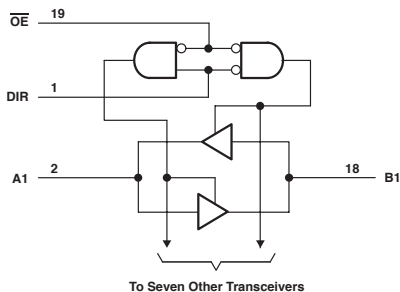
Logic Diagram



OCTAL BUS TRANSCEIVERS

- Bidirectional Bus Transceivers
- True Logic
- 3-State Outputs
- Schmitt-Triggered Inputs (SN74LS645, 645-1)

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT	UNIT
ICCZ	MAX	95	58	123	0.08	0.08	mA
ICCL	MAX	90	55	149	0.08	0.08	mA
IDH	MAX	-15	-15	-15	-6	-6	mA
IOL	MAX	24	24	64	6	6	mA
IOL*	MAX	48	48	-	-	-	mA

*645-1

SWITCHING CHARACTERISTICS

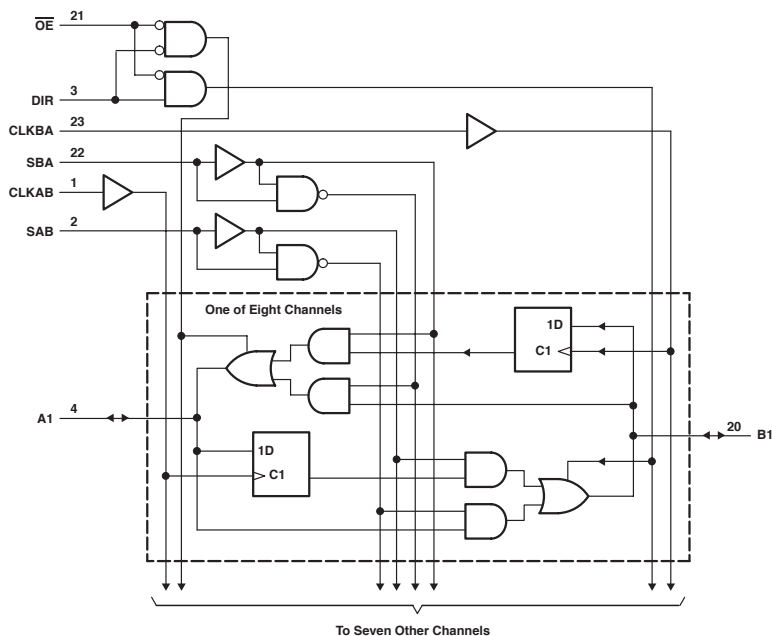
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT
tPLH	A	B	MAX	15	10	9.5	26	28
				15	10	9	26	28
tPHL	B	A	MAX	15	10	9.5	26	28
				15	10	9	26	28
tPZH	OE	A	MAX	40	20	11	58	58
				40	20	10	58	58
tPZH	OE	A	MAX	25	10	7	50	50
				25	15	12	50	50
tPZH	OE	B	MAX	40	20	11	58	58
				40	20	10	58	58
tPHZ	OE	B	MAX	25	10	7	50	50
				25	15	12	50	50

UNIT: ns

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bidirectional Bus Transceivers
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- 3-State Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	ABT Ver.A	LVTH 3V	UNIT
I_{CC}	MAX	165	88	211	0.08	0.16	0.08	0.08	67	30	30	5	mA
I_{OH}	MAX	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	-32	mA
I_{OL}	MAX	24	24	48	6	6	6	6	64	64	64	64	mA
I_{OL}^*	MAX	-	48	-	-	-	-	-	-	-	-	-	mA

PARAMETER	MAX or MIN	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V	UNIT
I_{CC}	MAX	0.08	0.08	0.08	0.08	0.01	mA
I_{OH}	MAX	-24	-24	-24	-24	-24	mA
I_{OL}	MAX	24	24	24	24	24	mA
I_{OL}^*	MAX	-	-	-	-	-	mA

*646-1

FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION			
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8				
H	X	H to L	H to L	X	X	Input	Input	Isolation Store A and B data			
H	X	↑	↑	X	X	Input	Input				
L	L	X	X	X	L	Output	Input	Real-time B data to A bus Stored B data to A bus			
L	L	X	H to L	X	H	Output	Input				
L	H	X	X	L	X	Input	Output	Real-time A data to B bus Stored A data to B bus			
L	H	H to L	X	H	X	Input	Output				

† The data output functions can be enabled or disabled by various signals at OE and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT
t _{max}			MIN	-	40	90	27	25	27	20	83
t _w	CLKBA,CLKAB "H"		MIN	15	12.5	5	19	20	19	31	6
	CLKBA,CLKAB "L"			30	12.5	6	19	20	19	31	6
	DATA			30	-	-	-	-	-	-	-
t _{su}	CLKBA,CLKAB "H"		MIN	15	10	6	25	15	25	15	6
	CLKBA,CLKAB "L"			15	10	6	25	15	25	15	6
t _h	CLKBA,CLKAB		MIN	0	0	0	5	9	5	5	0.5
t _{PLH}	CLOCK	A, B	MAX	25	30	8.5	45	55	45	55	11.2
t _{PHL}				35	17	9	45	55	45	55	10.6
t _{PLH}	A, B	B, A	MAX	18	20	9	34	34	34	46	9.5
t _{PHL}				20	12	7	34	34	34	46	10.5
t _{PLH}	SAB, SBA (sored data high)	A, B	MAX	40	25	11	48	43	48	58	13.8
t _{PHL}				35	20	9	48	43	48	58	9.1
t _{PLH}	SAB, SBA (sored data low)	A, B	MAX	50	35	11	48	43	48	58	12
t _{PHL}				25	20	9	48	43	48	58	12.9
t _{PZH}	OE	A, B	MAX	55	17	9	61	44	61	56	13.2
t _{PZL}				65	20	14	61	44	61	56	14.4
t _{PHZ}	OE	A, B	MAX	35	10	9	61	44	61	44	10.9
t _{PLZ}				35	16	9	61	44	61	44	10.5
t _{PZH}	DIR	A, B	MAX	45	30	16	61	44	61	56	13.1
t _{PZL}				60	25	18	61	44	61	56	14.6
t _{PHZ}	DIR	A, B	MAX	30	10	10	61	44	61	44	12.6
t _{PLZ}				30	16	10	61	44	61	44	11.8

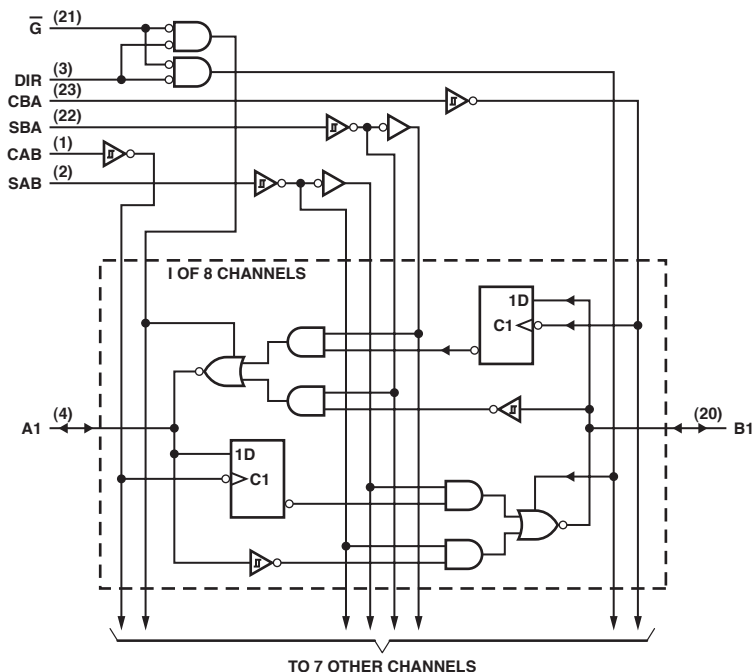
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABT A Ver.	LVTH 3V	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V
t _{max}			MIN	125	125	150	100	125	105	110	150
t _w	CLKBA,CLKAB "H"		MIN	4	4	3.3	5	4	4.8	4.5	3.3
	CLKBA,CLKAB "L"			4	4	3.3	5	4	4.8	4.5	3.3
	DATA			-	-	-	-	-	-	-	-
t _{su}	CLKBA,CLKAB "H"		MIN	3.5	3	1.2	4.5	2.5	4.5	2.5	1.5
	CLKBA,CLKAB "L"			3	3	1.6	4.5	2.5	4.5	2.5	1.5
t _h	CLKBA,CLKAB		MIN	0	0	0.8	1	2	2.5	2	1.7
t _{PLH}	CLOCK	A, B	MAX	7.8	5.6	4.7	11	13.5	13.5	15.5	8.4
t _{PHL}				8.4	5.6	4.7	12.2	13.5	14.9	15.5	8.4
t _{PLH}	A, B	B, A	MAX	6.9	4.8	3.5	8.8	11	11.5	12.5	7.4
t _{PHL}				6.9	5.4	3.5	9.8	11	12	12.5	7.4
t _{PLH}	SAB, SBA (sored data high)	A, B	MAX	7.1	6.5	4.9	9.4	12	11.5	14.5	8.6
t _{PHL}				7.9	5.9	4.9	10.7	12	13.5	14.5	8.6
t _{PLH}	SAB, SBA (sored data low)	A, B	MAX	7.1	6.5	4.9	9.9	12	12.4	14.5	8.6
t _{PHL}				7.9	5.9	4.9	11	12	13.1	14.5	8.6
t _{PZH}	OE	A, B	MAX	6.3	6.3	5.2	12	13.5	14.4	15.5	8.2
t _{PZL}				8.8	8.8	5.2	13.1	13.5	15.3	15.5	8.2
t _{PHZ}	OE	A, B	MAX	8.3	5	5.5	8.9	13.5	11.6	15.5	7.5
t _{PLZ}				7.5	4.5	5.5	8.3	13.5	10.6	15.5	7.5
t _{PZH}	DIR	A, B	MAX	6.7	6.7	5.2	12.6	13.5	15.3	15.5	8.3
t _{PZL}				9.5	9.5	5.2	13.7	13.5	16.5	15.5	8.3
t _{PHZ}	DIR	A, B	MAX	7.7	5.7	5.6	8.7	13.5	11.3	15.5	7.9
t _{PLZ}				8.2	6	5.6	8.1	13.5	10.3	15.5	7.9

UNIT f_{max} : MHz other : ns

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bidirectional Bus Transceivers
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- Open-Collector Outputs

Logic Diagram



FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
\bar{G}	DIR	CAB	CBA	SAB	SBA	A1–A8	B1–B8	
H	X	H to L	H to L	X	X	Input	Input	Isolation Store A and B data
H	X	†	†	X	X	Input	Input	
L	L	X	X	X	L	Output	Input	Real-time B data to A bus Stored B data to A bus
L	L	X	H to L	X	H	Output	Output	
L	H	X	X	L	X	Input	Output	Real-time A data to B bus Stored A data to B bus
L	H	H to L	X	H	X	Input	Output	

† The data output functions can be enabled or disabled by various signals at OE and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I _{CC}	MAX	150	mA
V _{GH}	MAX	5.5	V
I _{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

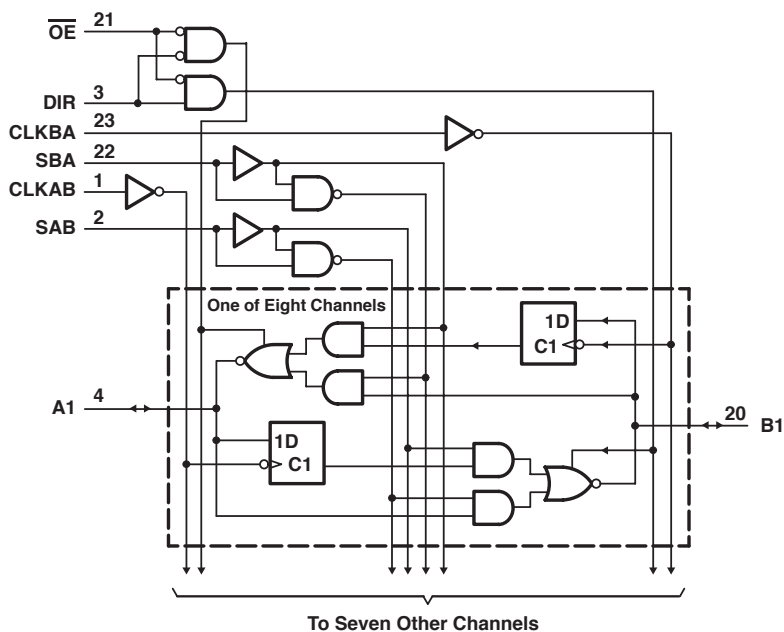
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t _w			MIN	30
t _{su}		A, B	MIN	15
t _h		A, B	MIN	0
t _{PLH}	CLOCK	A, B	MAX	35
t _{PHL}				45
t _{PLH}	A, B	B, A	MAX	26
t _{PHL}				27
t _{PLH}	SAB, SBA (With Bus Input High)	A, B	MAX	50
t _{PHL}				45
t _{PLH}	SAB, SBA (With Bus Input Low)	A, B	MAX	60
t _{PHL}				30
t _{PLH}	\bar{G}	A, B	MAX	40
t _{PHL}				50
t _{PLH}	DIR	A, B	MAX	35
t _{PHL}				40

UNIT: ns

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bidirectional Bus Transceivers
- Independent Registers for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- 3-State Outputs

Logic Diagram



FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
H	X	H to L	H to L	X	X	Input	Input	Isolation Store A and B data
H	X	†	†	X	X	Input	Input	
L	L	X	X	X	L	Output	Input	Real-time B data to A bus Stored B data to A bus
L	L	X	H to L	X	H	Output	Input	
L	H	X	X	L	X	Input	Output	Real-time A data to B bus Stored A data to B bus
L	H	H to L	X	H	X	Input	Output	

† The data output functions can be enabled or disabled by various signals at OE and DIR. Data input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT	UNIT
I _{CC}	MAX	180	88	195	0.08	0.08	mA
I _{OH}	MAX	-15	-15	-15	-6	-6	mA
I _{OL}	MAX	24	24	48	6	6	mA

SWITCHING CHARACTERISTICS

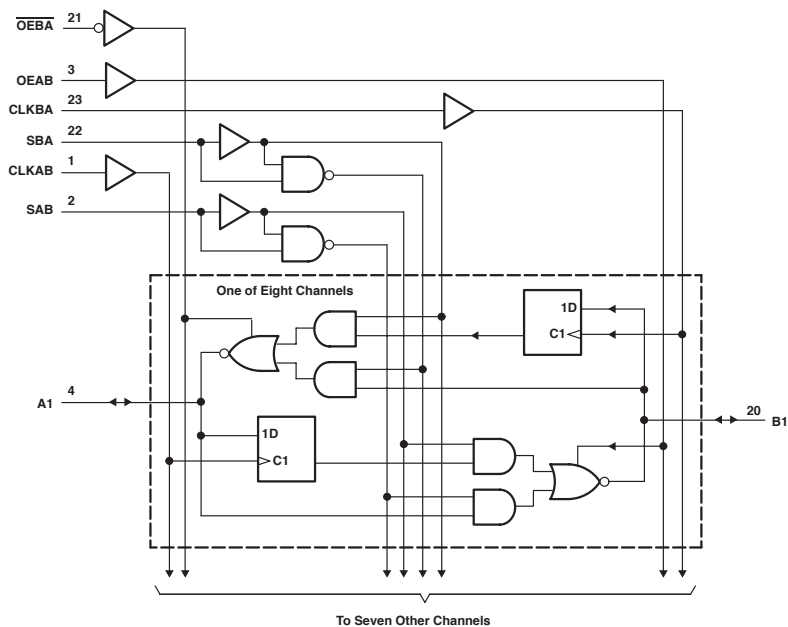
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT
f _{max}			MIN	-	40	90	27	27
t _w	CLKAB, CLKBA "H"		MIN	15	12.5	5	19	19
	CLKAB, CLKBA "L"		MIN	30	12.5	6	19	19
	DATA		MIN	30	-	-	-	-
t _{su}	CLKAB, CLKBA		MIN	15	10	6	25	25
t _h	CLKAB, CLKBA		MIN	0	0	0	5	5
t _{PLH}	CLOCK	A, B	MAX	25	33	8.5	45	45
t _{PHL}				40	20	9	45	45
t _{PLH}	A, B	B, A	MAX	18	17	8	34	34
t _{PHL}				25	10	7	34	34
t _{PLH}	SAB, SBA (With Bus Input High)	A, B	MAX	55	25	11	48	48
t _{PHL}				40	21	9	48	48
t _{PLH}	SAB, SBA (With Bus Input Low)	A, B	MAX	40	39	11	48	48
t _{PHL}				40	22	9	48	48
t _{PZH}	OE	A, B	MAX	50	22	9	61	61
t _{PZL}				55	22	15	61	61
t _{PHZ}	OE	A, B	MAX	45	10	9	61	61
t _{PLZ}				35	15	9	61	61
t _{PZH}	DIR	A, B	MAX	40	27	16	61	61
t _{PZL}				45	19	18	61	61
t _{PHZ}	DIR	A, B	MAX	35	14	10	61	61
t _{PLZ}				30	15	10	61	61

UNIT f_{max} : MHz other : ns

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bus Trceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- 3-State Outputs

Logic Diagram



FUNCTION TABLE

INPUTS						DATA I/O				OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8			
L	H	H to L	H to L	X	X	Input	Input			Isolation Store A and B data
L	H	↑	↑	X	X	Input	Input			
X	H	↑	H to L	X	X	Input	Unspecified			Store A, hold B Store A in both registers
H	H	↑	↑	X	X	Input	Output			
L	X	H to L	↑	X	X	Unspecified	Input			Hold A, store B Store B in both registers
L	L	↑	↑	X	X	Output	Input			
L	L	X	X	X	L	Output	Input			Real-time \bar{B} data to A bus Stored \bar{B} data to A bus
L	L	X	H to L	X	H	Output	Input			
H	H	X	X	L	X	Input	Output			Real-time \bar{A} data to B bus Stored \bar{A} data to B bus
H	H	H to L	X	H	X	Input	Output			
H	L	H to L	H to L	H	H	Output	Output			Stored \bar{A} data to B bus and stored \bar{B} data to A bus

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT	SN74 BCT	ABT	CD74 ACT	UNIT
I _{CC}	MAX	165	82	195	0.08	0.08	62	30	160	mA
I _{OH}	MAX	-15	-15	-15	-6	-6	-15	-32	-24	mA
I _{OL}	MAX	24	24	48	6	6	64	64	24	mA
I _{OL*}	MAX	-	48	-	-	-	-	-	-	mA

*651-1

SWITCHING CHARACTERISTICS

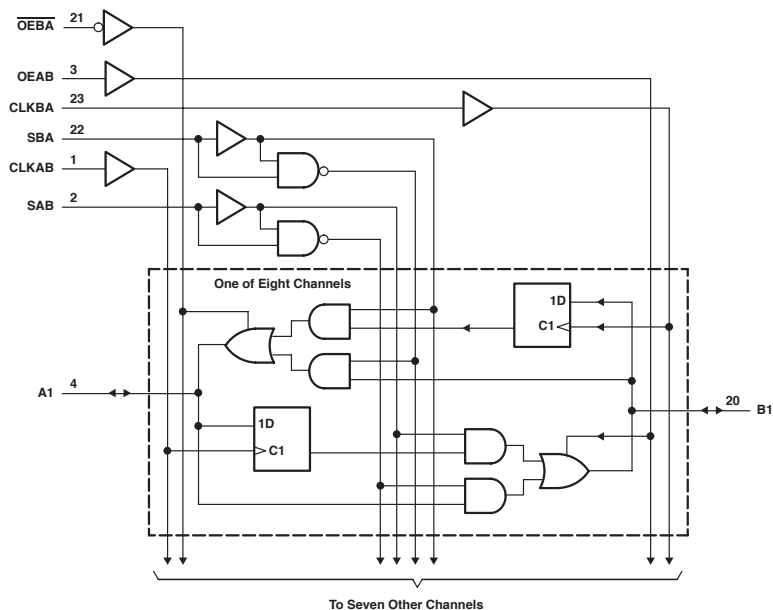
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	SN74 HCT	SN74 BCT	ABT	CD74 ACT
t _{max}			MIN	-	40	90	27	20	85	125	110
t _w	CLKBA, CLKAB "H"		MIN	15	12.5	5	19	25	4.8	4	4.5
	CLKBA, CLKAB "L"		MIN	15	12.5	6	19	25	7	4	4.5
t _{su}	DATA		MIN	15	-	-	-	-	-	-	-
	A,B		MIN	15	10	6	25	19	6	3	2.5
t _h	A,B		MIN	0	0	0	5	5	1	0	2
t _{PLH}	CLOCK	A,B	MAX	24	32	8.5	45	45	11.7	5.6	15.5
t _{PHL}				35	17	9	45	45	11.8	5.6	15.5
t _{PLH}	A,B	B,A	MAX	18	18	9	34	34	12.6	6.2	12.5
t _{PHL}				30	10	7	34	34	9.8	5.4	12.5
t _{PLH}	SAB,SBA (With Bus Input High)	A,B	MAX	47	38	11	48	48	9.8	6.5	15.5
t _{PHL}				33	21	9	48	48	15.5	5.9	15.5
t _{PLH}	SAB,SBA (With Bus Input Low)	A,B	MAX	35	25	11	48	48	14.6	6.5	15.5
t _{PHL}				30	21	9	48	48	12.8	5.9	15.5
t _{PZH}	OEBA	A	MAX	44	20	10	61	61	12	5.8	15.5
t _{PZL}				60	18	16	61	61	13.1	8.5	15.5
t _{PHZ}	OEBA	A	MAX	38	9	9	61	61	10.2	5	15.5
t _{PLZ}				30	12	9	61	61	9.6	4.1	15.5
t _{PZH}	OEAB	B	MAX	29	22	11	61	61	8.3	6.5	15.5
t _{PZL}				40	21	16	61	61	9.7	7.4	15.5
t _{PHZ}	OEAB	B	MAX	38	12	10	61	61	15	5.5	15.5
t _{PLZ}				30	14	11	61	61	12.3	5.1	15.5

UNIT f_{max} : MHz other : ns

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bus Transceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- 3-State Outputs
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	
L	H	H to L	H to L	X	X	Input	Input	Isolation Store A and B data
L	H	↑	↑	X	X	Input	Input	
X	H	↑	H to L	X	X	Input	Unspecified	Store A, hold B Store A in both registers
H	H	↑	↑	X	X	Input	Output	
L	X	H to L	↑	X	X	Unspecified	Input	Hold A, store B Store B in both registers
L	L	↑	↑	X	X	Output	Input	
L	L	X	X	X	L	Output	Input	Real-time \bar{B} data to A bus
L	L	X	H to L	X	H	Output	Input	Stored \bar{B} data to A bus
H	H	X	X	L	X	Input	Output	Real-time \bar{A} data to B bus
H	H	H to L	X	H	X	Input	Output	Stored \bar{A} data to B bus
H	L	H to L	H to L	H	H	Output	Output	Stored \bar{A} data to B bus and stored \bar{B} data to A bus

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT	ABT	ABT Ver.A	UNIT
I _{CC}	MAX	180	88	211	0.08	0.16	0.08	0.16	69	30	30	mA
I _{OH}	MAX	-15	-15	-15	-6	-6	-6	-6	-15	-32	-32	mA
I _{OL}	MAX	24	24	48	6	6	6	6	64	64	64	mA

PARAMETER	MAX or MIN	LVTH 3V	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V	UNIT
I _{CC}	MAX	5	0.08	0.16	0.08	0.16	0.01	mA
I _{OH}	MAX	-32	-24	-24	-24	-24	-24	mA
I _{OL}	MAX	64	24	24	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	AS	SN74 HC	CD74 HC	SN74 HCT	CD74 HCT	SN74 BCT
t _{max}			MIN	-	40	90	27	20	20	17	77
t _w	CLKBA, CLKAB "H"		MIN	15	12.5	5	19	24	25	38	6.5
	CLKBA, CLKAB "L"		MIN	15	12.5	6	19	24	25	38	6.5
	DATA		MIN	15	-	-	-	-	-	-	-
t _{su}	A,B High		MIN	15	10	6	25	18	19	18	5
t _{su}	A,B Low		MIN	15	10	6	25	18	19	18	5
t _h	A,B		MIN	0	0	0	5	11	5	5	1
t _{PLH}	CLOCK	A,B	MAX	25	30	8.5	45	66	45	66	10.5
t _{PHL}				36	17	9	45	66	45	66	9.9
t _{PLH}	A,B	B,A	MAX	18	18	9	34	41	34	56	8.9
t _{PHL}				20	12	7	34	41	34	56	9.8
t _{PLH}	SAB,SBA (With Bus Input High)	A,B	MAX	35	35	11	48	51	48	69	13.1
t _{PHL}				32	20	9	48	51	48	69	8.5
t _{PLH}	SAB,SBA (With Bus Input Low)	A,B	MAX	50	25	11	48	51	48	69	11.3
t _{PHL}				23	20	9	48	51	48	69	12.5
t _{PHZ}	OEBA	A	MAX	45	17	10	61	53	61	68	10.6
t _{PZL}				54	18	16	61	53	61	68	12
t _{PHZ}	OEBA	A	MAX	38	10	9	61	53	61	53	10
t _{PLZ}				30	16	9	61	53	61	53	9.5
t _{PHZ}	OEAB	B	MAX	30	22	11	61	53	61	68	8.1
t _{PZL}				38	18	16	61	53	61	68	9.3
t _{PHZ}	OEAB	B	MAX	38	10	10	61	53	61	53	11.6
t _{PLZ}				30	16	11	61	53	61	53	11.3

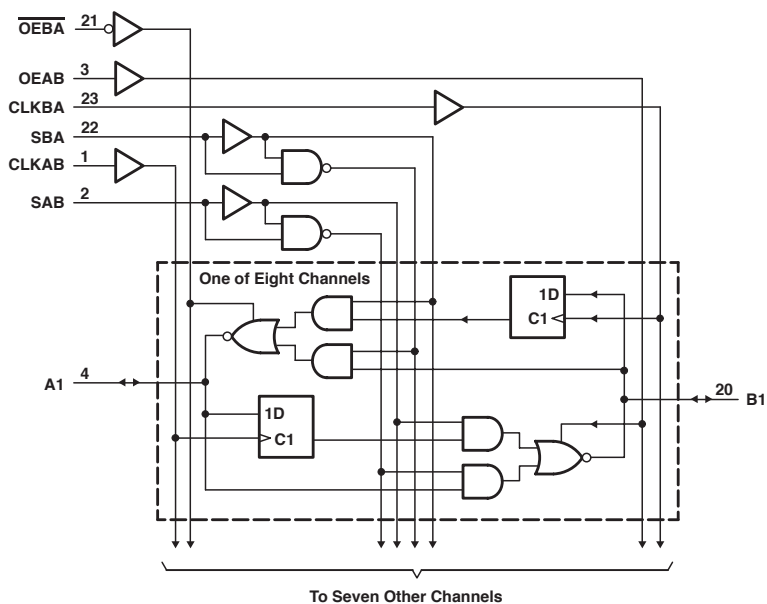
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABT Ver.A	LVTH 3V	AC 11	CD74 AC	ACT 11	CD74 ACT	LVC 3V
t _{max}			MIN	125	125	150	105	125	105	110	100
t _w	CLKBA, CLKAB "H"		MIN	4	4	3.3	4.8	4	4.8	4.5	3.3
	CLKBA, CLKAB "L"		MIN	4	4	3.3	4.8	4	4.8	4.5	3.3
	DATA		MIN	-	-	-	-	-	-	-	-
t _{su}	A,B High		MIN	3.5	3	1.2	4.5	2.5	4	2.5	1.9
t _{su}	A,B Low		MIN	3.5	3	1.6	4.5	2.5	4	2.5	1.9
t _h	A,B		MIN	0	0	0.8	1	2	2.5	2	1.7
t _{PLH}	CLOCK	A,B	MAX	7.8	5.6	4.7	10.7	13.5	13.1	15.5	8
t _{PHL}				8.4	5.6	4.7	12	13.5	14.4	15.5	8
t _{PLH}	A,B	B,A	MAX	6.7	4.8	3.5	8.6	11	11.1	12.5	7.4
t _{PHL}				6.7	5.4	3.5	9.6	11	11.6	12.5	7.4
t _{PLH}	SAB,SBA (With Bus Input High)	A,B	MAX	6.9	6.5	4.9	9.1	12	11	14.5	8.7
t _{PHL}				7.7	5.9	4.9	10.7	12	13.3	14.5	8.7
t _{PLH}	SAB,SBA (With Bus Input Low)	A,B	MAX	6.9	6.5	4.9	9.9	12	12.2	14.5	8.7
t _{PHL}				7.7	5.9	4.9	10.9	12	12.6	14.5	8.7
t _{PHZ}	OEBA	A	MAX	5.8	5.8	5.2	10.9	13.5	12.6	15.5	7.4
t _{PZL}				8.5	8.5	5.2	12.2	13.5	13.8	15.5	7.4
t _{PHZ}	OEBA	A	MAX	8.2	5	5.5	7.6	13.5	9.9	15.5	7.5
t _{PLZ}				6.8	4.1	5.5	7.1	13.5	9.3	15.5	7.5
t _{PHZ}	OEAB	B	MAX	6.5	6.5	4.7	11.3	13.5	15.2	15.5	7.1
t _{PZL}				7.4	7.4	4.7	12.3	13.5	16.1	15.5	7.1
t _{PHZ}	OEAB	B	MAX	6.9	5.5	5.6	7.6	13.5	10.3	15.5	7.4
t _{PLZ}				6.2	5.1	5.6	7.2	13.5	9.3	15.5	7.4

UNIT f_{max} : MHz other : ns

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bus Trceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- Inverting Data Paths
- Outputs
 - A Bus: Open-Collector
 - B Bus: 3-State

Logic Diagram



FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1–A8	B1–B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation Store A and B data
X	H	↑	H or L	X	X	Input	Unspecified‡	Store A, hold B Store A in both registers
H	H	↑	↑	X†	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified‡	Input	Hold A, store B Store B in both registers
L	L	↑	↑	X	X†	Output	Input	Store B data to A bus
L	L	X	X	X	L	Output	Input	Real-time \bar{B} data to A bus Stored B data to A bus
L	L	X	H or L	X	H	Output	Input	Real-time \bar{B} data to A bus Stored B data to A bus
H	H	X	X	L	X	Input	Output	Real-time \bar{A} data to B bus Stored \bar{A} data to B bus
H	H	H or L	X	H	X	Input	Output	Real-time \bar{A} data to B bus Stored \bar{A} data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored \bar{A} data to B bus and stored \bar{B} data to A bus

NOTES:

† The data output functions can be enabled or disabled by a variety of level combinations at GAB or GB̄A. Data input functions always are enabled; i.e., data at the bus terminals is stored on every low-to-high transition on the clock inputs.

‡ Select control = L: clocks can occur simultaneously.

† Select control = H: clock must be staggered to load both registers.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	UNIT
I _{CC}	MAX	165	88	mA
I _{OH}	MAX	-15	-15	mA
I _{OL}	MAX	24	24	mA

SWITCHING CHARACTERISTICS

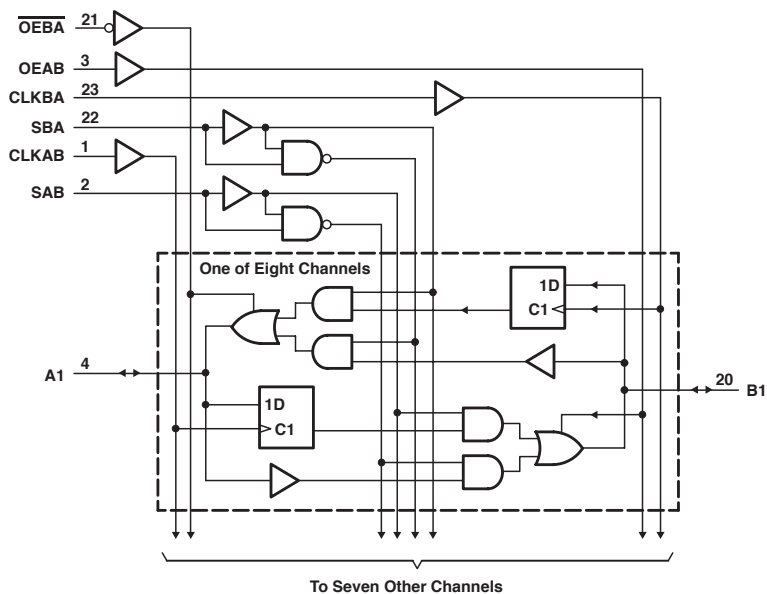
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS
t _w	CLK "H"		MIN	15	14.5
	CLK "L"		MIN	30	14.5
	DATA		MIN	30	-
t _{su}	A, B		MIN	15	10
	A, B		MIN	0	0
t _{PLH}	CLKBA	A	MAX	38	64
t _{PHL}				39	22
t _{PLH}	CLKAB	B	MAX	23	30
t _{PHL}				36	17
t _{PLH}	A	B	MAX	18	18
t _{PHL}				30	15
t _{PLH}	B	A	MAX	32	56
t _{PHL}				24	15
t _{PLH}	SBA (B "H")	A	MAX	57	62
t _{PHL}				39	25
t _{PLH}	SBA (B "L")	A	MAX	51	62
t _{PHL}				35	25
t _{PLH}	SAB (A "H")	B	MAX	48	35
t _{PHL}				33	22
t _{PLH}	SAB (A "L")	B	MAX	36	25
t _{PHL}				30	22
t _{PLH}	OEBA	A	MAX	35	30
t _{PHL}				55	24
t _{PZH}	OEAB	B	MAX	29	22
t _{PZL}				38	22
t _{PHZ}	OEAB	B	MAX	39	14
t _{PLZ}				29	16

UNIT:ns

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Bus Trceivers / Registers
- Independent Registers and Enables for A and B Buses
- Multiplexed Real-Time and Stored Data
- True Data Paths
- Outputs
 - A Bus: Open-Collector
 - B Bus: 3-State

Logic Diagram



FUNCTION TABLE

		INPUTS				DATA I/O				OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8			
L	H	H to L	H to L	X	X	Input	Input	Isolation Store A and B data		
L	H	↑	↑	X	X	Input	Input			
X	H	↑	H to L	X	X	Input	Unspecified	Store A, hold B Store A in both registers		
H	H	↑	↑	X	X	Input	Output			
L	X	H to L	↑	X	X	Unspecified Output	Input	Hold A, store B Store B in both registers		
L	L	↑	↑	X	X		Input		Input	
L	L	X	X	X	L	Output	Input	Real-time \overline{B} data to A bus Stored \overline{B} data to A bus		
L	L	X	H to L	X	H	Output	Input			
H	H	X	X	L	X	Input	Output	Real-time \overline{A} data to B bus Stored \overline{A} data to B bus		
H	H	H to L	X	H	X	Input	Output			
H	L	H to L	H to L	H	H	Output	Output	Stored \overline{A} data to B bus and stored \overline{B} data to A bus		

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	UNIT
I _{CC}	MAX	180	88	mA
I _{OH}	MAX	-15	-15	mA
I _{OL}	MAX	24	24	mA

SWITCHING CHARACTERISTICS

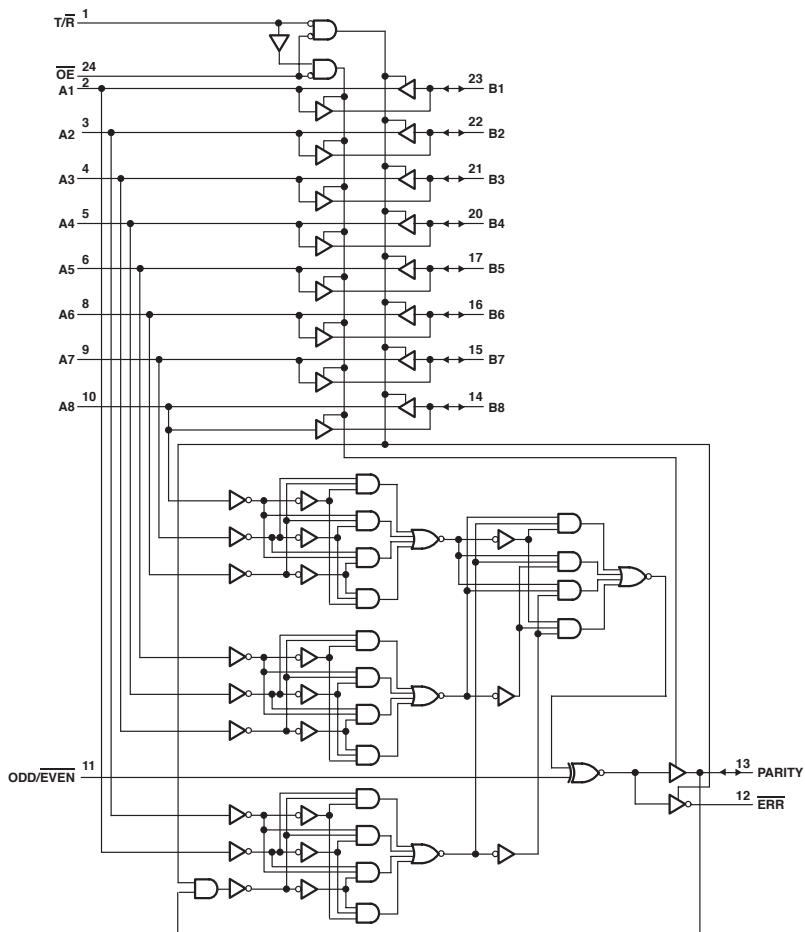
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS
t _w	CLKBA, CLKAB "H"		MIN	15	14.5
	CLKBA, CLKAB "L"		MIN	30	14.5
	DATA		MIN	30	-
t _{su}	A, B		MIN	15	10
	A, B		MIN	0	0
t _{PLH}	CLKBA	A	MAX	33	64
t _{PHL}				36	22
t _{PLH}	CLKAB	B	MAX	21	30
t _{PHL}				33	17
t _{PLH}	A	B	MAX	18	18
t _{PHL}				30	15
t _{PLH}	B	A	MAX	27	56
t _{PHL}				21	21
t _{PLH}	SBA (B "H")	A	MAX	48	62
t _{PHL}				32	25
t _{PLH}	SBA (B "L")	A	MAX	54	62
t _{PHL}				29	25
t _{PLH}	SAB (A "H")	B	MAX	35	25
t _{PHL}				27	22
t _{PLH}	SAB (A "L")	B	MAX	45	35
t _{PHL}				21	22
t _{PLH}	\overline{OEBA}	A	MAX	35	30
t _{PHL}				53	24
t _{PZH}	OEAB	B	MAX	29	22
t _{PZL}				33	22
t _{PHZ}	OEAB	B	MAX	39	14
t _{PLZ}				29	16

UNIT: ns

OCTAL BUS TRANSCEIVERS WITH 8-BIT PARITY GENERATORS/CHECKERS

- Combines SN74F245 and SN74F280B Functions in One Package
- 3-State Outputs
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	F	SN74 BCT	ABT	ACT 11	UNIT
ICCH	MAX	125	2	0.25	0.08	mA
ICCL	MAX	150	90	40	0.08	mA
ICZZ	MAX	145	1	0.25	0.08	mA
I _{DH} A1-A9	MAX	-3	-3	-32	-24	mA
I _{DH} B1-B9, PARITY, ERR	MAX	-12	-15	-32	-24	mA
I _{DL} A1-A8	MAX	24	24	64	24	mA
I _{DL} B1-B8, PARITY, ERR	MAX	64	64	64	24	mA

SWITCHING CHARACTERISTICS

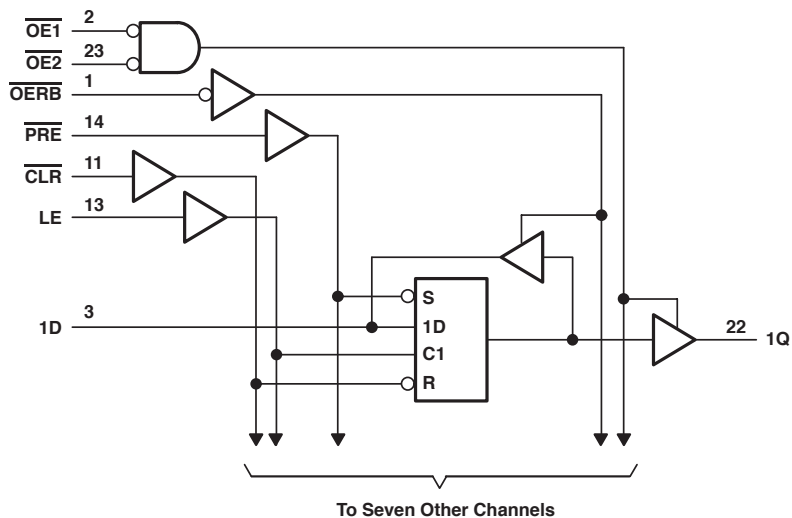
PARAMETER	INPUT	OUTPUT	MAX or MIN	F	SN74 BCT	ABT	ACT 11
I _{PLH}	A, B	B, A	MAX	8	6.6	4.6	9.4
I _{PHL}			MAX	8	9	4.3	9.4
I _{PLH}	A	PARITY	MAX	16	15.4	8.1	14.4
I _{PHL}			MAX	16	15.9	7.7	15
I _{PLH}	ODD/EVEN	PARITY, ERR	MAX	12	7.1	4.9	10.7
I _{PHL}			MAX	12.5	9	4.9	11.3
I _{PLH}	B	$\overline{\text{ERR}}$	MAX	22.5	15.3	7.9	23.6
I _{PHL}			MAX	22.5	15.5	7.8	24.6
I _{PLH}	PARITY	$\overline{\text{ERR}}$	MAX	16.5	13.2	7.7	14.6
I _{PHL}			MAX	17	13.9	7.5	14.7
I _{PZH}	$\overline{\text{OE}}$	A, B, PARITY	MAX	9	9.1	6.5	12.1
I _{PZL}			MAX	11	16.3	6.5	13.8
I _{PZH}	$\overline{\text{OE}}$	$\overline{\text{ERR}}$	MAX	9	9.1	6.6	12.1
I _{PZL}			MAX	11	16.3	9.2	13.8
I _{PHZ}	$\overline{\text{OE}}$	A, B, PARITY, ERR	MAX	8	9.1	6.2	12.1
I _{PLZ}			MAX	6.5	8	7.8	11.6

UNIT: ns

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

- 3-State I/O-Type Read-Back Inputs
- True Outputs
- Bus-Structured Pinout

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I _{CC}		MAX	73	mA
I _{OH}	Q	MAX	-2.6	mA
	D	MAX	-0.4	mA
I _{OL}	Q	MAX	24	mA
	D	MAX	8	mA

SWITCHING CHARACTERISTICS

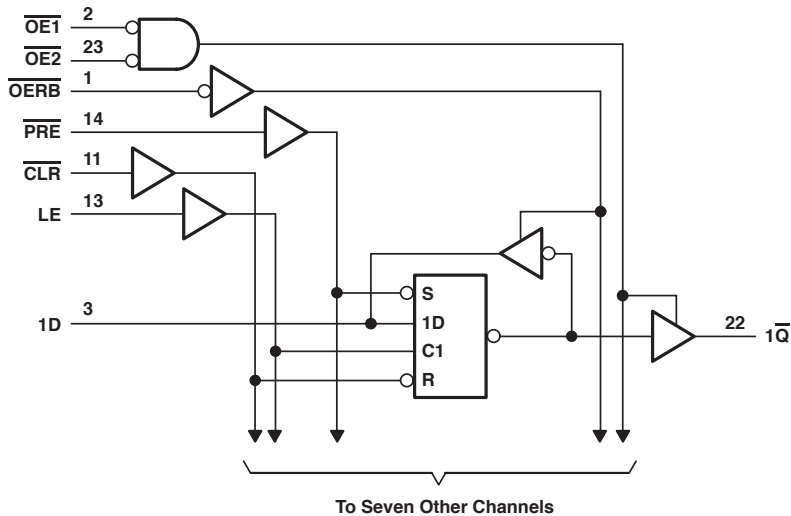
PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS
t _w	LE 'H'			MIN	10
	CLR 'L'			MIN	10
	PRE 'L'			MIN	10
t _{su}	DATA (LE)			MIN	10
	DATA (OERB)			MIN	10
t _h	DATA (LE)			MIN	5
t _{PLH}	D	Q	MAX	14	
t _{PHL}				18	
t _{PLH}	LE	Q	MAX	21	
t _{PHL}				27	
t _{PHL}	CLR	Q	MAX	29	
t _{PLH}		D		32	
t _{PLH}	PRE	Q	MAX	22	
t _{PHL}		D		28	
t _{en}	OERB	D	MAX	21	
t _{dis}				14	
t _{en}	OE1, OE2	Q	MAX	21	
t _{dis}				14	

UNIT: ns

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

- 3-State I/O-Type Read-Back Inputs
- Inverted Outputs
- Bus-Structured Pinout

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I _{CC}		MAX	79	mA
I _{OH}	Q	MAX	-2.6	mA
	D	MAX	-0.4	mA
I _{OL}	Q	MAX	24	mA
	D	MAX	8	mA

SWITCHING CHARACTERISTICS

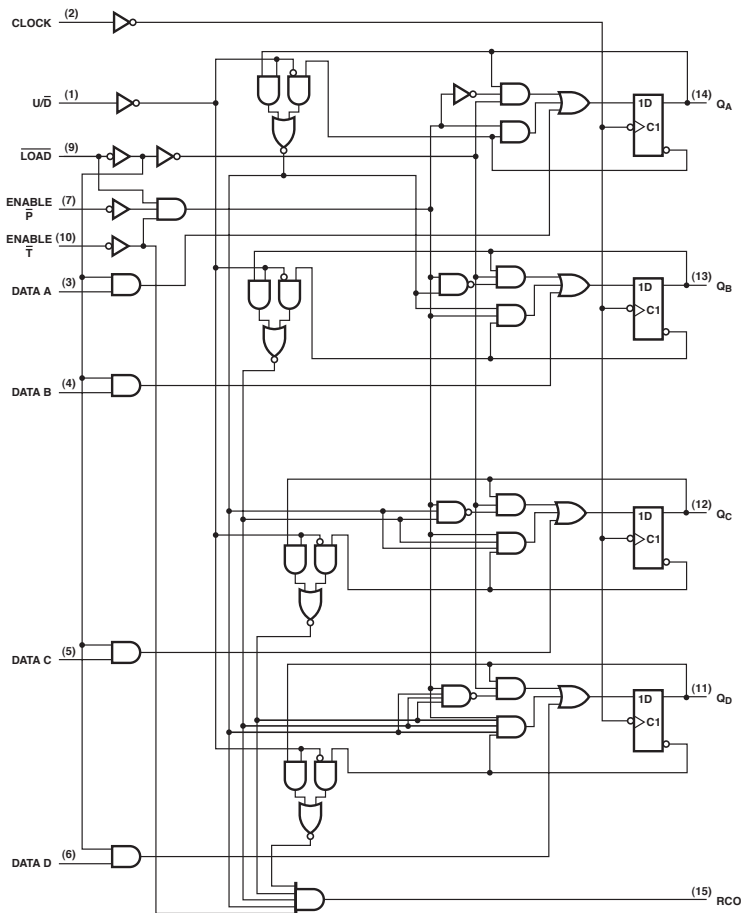
PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS
t _w	LE "H"			MIN	10
	$\overline{\text{CLR}}$ "L"			MIN	10
	PRE "L"			MIN	10
t _{su}	DATA (LE)			MIN	10
	DATA (O _{ERB})			MIN	10
t _h	DATA (LE)			MIN	5
t _{PLH}	D	$\overline{\text{Q}}$	MAX	20	
t _{PHL}				15	
t _{PLH}	LE	$\overline{\text{Q}}$	MAX	28	
t _{PHL}				22	
t _{PHL}	$\overline{\text{CLR}}$	$\overline{\text{Q}}$	MAX	24	
		D		26	
t _{PLH}	PRE	$\overline{\text{Q}}$	MAX	25	
t _{PHL}		D		28	
t _{en}	$\overline{\text{OERB}}$	D	MAX	21	
t _{es}				14	
t _{en}	$\overline{\text{OE1}}, \overline{\text{OE2}}$	$\overline{\text{Q}}$	MAX	21	
t _{es}				14	

UNIT: ns

SYNCHRONOUS 4-BIT UP/DOWN BINARY COUNTER

- Fully Synchronous Operation for Counting and Programming
- Internal Look-Ahead for Fast Counting
- Carry Output for n-Bit Cascading

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I _{CC}	MAX	34	mA
I _{OH}	MAX	-0.4	mA
I _{OL}	MAX	8	mA

SWITCHING CHARACTERISTICS

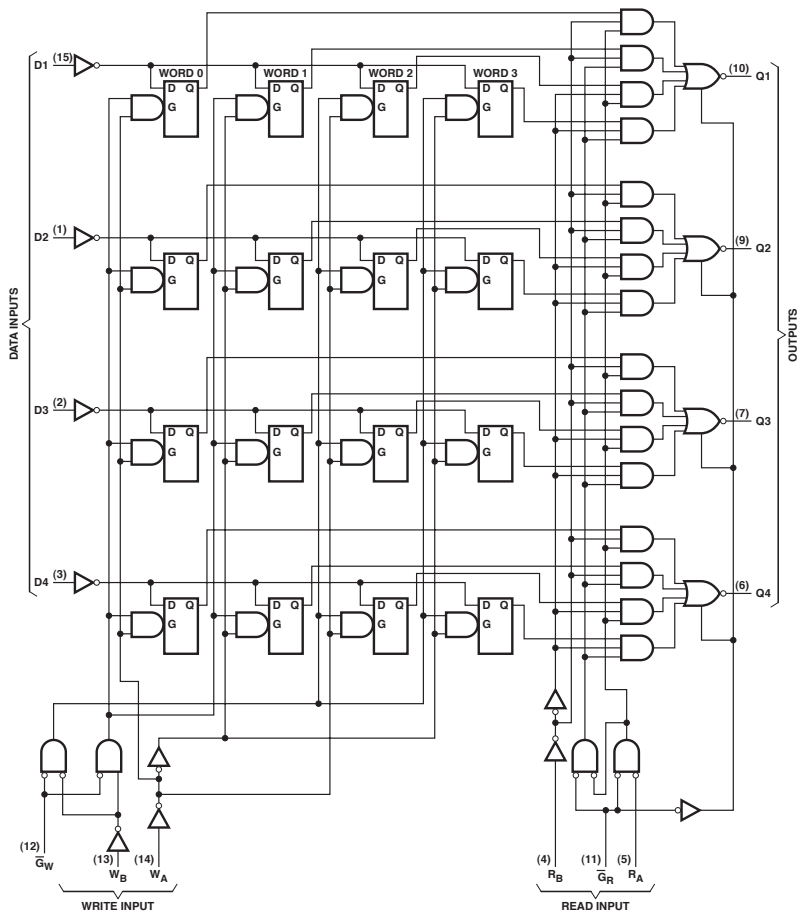
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS		
f _{max}			MIN	25		
t _w			MIN	20		
t _{su}			A, B, C, D	MIN	25	
			ENP, ENT	MIN	40	
			LOAD	MIN	30	
			U/D	MIN	45	
t _h					MIN	0
t _{PLH}			CLOCK	\overline{RCO}	MAX	40
t _{PHL}	60					
t _{PLH}	CLOCK	Q	MAX	27		
t _{PHL}				27		
t _{PLH}	\overline{ENT}	\overline{RCO}	MAX	17		
t _{PHL}				45		
t _{PLH}	U/D	\overline{RCO}	MAX	35		
t _{PHL}				40		

UNIT f_{max} : MHz other : ns

4-BY-4 REGISTER FILE

- Separate Read / Write Addressing Permits Simultaneous Reading and Writing
- Organized as 4 Words of 4 Bits
- Expandable to 512 Words of n-Bits
- 3-State Outputs

Logic Diagram



FUNCTION TABLE

WRITE INPUTS			WORD			
W _B	W _A	W _V	0	1	2	3
L	L	L	Q = D	Q ₀	Q ₀	Q ₀
L	H	L	Q ₀	Q = D	Q ₀	Q ₀
H	L	L	Q ₀	Q ₀	Q = D	Q ₀
H	H	L	Q ₀	Q ₀	Q ₀	Q = D
X	X	H	Q ₀	Q ₀	Q ₀	Q ₀

READ INPUTS			OUTPUTS			
R _B	R _A	R _R	Q1	Q2	Q3	Q4
L	L	L	W0B1	W0B2	W0B3	W0B4
L	H	L	W1B1	W1B2	W1B3	W1B4
H	L	L	W2B1	W2B2	W2B3	W2B4
H	H	L	W3B1	W3B2	W3B3	W3B4
X	X	H	Z	Z	Z	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	50	0.16	0.16	mA
I _{DH}	MAX	-2.6	-6	-6	mA
I _{OL}	MAX	8	6	6	mA

SWITCHING CHARACTERISTICS

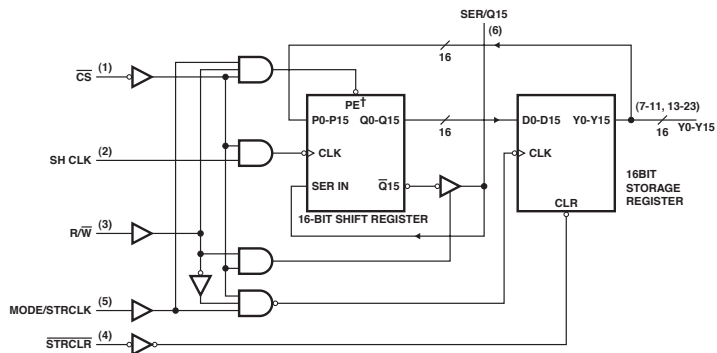
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	CD74 HC	CD74 HCT
t _w			MIN	25	24	30
t _{su} (D)			MIN	10	18	18
t _{su} (W)			MIN	15	18	30
t _h (D)			MIN	15	5	5
t _h (W)			MIN	5	5	5
t _{setup}			MIN	25	30	38
t _{PLH}	Read Select	Q	MAX	40	59	53
t _{PHL}				45	59	53
t _{PLH}	Write Enable	Q	MAX	45	75	75
t _{PHL}				50	75	75
t _{PLH}	Data	Q	MAX	45	75	75
t _{PHL}				40	75	75
t _{PZH}	Read Enable	Q	MAX	35	45	57
t _{PZL}				40	45	57
t _{PHZ}	Read Disable	Q	MAX	50	45	53
t _{PLZ}				35	45	53

UNIT: ns

16-BIT SHIFT REGISTER

- 16-Bit Serial-In, Serial-Out Shift Register with 16-Bit Parallel-Out Storage Register
- Performs Serial-to-Parallel Conversion

Logic Diagram



† When PE is active, data synchronously parallel loaded into the shift registers form the 16 P inputs and no shifting takes place.

FUNCTION TABLE

INPUTS					SHIFT REGISTER FUNCTIONS				STORAGE REGISTER FUNCTIONS		
CS	R/W	SH CLK	STRCLR	MODE/STRCLK	SER/Q15	SHIFT	READ FROM SERIAL INPUT	WRITE INTO SERIAL INPUT	PARALLEL LOAD	CLEAR	LOAD
H	X	X	X	X	Z	NO	NO	NO	NO		
X	X	X	L	X						YES	
L	L	↓	X	X	Z	YES	NO	YES	NO		
L	H	X	X	X	Q15		YES	NO	NO		NO
L	H	↓	X	L	Q14n	YES	YES	NO	NO		NO
L	H	↓	L	X	L	NO	YES		YES	YES;	NO
L	H	↓	H	X	Y15n	NO	YES		YES	NO	NO
L	L	X	H	↑	Z		NO			NO	YES

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
Icc		MAX	80	mA
I _{DH}	SER/Q15	MAX	-2.6	mA
	Y0-Y15	MAX	-0.4	mA
I _{OL}	SER/Q15	MAX	24	mA
	Y0-Y15	MAX	8	mA

SWITCHING CHARACTERISTICS

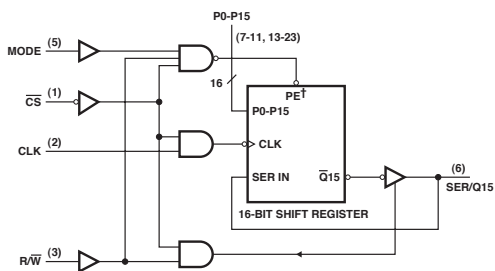
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
f _{max}				MIN	20
t _w	CLK			MIN	20
	CLR			MIN	20
t _{su}	SER/Q15			MIN	20
	Y0-Y15			MIN	20
	Mode			MIN	35
	R/W, CS			MIN	35
t _h	SER/Q15			MIN	0
	Y0-Y15			MIN	0
	Mode			MIN	0
t _{PLH}		STRCLR	Y0-Y15	MAX	40
t _{PLH}		MODE/STRCLK	Y0-Y15	MAX	45
t _{PHL}					45
t _{PLH}		SH CLK	SER/Q15	MAX	33
t _{PHL}					40

 UNIT f_{max} : MHz other : ns

16-BIT SHIFT REGISTER

- 16-Bit Parallel-In, Serial-Out Shift Register
- Performs Parallel-to-Serial Conversion

Logic Diagram



† When PE is active, data synchronously parallel loaded into the shift registers from the 16 P inputs and no shifting takes place.

FUNCTION TABLE

INPUTS				SER/ Q15	OPERATION
\overline{CS}	R/W	MODE	CLK		
H	X	X	X	Z	Do nothing
L	L	X	↓	Z	Shift and write (serial load)
L	H	L	↓	Q14n	Shift and read
L	H	H	↓	P15	parallel load

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I _{CC}		MAX	40	mA
I _{OH}	SER/Q15	MAX	-2.6	mA
	P0-P15	MAX	-0.4	mA
I _{OL}	SER/Q15	MAX	24	mA
	P0-P15	MAX	8	mA

SWITCHING CHARACTERISTICS

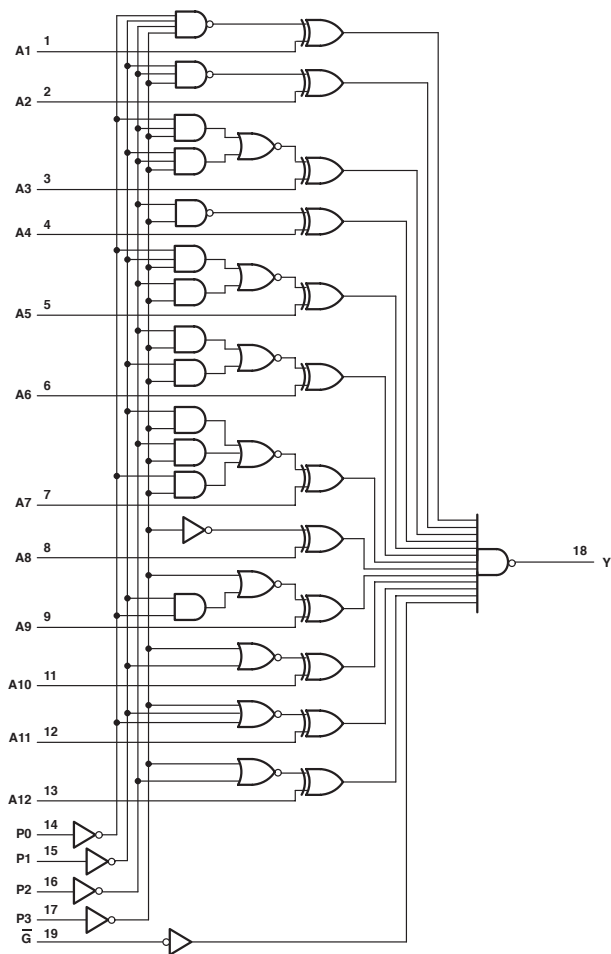
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
t _{max}				MIN	20
t _v	CLK			MIN	20
	CLR				20
t _{su}	SER/Q15			MIN	20
	P0-P15				20
	Mode				35
	$\overline{R/W}, \overline{CS}$				35
t _h	SER/Q15			MIN	0
	P0-P15				0
	Mode				0
t _{PLH}	CLK		SER/Q15	MAX	33
t _{PHL}	CLK		SER/Q15	MAX	40
t _{PZH}	$\overline{CS}, \overline{R/W}$		SER/Q15	MAX	45
t _{PZL}	$\overline{CS}, \overline{R/W}$		SER/Q15	MAX	45
t _{PHZ}	CS, R/W		SER/Q15	MAX	40
t _{PLZ}	CS, R/W		SER/Q15	MAX	40

UNIT f_{max} : MHz other : ns

ADDRESS COMPARATOR

- 12-Bit Address Comparator with Enable

Logic Diagram



FUNCTION TABLE

G	INPUTS													OUTPUT			
	P3	P2	P1	P0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	Y
L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L
L	L	L	H	H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	L	L	H	H	L	L	L	H	H	H	H	H	H	H	H	H	L
L	L	H	L	L	L	L	L	L	H	H	H	H	H	H	H	H	L
L	L	H	L	H	L	L	L	L	L	H	H	H	H	H	H	H	L
L	L	H	H	L	L	L	L	L	L	L	H	H	H	H	H	H	L
L	L	H	H	H	L	L	L	L	L	L	L	H	H	H	H	H	L
L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L
L	H	L	L	H	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L
L	H	H	L	H	L	L	L	L	L	L	L	L	L	L	H	H	L
L	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	H	L
L	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L
L	All other combinations																H
H	Any combination																H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 HC	UNIT
I _{CC}	MAX	28	0.08	mA
I _{OH}	MAX	-2.6	-4	mA
I _{OL}	MAX	24	4	mA

SWITCHING CHARACTERISTICS

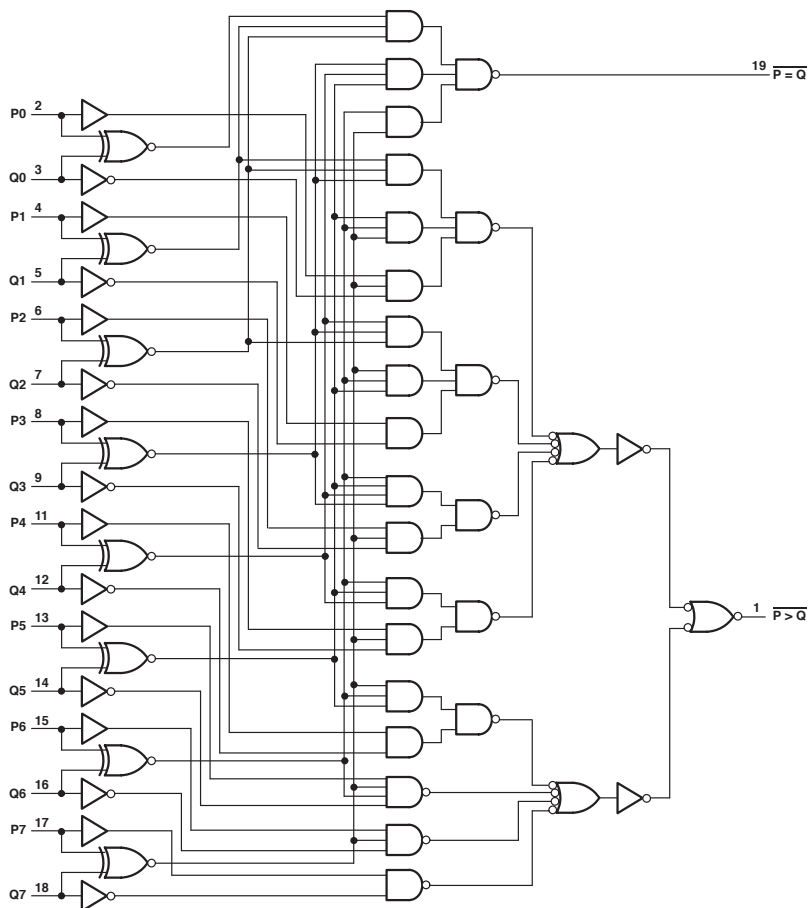
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 HC
t _{PLH}	Any P	Y	MAX	25	375
t _{PHL}				35	375
t _{PLH}	Any A	Y	MAX	22	78
t _{PHL}				30	78
t _{PLH}	G	Y	MAX	13	31
t _{PHL}				25	31

UNIT: ns

8-BIT IDENTITY COMPARATOR

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs
- 20k Ω Pullup Resistors on the Q Inputs

Logic Diagram



FUNCTION TABLE

DATA INPUT P, Q	OUTPUTS	
	$\overline{P=Q}$	$\overline{P>Q}$
P=Q	L	H
P>Q	H	L
P<Q	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	UNIT
I _{CC}	MAX	70	0.11	mA
I _{DH}	MAX	-0.4	-4	mA
I _{OL}	MAX	24	4	mA

SWITCHING CHARACTERISTICS

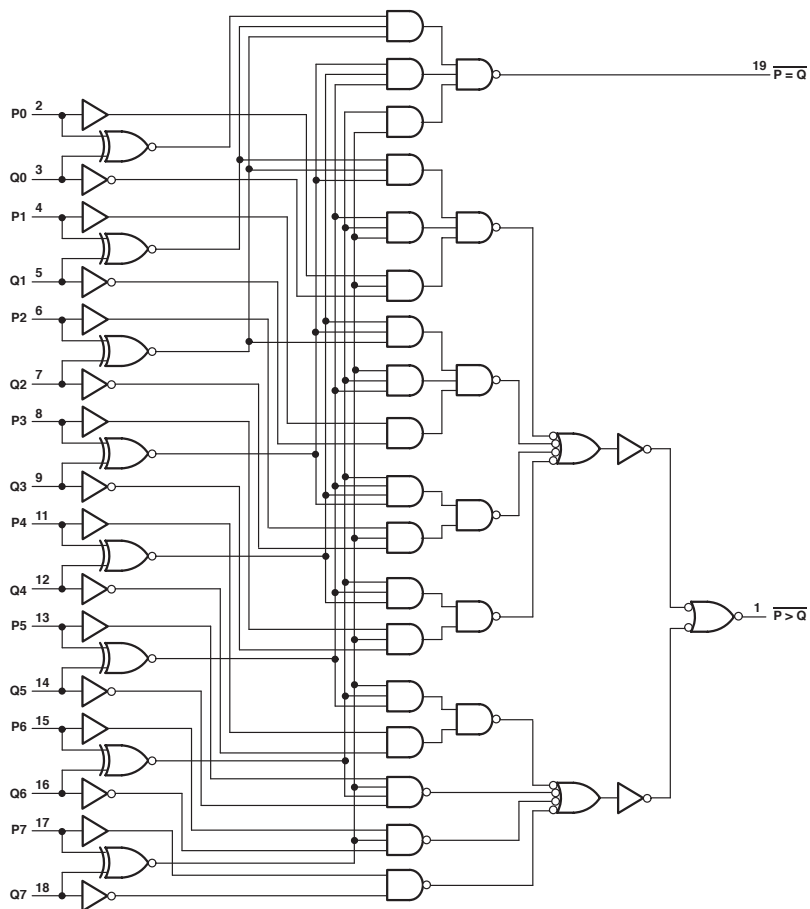
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
t _{PLH}	P	$\overline{P=Q}$	MAX	25	69
t _{PHL}				25	69
t _{PLH}	Q	$\overline{P=Q}$	MAX	25	69
t _{PHL}				25	69
t _{PLH}	P	$\overline{P>Q}$	MAX	30	69
t _{PHL}				30	69
t _{PLH}	Q	$\overline{P>Q}$	MAX	30	69
t _{PHL}				30	69

UNIT: ns

8-BIT IDENTITY COMPARATOR

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs

Logic Diagram



FUNCTION TABLE

DATA INPUT P, Q	OUTPUTS	
	$\overline{P=Q}$	$\overline{P>Q}$
$\overline{P=Q}$	L	H
$\overline{P>Q}$	H	L
$\overline{P<Q}$	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	SN74 HC	UNIT
I_{CC}	MAX	65	0.08	mA
I_{OH}	MAX	-0.4	-4	mA
I_{OL}	MAX	24	4	mA

SWITCHING CHARACTERISTICS

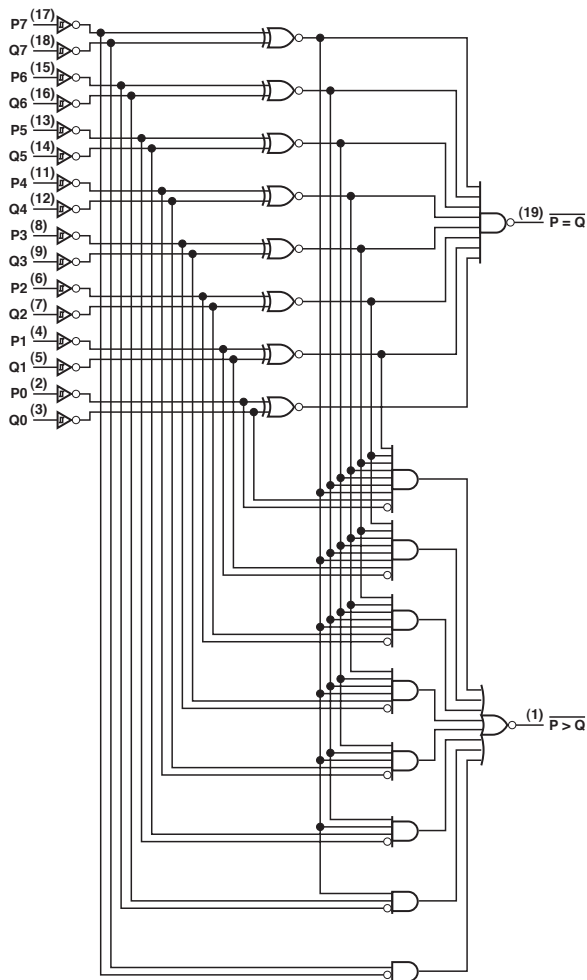
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	SN74 HC
t_{PLH}	P	$\overline{P=Q}$	MAX	25	69
t_{PHL}				25	69
t_{PLH}	Q	$\overline{P=Q}$	MAX	25	69
t_{PHL}				25	69
t_{PLH}	P	$\overline{P>Q}$	MAX	30	69
t_{PHL}				30	69
t_{PLH}	Q	$\overline{P>Q}$	MAX	30	69
t_{PHL}				30	69

UNIT: ns

8-BIT IDENTITY COMPARATOR

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs

Logic Diagram



FUNCTION TABLE

DATA	INPUTS		OUTPUTS	
	ENABLE		$\overline{P=Q}$	$\overline{P>Q}$
P, Q	$\overline{G1}$	$\overline{G2}$		
P=Q	L	L	L	H
P>Q	L	L	H	L
P<Q	L	L	H	H
X	H	H	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	UNIT
I _{CC}	MAX	75	mA
I _{QH}	MAX	-0.4	mA
I _{QL}	MAX	24	mA

SWITCHING CHARACTERISTICS

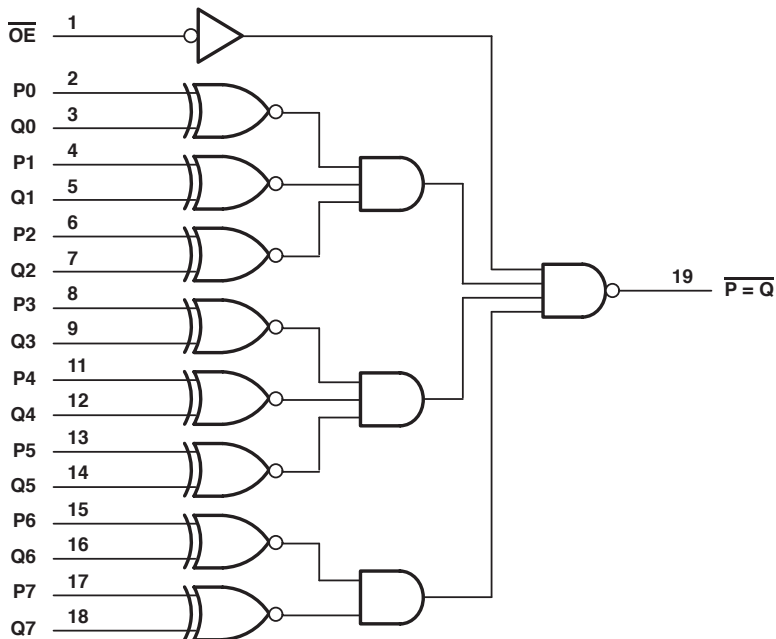
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS
t _{PLH}	P	$\overline{P=Q}$	MAX	25
t _{PHL}				30
t _{PLH}	Q	$\overline{P=Q}$	MAX	25
t _{PHL}				30
t _{PLH}	$\overline{G1}$	$\overline{P=Q}$	MAX	20
t _{PHL}				30
t _{PLH}	P	$\overline{P>Q}$	MAX	30
t _{PHL}				30
t _{PLH}	Q	$\overline{P>Q}$	MAX	30
t _{PHL}				30
t _{PLH}	$\overline{G2}$	$\overline{P>Q}$	MAX	30
t _{PHL}				25

UNIT: ns

8-BIT IDENTITY COMPARATOR

- Totem-Pole Outputs
- Hysteresis at P and Q Inputs

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
DATA	ENABLE	P=Q
P, Q	\bar{G}	
P=Q	L	L
P>Q	L	H
P<Q	L	H
X	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LS	ALS	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	65	19	0.08	0.16	0.16	mA
I _{DH}	MAX	-0.4	-2.6	-4	-4	-4	mA
I _{OL}	MAX	24	24	4	4	4	mA

SWITCHING CHARACTERISTICS

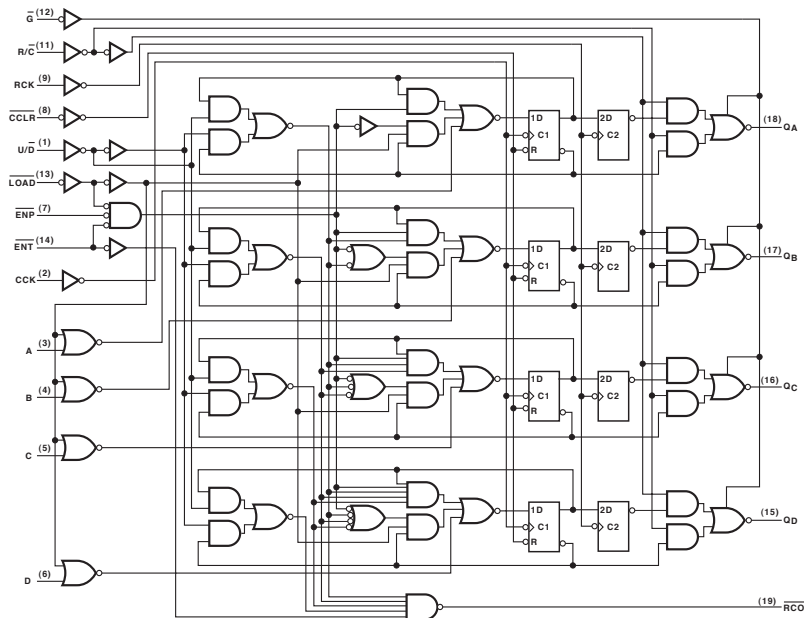
PARAMETER	INPUT	OUTPUT	MAX or MIN	LS	ALS	SN74 HC	CD74 HC	CD74 HCT
t _{PLH}	P	$\overline{P = Q}$	MAX	18	12	53	51	51
t _{PHL}				23	20	53	51	51
t _{PLH}	\bar{Q}	$\overline{P = Q}$	MAX	18	12	53	51	51
t _{PHL}				23	20	53	51	51
t _{PLH}	\bar{G}	$\overline{P = Q}$	MAX	18	12	30	36	36
t _{PHL}				20	22	30	36	36

UNIT: ns

SYNCHRONOUS UP/DOWN COUNTER WITH OUTPUT REGISTER, MULTIPLEXED THREE-STATE OUTPUT

- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- Binary Counter, Direct Clear

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I _{CC}		MAX	70	mA
I _{OH}	\overline{Q}	MAX	-2.6	mA
	\overline{RCO}		-0.4	mA
I _{OL}	Q	MAX	24	mA
	\overline{RCO}		8	mA

SWITCHING CHARACTERISTICS

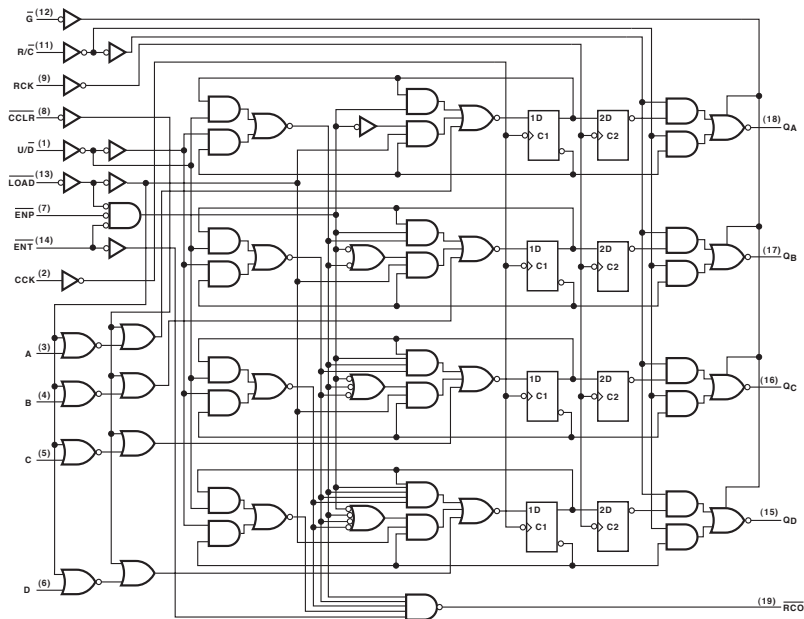
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS
t _w	CCK			MIN	25
	RCK				25
t _{su}	A thru D			MIN	30
	\overline{ENT} , \overline{ENP}				30
	U/D				35
t _h				MIN	0
t _{PLH}	CCK '	\overline{RCO}	MAX	40	
t _{PHL}				40	
t _{PLH}	\overline{ENT}	\overline{RCO}	MAX	20	
t _{PHL}				20	
t _{PLH}	CCK '	Q	MAX	20	
t _{PHL}				25	
t _{PLH}	RCK '	Q	MAX	20	
t _{PHL}				25	
t _{PHL}	\overline{CCLR} '	Q	MAX	40	
t _{PLH}	R / \overline{C}	Q	MAX	25	
t _{PHL}				25	

UNIT: ns

SYNCHRONOUS UP/DOWN COUNTER WITH OUTPUT REGISTER, MULTIPLEXED THREE-STATE OUTPUT

- Multiplexed Outputs for Counter or Latched Data
- 3-State Outputs Drive Bus Lines Directly
- Binary Counter, Synchronous Clear

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	LS	UNIT
I _{CC}		MAX	70	mA
I _{OH}	\overline{Q}	MAX	-2.6	mA
	\overline{RCO}	MAX	-0.4	mA
I _{OL}	\overline{Q}	MAX	24	mA
	\overline{RCO}	MAX	8	mA

SWITCHING CHARACTERISTICS

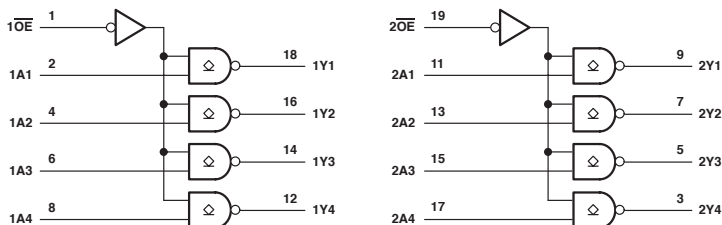
PARAMETER		INPUT	OUTPUT	MAX or MIN	LS	
t _w	CCK			MIN	25	
	RCK			25		
t _{su}	A thru D			MIN	30	
	\overline{ENT} , \overline{ENP}			30		
	U/D			35		
	\overline{CCLR}			30		
t _h				MIN	0	
$\overline{P}LH$	CCK ' 1			\overline{RCO}	MAX	40
$\overline{P}HL$					40	
$\overline{P}LH$	\overline{ENT}			\overline{RCO}	MAX	20
$\overline{P}HL$		20				
$\overline{P}LH$	CCK ' 1	\overline{Q}	MAX	20		
$\overline{P}HL$			25			
$\overline{P}LH$	RCK ' 1	\overline{Q}	MAX	20		
$\overline{P}HL$			25			
$\overline{P}LH$	R/C	\overline{Q}	MAX	25		
$\overline{P}HL$			25			

UNIT: ns

OCTAL BUFFER/LINE DRIVER/LINE RECEIVER WITH OPEN-COLLECTOR OUTPUTS

- Eliminate the Need for 3-State Overlap Protection
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of SN74AS240A

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	SN74 BCT	UNIT
I_{CC}	MAX	80	86	mA
V_{OH}	MAX	5.5	5.5	V
I_{OL}	MAX	64	64	mA

SWITCHING CHARACTERISTICS

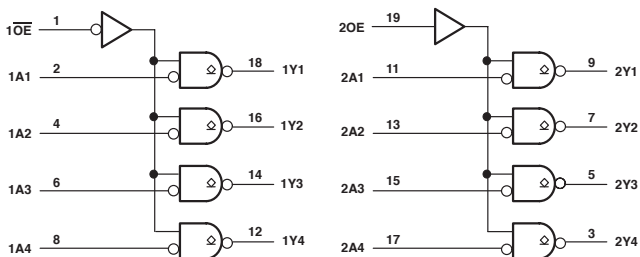
PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	SN74 BCT
t_{PLH}	A	Y	MAX	19	11.3
t_{PHL}				6	4.2
t_{PLH}	\overline{OE}	Y	MAX	19.5	16.5
t_{PHL}				7.5	10.3

UNIT:ns

OCTAL BUFFER/LINE DRIVER/LINE RECEIVER WITH OPEN-COLLECTOR OUTPUTS

- Eliminate the Need for 3-State Overlap Protection
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of SN74AS241

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	SN74 BCT	SN64 BCT	UNIT
I_{CC}	MAX	95	77	77	mA
V_{OH}	MAX	5.5	5.5	5.5	V
I_{OL}	MAX	64	64	64	mA

SWITCHING CHARACTERISTICS

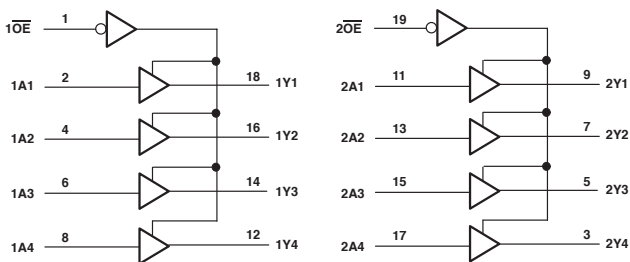
PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	SN74 BCT	SN64 BCT
t_{PLH}	A	Y	MAX	18.5	10.1	10.1
t_{PHL}				6	6.6	6.6
t_{PLH}	$\overline{1OE}$	1Y	MAX	20	19.7	19.7
t_{PHL}				7	6.9	6.9
t_{PLH}	2OE	2Y	MAX	21	18	18
t_{PHL}				7.5	8.5	8.5

UNIT:ns

OCTAL BUFFER/LINE DRIVER/LINE RECEIVER WITH OPEN-COLLECTOR OUTPUTS

- Open-Collector Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading
- Open-Collector Versions of SN74ALS244 and SN74AS244

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	SN74 BCT	UNIT
I_{CC}	MAX	19	94	76	mA
V_{OH}	MAX	5.5	5.5	5.5	V
I_{OL}	MAX	24	64	64	mA

SWITCHING CHARACTERISTICS

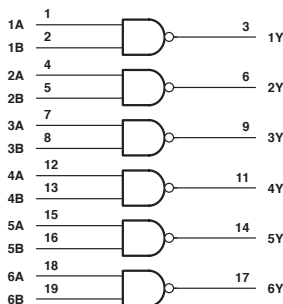
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 BCT
t_{PLH}	A	Y	MAX	15	18.5	10
t_{PHL}				12	6	7.2
t_{PLH}	\overline{OE}	Y	MAX	16	18.5	17.5
t_{PHL}				13	7	9.9

UNIT:ns

HEX 2-INPUT NAND DRIVERS

- $Y = \overline{A \cdot B}$
- High Capacitive-Drive Capability

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	SN74 HC	UNIT
I_{CC}	MAX	12	27	0.08	mA
I_{OH}	MAX	-15	-48	-6	mA
I_{OL}	MAX	24	48	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC
t_{PLH}	A, B	Y	MAX	7	4	25
t_{PHL}			MAX	8	4	25

UNIT:ns

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HEX 2-INPUT NOR DRIVERS

- $Y = \overline{A + B}$
- High Capacitive-Drive Capability

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	L
X	H	L
L	L	H

RECOMMENDED OPERATING CONDITIONS

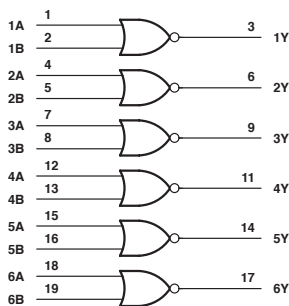
PARAMETER	MAX or MIN	ALS	AS	SN74 HC	UNIT
I_{CC}	MAX	14	32	0.08	mA
I_{OH}	MAX	-15	-48	-6	mA
I_{OL}	MAX	24	48	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC
t_{PLH}	A, B	Y	MAX	7	4.3	24
t_{PHL}			MAX	8	4.3	24

UNIT:ns

Logic Diagram



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HEX 2-INPUT AND DRIVERS

- $Y = A + B$
- High Capacitive-Drive Capability

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	H
L	X	L
X	L	L

RECOMMENDED OPERATING CONDITIONS

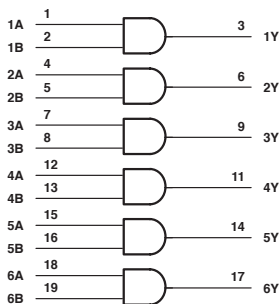
PARAMETER	MAX or MIN	SN74 HC	AS	UNIT
I_{CC}	MAX	0.08	33	mA
I_{OH}	MAX	-6	-48	mA
I_{OL}	MAX	6	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	AS
t_{PLH}	A, B	Y	MAX	25	6
t_{PHL}			MAX	25	6

UNIT:ns

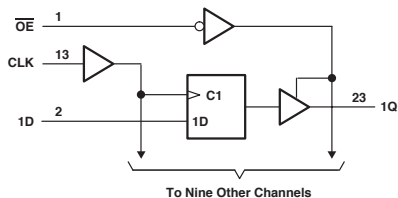
Logic Diagram



10-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUT

- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	ABT	LVC	UNIT
I _{CC}	MAX	113	38	0.01	mA
I _{OH}	MAX	-24	-32	-24	mA
I _{OL}	MAX	48	64	24	mA

SWITCHING CHARACTERISTICS

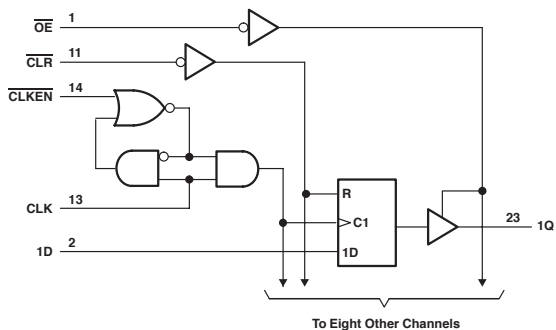
PARAMETER	INPUT	OUTPUT	MAX or MIN	AS	ABT	LVC 3V
t _w	High		MIN	8	2.9	3.3
	Low		MIN	8	3.8	3.3
t _{su}			MIN	6	2.1	1.9
			MIN	0	1.3	1.5
t _{PH}	CLK	Q	MAX	7.5	6.2	7.3
t _{PHL}			13	6.7	7.3	
t _{PZH}	OE	Q	MAX	11	5.8	7.6
t _{PZL}			12	6.3	7.6	
t _{PHZ}	OE	Q	MAX	8	6.7	6.2
t _{PLZ}			8	6.5	6.2	

UNIT: ns

9-BIT BUS INTERFACE FLIP-FLOP WITH 3-STATE OUTPUT

- Functionally Equivalent to AMD's AM29823 and AM29824
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT
\overline{OE}	\overline{CLR}	\overline{CLKEN}	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q_0
H	X	X	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	ABT	LVC 3V	UNIT
I_{CC}	MAX	103	38	0.01	mA
I_{OH}	MAX	-24	-32	-24	mA
I_{OL}	MAX	48	64	24	mA

SWITCHING CHARACTERISTICS

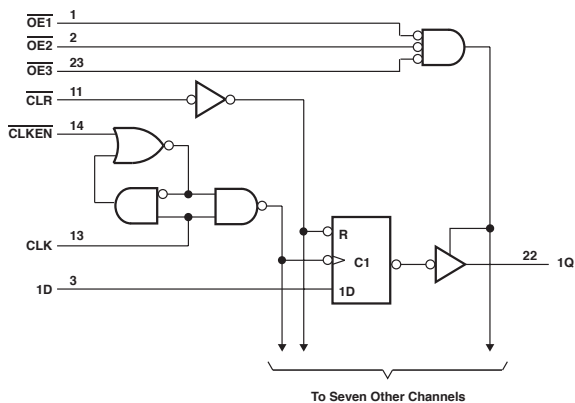
PARAMETER		INPUT	OUTPUT	MAX or MIN	AS	ABT	LVC 3V
t_{bv}	\overline{CLR} "L"			MIN	6.5	5.5	3.3
	CLK "H"				8	2.9	3.3
	CLK "L"				8	3.8	3.3
t_{bu}	\overline{CLR}			MIN	8	2.5	1
	DATA				6	2.1	1.3
	\overline{CLKEN} "H"				7.5	2	1.8
	\overline{CLKEN} "L"				-	3.3	1.8
t_h	DATA			MIN	-	1.3	2
	\overline{CLKEN} "H"				0	1	-
	\overline{CLKEN} "L"	0	2		1.3		
t_{PLH}	CLK	Q	MAX	7.5	6.8	8	
t_{PHL}				13	6.7	8	
t_{PHL}	\overline{CLR}	Q	MAX	15.5	7.1	7.9	
t_{PZH}	\overline{OE}	Q	MAX	11	6	7.2	
t_{PZL}				12	6.5	7.2	
t_{PHZ}	\overline{OE}	Q	MAX	8	7.5	6	
t_{PLZ}				8	6.9	6	

UNIT: ns

8-BIT BUS INTERFACE FLIP-FLOP WITH 3-STATE OUTPUT

- Improved I_{OH} Specifications (Max: -24mA)
- Outputs Have Undershoot-Protection Circuitry
- Power-Up High-Impedance State

Logic Diagram



FUNCTION TABLE

\overline{OE}	INPUTS				OUTPUT
	CLR	CLKEN	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	H	X	X	Q ₀
H	X	X	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	UNIT
I _{CC}	MAX	95	mA
I _{DH}	MAX	-24	mA
I _{OL}	MAX	48	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	AS
t _w	CLR "L"		Q	MIN	4
	CLK "H"				8
	CLK "L"				8
t _{su}	CLR			MIN	8
	DATA				6
	CLKEN				6
t _h		MIN	0		
t _{PLH}		CLK	Q	MAX	7.5
t _{PHL}		CLK	Q	MAX	13
t _{PHL}		CLR	Q	MAX	15.5
t _{PZH}		\overline{OE}	Q	MAX	11
t _{PZL}		\overline{OE}	Q	MAX	12
t _{PHZ}		\overline{OE}	Q	MAX	8
t _{PLZ}		\overline{OE}	Q	MAX	8

UNIT: ns

10-BIT BUFFERS/BUS DRIVERS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	H	H
L	L	L	L
X	H	X	Z
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

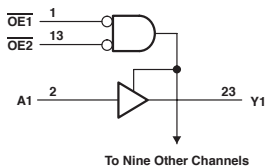
PARAMETER	MAX or MIN	ABT	AC 11	ACT 11	LVC 3V	UNIT
ICC	MAX	40	0.08	0.08	0.01	mA
IOH	MAX	-32	-24	-24	-24	mA
IOL	MAX	64	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	AC 11	ACT 11	LVC 3V	
tPLH	A	Y	MAX	4.8	8.7	9.2	6.7	
				4.7	9.7	11.2	6.7	
tPZH	\overline{OE}		MAX	5.9	9.7	11.3	7.3	
				6.9	13	14	7.3	
tPHZ	\overline{OE}		MAX	MAX	6.8	9.1	12	6.7
					6.9	8.8	11.6	6.7

UNIT: ns

Logic Diagram



10-BIT BUFFERS/BUS DRIVERS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- 74AC11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)
- 74ACT11xxx: Product Available in Reduced-Noise Advanced CMOS (11000 Series)

FUNCTION TABLE

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	H	L
L	L	L	H
H	X	X	Z
X	H	X	Z

RECOMMENDED OPERATING CONDITIONS

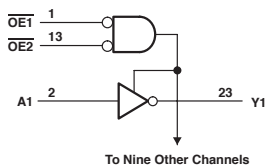
PARAMETER	MAX or MIN	AC 11	ACT 11	LVC 3V	UNIT
ICC	MAX	0.08	0.08	0.01	mA
IOH	MAX	-24	-24	-24	mA
IOL	MAX	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC 11	ACT 11	LVC 3V	
tPLH	A	Y	MAX	9.5	10.2	6.7	
				10.4	11.7	6.7	
tPZH	\overline{OE}		MAX	10.7	12.1	7.3	
				13.2	14.7	7.3	
tPHZ	\overline{OE}		MAX	MAX	9.6	12.3	6.7
					9.2	11.7	6.7

UNIT: ns

Logic Diagram



HEX 2-INPUT OR DRIVERS

- $Y = A + B$
- High Capacitive-Drive Capability

FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

RECOMMENDED OPERATING CONDITIONS

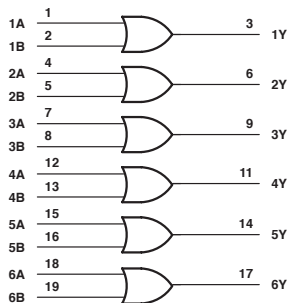
PARAMETER	MAX or MIN	ALS	AS	SN74 HC	UNIT
I_{CC}	MAX	16	36	0.08	mA
I_{OH}	MAX	-15	-48	-6	mA
I_{OL}	MAX	24	48	6	mA

SWITCHING CHARACTERISTICS

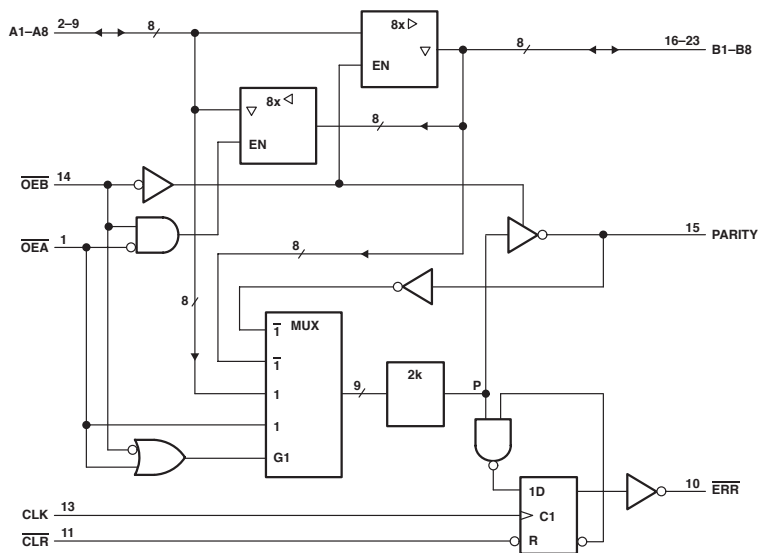
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	SN74 HC
t_{PLH}	A, B	Y	MAX	9	6.3	25
t_{PHL}			MAX	8	6.3	25

UNIT:ns

Logic Diagram



Logic Diagram



FUNCTION TABLE

INPUTS						OUTPUTS AND I/O				FUNCTION
OEB	OEA	CLR	CLK	A ₁ Σ OF H's Odd Even	B ₁ Σ OF H's Odd Even	A	B	PARITY	ERR	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Check error flag register
H	H	H	↑	No ↑ L H ↑	X X Odd Even	X	Z	Z	Z NC H H L	Isolation
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT ERR	FUNCTION
CLR	CLK	POINT P	ERR _{n-1} †	ERR	
H	↑	H	H	H	Sample
H	↑	X	L	H	
H	↑	L	X	L	
L	X	X	X	H	Clear

† The state of ERR before any changes at CLR, CLK, or point P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I _{CC}	MAX	38	mA
I _{DH}	MAX	-32	mA
I _{OL}	MAX	64	mA

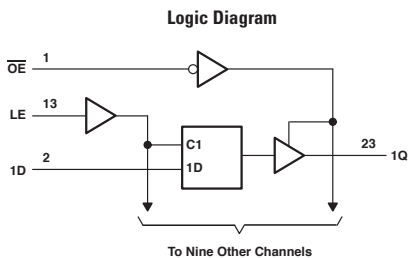
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t _{PLH}	A or B	B or A	MAX	5.3
				5.3
t _{PLH}	A	PARITY	MAX	11.2
				11
t _{PZH}	OE	PARITY	MAX	10.5
				10
t _{PLH}	CLR	ERR	MAX	5.2
				6.2
t _{PZH}	OE	A,B, or PARITY	MAX	6.5
				6.5
t _{PLZ}	OE	A,B, or PARITY	MAX	7.9
				8.1

UNIT: ns

10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Provide Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State



FUNCTION TABLE

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	L
L	H	L	H
L	L	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	ABT	LVC 3V	UNIT
I _{CC}	MAX	62	94	38	0.01	mA
I _{OH}	MAX	-2.6	-24	-32	-24	mA
I _{OL}	MAX	24	48	64	24	mA

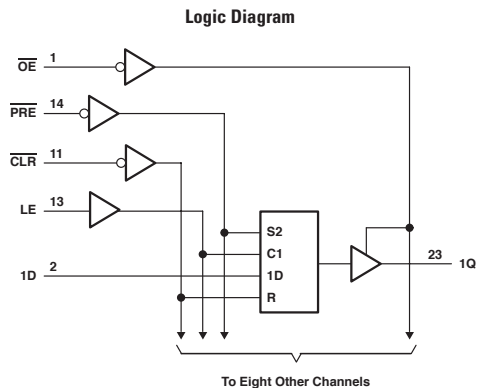
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS	ABT	LVC 3V
t _w			MIN	20	4	3.3	3.3
t _{su}	High			10	2.5	2.5	2.1
t _{su}	Low			10	2.5	1.5	2.1
t _h				5	2.5	1.5	1
t _{PLH}	D	Q	MAX	13	6.5	6.2	6.7
t _{PHL}				13	10.5	6.2	6.7
t _{PLH}	LE	Q	MAX	21	12	6.5	7.6
t _{PHL}				26	12	6.7	7.6
t _{PZH}	$\overline{\text{OE}}$	Q	MAX	12	14	5.3	7.2
t _{PZL}				12	16	6.3	7.2
t _{PHZ}	$\overline{\text{OE}}$	Q	MAX	10	8	7.1	5.9
t _{PLZ}				12	8	6.5	5.9

UNIT: ns

9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Provides Extra Bus-Driving Latches Necessary for Wider Address/Data Paths or Buses with Parity
- Power-Up High-Impedance State



FUNCTION TABLE

INPUTS					OUTPUT
PRE	CLR	OE	LE	D	
L	H	L	X	X	H
H	L	L	X	X	L
L	L	L	X	X	H
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q ₀
X	X	H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

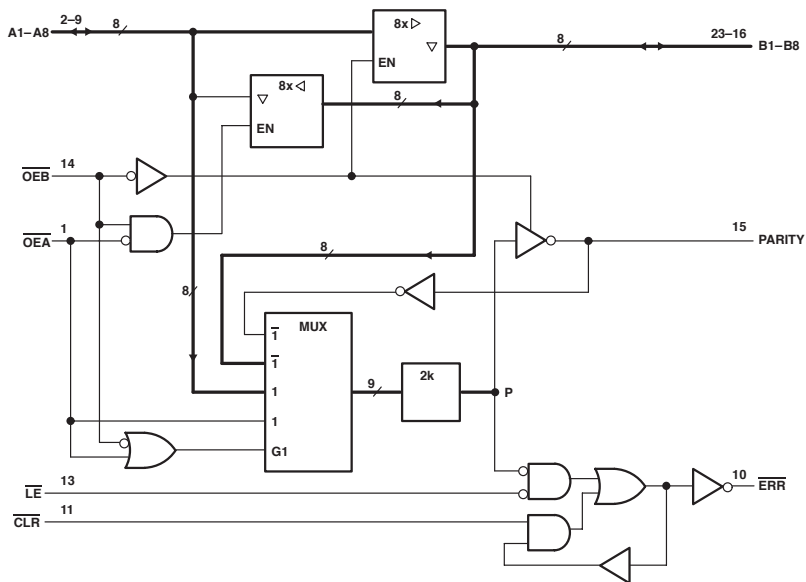
PARAMETER	MAX or MIN	ALS	AS	ABT	UNIT
I _{CC}	MAX	67	92	34	mA
I _{OH}	MAX	-2.6	-24	-32	mA
I _{OL}	MAX	24	48	64	mA

SWITCHING CHARACTERISTICS

PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS	AS	ABT
t _w	CLR "L"			MIN	35	4	5.5
	PRE "L"				35	4	4.5
	LE "H"				20	4	-
	LE "L"				-	4	3.4
t _{su}	LE "L"			MIN	10	2.5	2.5
	LE "H"				10	2.5	3
	PRE inactive				-	15	1.6
	CLR inactive				-	14	2
t _h	LE "L"			MIN	5	2.5	1
	LE "H"				5	2.5	1.5
t _{PLH}	D	Q	MAX	13	6.5	6.7	
t _{PHL}				18	9	7.2	
t _{PLH}	LE	Q	MAX	21	12	7.2	
t _{PHL}				26	12	6.9	
t _{PLH}	CLR	Q	MAX	-	-	7.1	
t _{PHL}				23	13	8	
t _{PLH}	PRE	Q	MAX	22	10	7.4	
t _{PHL}				-	-	7.2	
t _{PZH}	OE	Q	MAX	12	10.5	5.7	
t _{PZL}				14	13.5	6.5	
t _{PHZ}	OE	Q	MAX	10	8	6.8	
t _{PLZ}				12	8	5.9	

UNIT: ns

Logic Diagram



FUNCTION TABLE

INPUTS						OUTPUT AND I/Os				FUNCTION
OEB	OEA	CLR	LE	A _Σ OF H Odd Even	B _Σ OF H NA	A	B	PARITY	ERR‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	L	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
H	L	H	H	X	X	X	NA	NA	NC	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error flag register
H	H	H	H	X	X	Z	Z	Z	NC	Isolation§ (parity check)
			L	H					H	
			L	L					L	
			L	L					L	
L	L	X	X	Odd Even	NA	NA	A	H L	A data to B bus and generate inverted parity	

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT ERR	FUNCTION
CLR	LE	POINT P	ERR _{n-1†}		
L	L	L H	X	L H	Pass
H	L	L	X	L	Sample
		X H	L H	L H	
L	H	X	X	H	Clear
H	H	X	L	L H	Store

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I _{CC}	MAX	38	mA
I _{OH}	MAX	-32	mA
I _{OL}	MAX	64	mA

SWITCHING CHARACTERISTICS

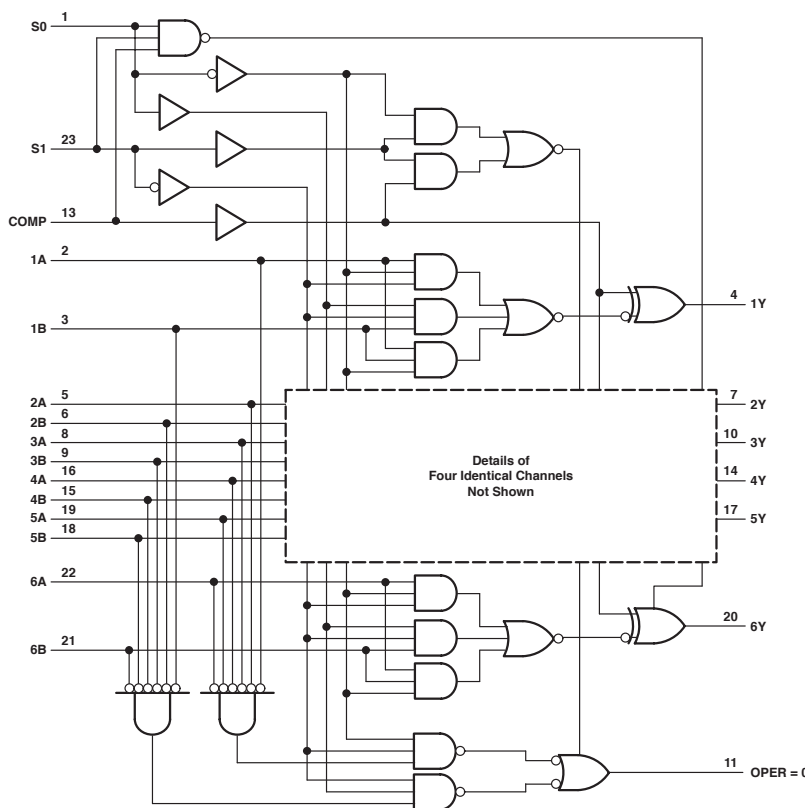
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t _{PLH}	A or B	B or A	MAX	5.3
t _{PHL}				5.3
t _{PLH}	A	PARITY	MAX	11.2
t _{PHL}				11
t _{PLH}	OE	PARITY	MAX	10.5
t _{PHL}				10
t _{PLH}	CLR	ERR	MAX	6.2
t _{PHL}				6
t _{PLH}	LE	ERR	MAX	6.6
t _{PHL}				6.6
t _{PLH}	B or RARITY	ERR	MAX	11.7
t _{PHL}				12.8
t _{PZH}	OE	A or B or PARITY	MAX	6.7
t _{PZL}				6.7
t _{PHZ}	OE	A or B or PARITY	MAX	7.9
t _{PLZ}				8.1

UNIT: ns

HEX 2-TO-1 UNIVERSAL MULTIPLEXERS

- Select True or Complementary Data
- Perform AND/NAND (Masking) of A or B Operand
- Cascadable to Expand Number of Operands
- Detect Zeros on A or B Operands
- 3-State Outputs Interface Directly with System Bus

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
COMP	S1	S0	Y	OPER = 0
L	L	L	A	H = all A inputs L
L	L	H	B	H = all B inputs L
L	H	L	A·B	Z
L	H	H	\overline{L}	L
H	L	L	\overline{A}	H = all A inputs L
H	L	H	\overline{B}	H = all B inputs L
H	H	L	$\overline{A \cdot B}$	Z
H	H	H	Z	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT	
I _{CCZ}	MAX	36	135	mA	
I _{CCL}	MAX	33	175	mA	
I _{OH}	Y	MAX	-2.6	-15	mA
	OPER = 0	MAX	-2.6	-2	mA
I _{OL}	Y	MAX	24	48	mA
	OPER = 0	MAX	24	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t _{pd}	A or B (COMP = "H")	Y inverting	MAX	14	12
t _{pd}	A or B (COMP = "L")	Y non-inverting	MAX	14	10
t _{pd}	S0 or S1	Y	MAX	33	13
t _{pd}	COMP	Y		18	13
t _{pd}	A or B	OPER = 0		37	14
t _{pd}	S0 to S1	OPER = 0		23	18
t _{en}	S0 to S1	Y		35	12
t _{fs}	COMP	Y	MAX	23	11
t _{en}				24	12
t _{fs}				21	9
t _{en}	S0	OPER = 0	MAX	20	12
t _{fs}				27	9
t _{en}	S1	OPER = 0	MAX	25	12
t _{fs}				19	9
t _{en}	COMP	OPER = 0	MAX	25	13
t _{fs}				20	9

UNIT: ns

10-BIT TRANSCEIVERS WITH 3-STATE OUTPUTS

FUNCTION TABLE

INPUTS		OPERATION
OEAB	OEBA	
L	H	A data to B bus
H	L	B data to A bus
H	H	Isolation
L	L	Latch A and B (A = B)

RECOMMENDED OPERATING CONDITIONS

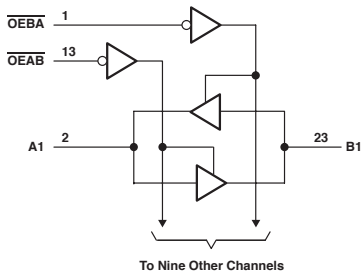
PARAMETER	MAX or MIN	ABT	LVC 3V	UNIT
I _{CC}	MAX	38	0.01	mA
I _{OH}	MAX	-32	-24	mA
I _{OL}	MAX	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVC 3V
t _{PLH}	A or B	B or A	MAX	5.2	6.4
t _{PHL}				4.9	6.4
t _{PZH}	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	B or A	MAX	5.9	7
t _{PZL}				6.9	7
t _{PHZ}	$\overline{\text{OEAB}}$ or $\overline{\text{OEBA}}$	B or A	MAX	7.5	5.9
t _{PLZ}				7.1	5.9

UNIT: ns

Logic Diagram

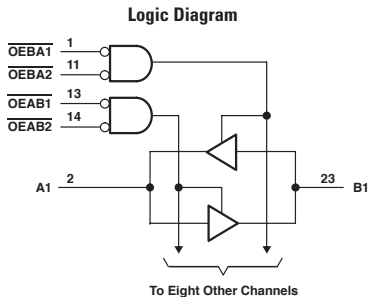


9-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

● 3-State Outputs

FUNCTION TABLE

INPUTS				OPERATION
OEAB1	OEAB2	OEBA1	OEBA2	
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	H	
H	X	L	L	B to A
X	H	L	L	
H	X	H	X	Isolation
H	X	X	H	
X	H	X	H	
X	H	X	H	
X	H	H	X	



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVC 3V	UNIT
I_{CC}	MAX	38	0.01	mA
I_{OH}	MAX	-32	-24	mA
I_{OL}	MAX	64	24	mA

SWITCHING CHARACTERISTICS

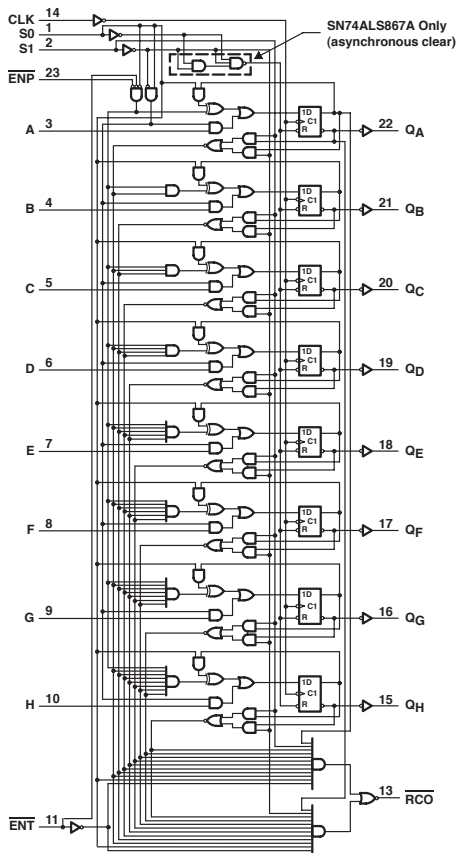
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVC 3V
t_{PLH}	A or B	B or A	MAX	5.7	6.1
t_{PHL}				3.9	6.1
t_{PZH}	\overline{OE}	A or B	MAX	5.5	7.2
t_{PZL}				5.4	7.2
t_{PHZ}	\overline{OE}	A or B	MAX	6.7	6.3
t_{PLZ}				6.9	6.3

UNIT: ns

8-BIT SYNCHRONOUS BIDIRECTIONAL COUNTER

- Fully Programmable with Synchronous Counting and Loading
- Asynchronous Clear
- Ripple-Carry Output for n-Bit Cascading

Logic Diagram



FUNCTION TABLE

S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I _{CC}	MAX	45	195	mA
I _{OH}	MAX	-0.4	-2	mA
I _{OL}	MAX	8	20	mA

SWITCHING CHARACTERISTICS

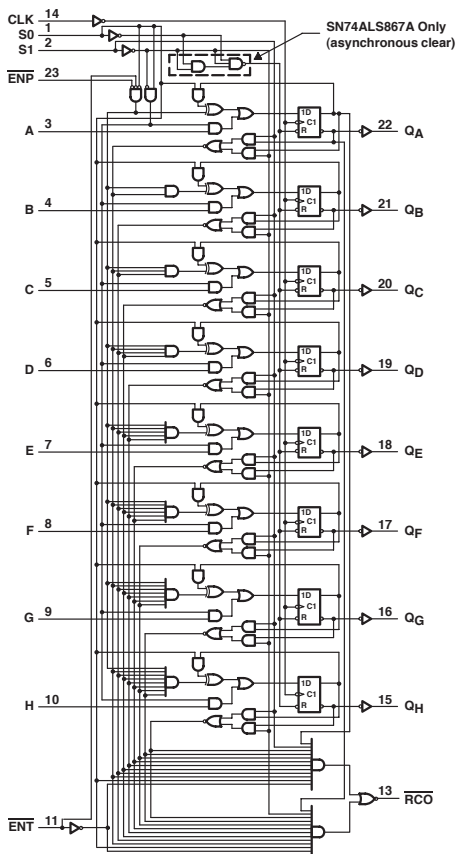
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
f _{max}			MIN	35	50
t _w	CLK (clock)		MIN	14	10
	S0 and S1 (clear)			10	10
t _{su}	Data input A-H		MIN	10	4
	\overline{ENP} or \overline{ENT}			15	8
	S0 low and S1 high (load)			12	10
	S0 and S1 low (clear)			-	10
	S0 high and S1 low (count down)			12	40
	S0 and S1 high (count up)			12	40
t _h	S0 high after S1 ' or S1 high after S0 '		MIN	3	-
	Data input A-H			0	0
t _{PLH}	CLK	\overline{RCO}	MAX	14	22
t _{PHL}				14	16
t _{PLH}	CLK	Any Q	MAX	16	11
t _{PHL}				16	15
t _{PLH}	\overline{ENT}	\overline{RCO}	MAX	14	10
t _{PHL}				9	17
t _{PLH}	\overline{ENP}	\overline{RCO}	MAX	-	14
t _{PHL}				-	17
t _{PHL}	S0, S1 (clear mode)	Any Q	MAX	26	-
t _{PLH}	S0 or S1 (count up/down)	\overline{RCO}	MAX	16	-
t _{PHL}				16	-
t _{PHL}	S0 or S1 (clear mode)	\overline{RCO}	MAX	16	21

 UNIT f_{max} : MHz other : ns

8-BIT SYNCHRONOUS BIDIRECTIONAL COUNTER

- Fully Programmable with Synchronous Counting and Loading
- Synchronous Clear
- Ripple-Carry Output for n-Bit Cascading

Logic Diagram



FUNCTION TABLE

S1	S0	FUNCTION
L	L	Clear
L	H	Count down
H	L	Load
H	H	Count up

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I _{CC}	MAX	45	195	mA
I _{OH}	MAX	-0.4	-2	mA
I _{OL}	MAX	8	20	mA

SWITCHING CHARACTERISTICS

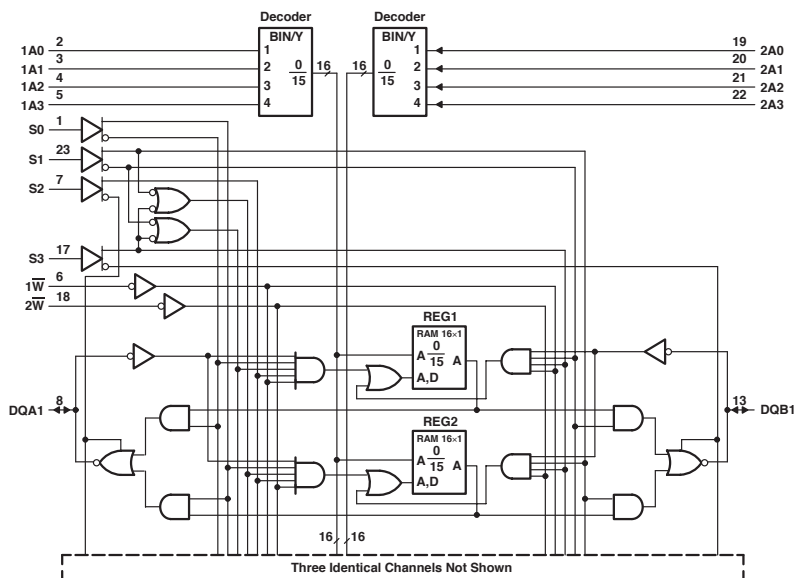
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
f _{max}			MIN	35	45
t _w	CLK		MIN	14	11
t _{su}	Data input A-H		MIN	10	5
	ENP or ENT			15	9
	S0 low and S1 high (load)			13	11
	S0 and S1 low (clear)			13	11
	S0 high and S1 low (count down)			13	50
	S0 and S1 high (count up)			13	50
t _h	S0 high after S1 ' or S1 high after S0 '		MIN	3	-
	Data input A-H			0	0
t _{PLH}	CLK	\overline{RCO}	MAX	14	35
t _{PHL}				14	18
t _{PLH}	CLK	Any Q	MAX	16	11
t _{PHL}				16	15
t _{PLH}	\overline{ENT}	\overline{RCO}	MAX	14	15
t _{PHL}				9	17
t _{PLH}	\overline{ENP}	\overline{RCO}	MAX	-	19
t _{PHL}				-	18
t _{PLH}	S1 (count up/down)	\overline{RCO}	MAX	15	-
t _{PHL}				15	-
t _{PLH}	S0 (clear/load)	\overline{RCO}	MAX	16	-
t _{PHL}				12	-

 UNIT f_{max} : MHz other : ns

DUAL 16-BY 4-BIT REGISTER FILES

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Each Register File Has Individual Write-Enabled Controls and Address Lines

Logic Diagram



FUNCTION TABLE

FILE SELECT			INPUT/OUTPUT		
S0	S1	FILE SEL	S2	S3	I/O SEL
L	L	1R to A, 1R to B	L	L	A out B A out, B out
H	L	2R to A, 1R to B			
L	H	1R to A, 2R to B			
H	H	2R to A, 2R to B			
L	L	A to 1R, 1R to B	H	L	A in B A in, B out
H	L	A to 2R, 1R to B			
L	H	A to 1R, 2R to B			
H	H	A to 2R, 2R to B			
L	L	1R to A, B to 1R	L	H	A out B A out, B in
H	L	2R to A, B to 1R			
L	H	1R to A, B to 2R			
H	H	2R to A, B to 2R			
L	L	B to 1R	H	H	A in Bin A in, B
H	L	A to 2R, B to 1R			
L	H	A to 1R, B to 2R			
H	H	B to 2R			

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I _{CC}	MAX	110	190	mA
I _{OL}	MAX	24	48	mA
I _{OH}	MAX	-2.6	-15	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t _w	write		MIN	12	12
t _{su}	Address before write ,		MIN	5	5
	Data before write '			15	15
	Select before write ,			12	12
t _h	Address before write ,		MIN	0	0
	Data before write '			0	0
	Select before write ,			12	12
t _{st(A)}	Any A	Any DQ	MAX	19	15
t _{st(S)}	S0	Any DQA	MAX	15	13
	S1	Any DQB		15	13
t _{st(S)}	S2	Any DQA	MAX	14	11
	S3	Any DQB		14	11
t _{en}	S2	Any DQA	MAX	17	12
	S3	Any DQB		17	12
t _{p-d}	\overline{W}	Any \overline{DQ}	MAX	23	19
	DA	DQB		26	22
	DQB	DQA		26	22

UNIT: ns

DUAL 4-BIT D-TYPE LATCHES

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Asynchronous Clear

FUNCTION TABLE

INPUTS				D	OUTPUT
OE	CLR	ENABLE LE			
L	L	X	X	L	L
L	H	H	H	H	H
L	H	H	L	L	L
L	H	L	X	X	Q ₀
H	X	X	X	X	Z

RECOMMENDED OPERATING CONDITIONS

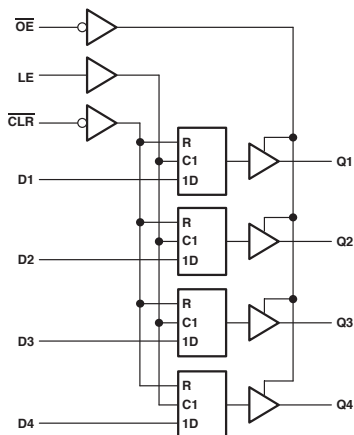
PARAMETER	MAX or MIN	ALS	AS	UNIT
I _{CC}	MAX	31	129	mA
I _{DH}	MAX	-2.6	-15	mA
I _{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t _w	CLR low		MIN	15	5
	LE high			10	5
				10	2
t _{bu}				7	4.5
t _h				14	9.5
t _{PLH}	D	Q	MAX	14	7.5
t _{PHL}				22	13
t _{PLH}	LE	Q	MAX	21	7.5
t _{PHL}				20	9
t _{PHL}	CLR	Q	MAX	20	9
t _{PZH}	OE	Q	MAX	18	6.5
t _{PZL}				18	10.5
t _{PHZ}	OE	Q	MAX	10	7.5
t _{PLZ}				15	7.5

UNIT: ns

Logic Diagram



DUAL 4-BIT D-TYPE EDGE-TRIGGERED FLIP-FLOPS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Asynchronous Clear

FUNCTION TABLE

INPUTS					OUTPUTS
OE	CLR	CLK	D	Q	
L	L	X	X	L	
L	H	↑	H	H	
L	H	↑	L	L	
L	H	L	X	Q ₀	
H	X	X	X	Z	

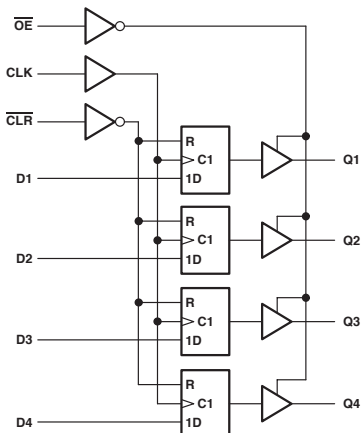
RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I _{CC}	MAX	32	160	mA
I _{DH}	MAX	-2.6	-15	mA
I _{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t _{max}			MIN	30	125
t _w	PRE or CLR low		MIN	10	2
	CLK "H"			16.5	3
	CLK "L"			16.5	4
t _{su}	Data		MIN	15	2
	PRE or CLR inactive			10	4
t _b			MIN	0	1
t _{PLH}	CLK	Q	MAX	14	8.5
t _{PHL}				14	10.5
t _{PHL}	CLR	Q	MAX	17	9.5
t _{PZH}	OE	Q	MAX	18	7
t _{PZL}				18	10.5
t _{PHZ}	OE	Q	MAX	10	6
t _{PLZ}				12	7.5

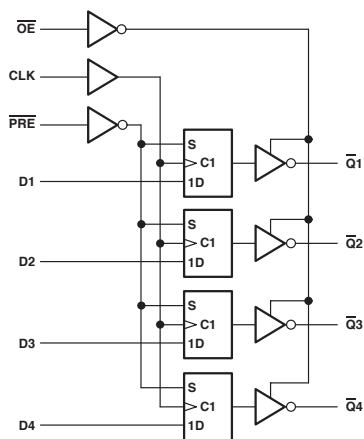
 UNIT f_{max} : MHz other : ns

Logic Diagram


DUAL 4-BIT D-TYPE FLIP-FLOPS

- 3-State Buffer-Type Outputs Drive Bus Lines Directly
- Bus-Structured Pinout
- Asynchronous Clear

Logic Diagram



FUNCTION TABLE
(each flip-flop)

INPUTS				OUTPUT
OE	PRE	CLK	D	Q
L	L	X	X	L
L	H	↑	H	L
L	H	↑	L	H
L	H	L	X	\bar{Q}_0
H	X	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I _{CC}	MAX	31	160	mA
I _{OH}	MAX	-2.6	-15	mA
I _{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

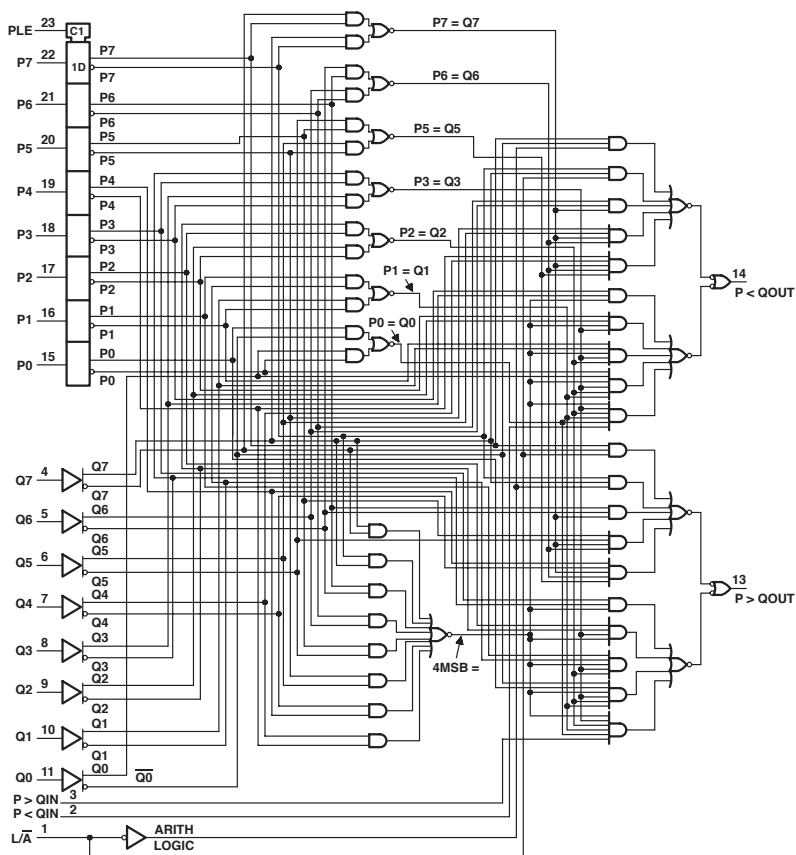
PARAMETER		INPUT	OUTPUT	MAX or MIN	ALS	AS
f _{max}				MIN	30	80
t _{sv}	$\overline{\text{PRE}}$ 'L'			MIN	10	4.5
	CLK 'H'				16.5	6.2
	CLK 'L'				16.5	6.2
t _{su}	Data			MIN	15	4.5
	$\overline{\text{PRE}}$ inactive				10	5
t _h				MIN	0	2
t _{PLH}		CLK	\bar{Q}	MAX	14	8.5
t _{PHL}					14	10.5
t _{PHL}		$\overline{\text{PRE}}$	\bar{Q}	MAX	19	9.5
t _{PZH}		$\overline{\text{OE}}$	\bar{Q}	MAX	18	7
t _{PZL}					18	11
t _{PHZ}		$\overline{\text{OE}}$	\bar{Q}	MAX	10	7
t _{PLZ}					13	7

UNIT f_{max}: MHz, other: ns

8-BIT MAGNITUDE COMPARATOR

- SN54AS885 Latchable P-Input Ports with Power-Up Clear
- Choice of Logical or Arithmetic (Two's Complement) Comparison
- Data and PLE Inputs Utilize pnp Input Transistors to Reduce dc Loading Effects
- Cascadable to n Bits While Maintaining High Performance

Logic Diagram



FUNCTION TABLE

COMPARISON	INPUTS				OUTPUTS	
	L/A	DATA P0-P7, Q0-Q7	P > QIN	P < QIN	P > QOUT	P < QOUT
Logical	H	P > Q	X	X	H	L
Logical	H	P < Q	X	X	L	H
Logical†	H	P = Q	H or L	H or L	H or L	H or L
Arithmetic	L	P AG Q	X	X	H	L
Arithmetic	L	Q AG P	X	X	L	H
Arithmetic†	L	P = Q	H or L	H or L	H or L	H or L

† In these cases, P > QOUT follows P > QIN and P < QOUT follows P < QIN.
AG = arithmetically greater than

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AS	UNIT
I _{CC}	MAX	210	mA
I _{DH}	MAX	-2	mA
I _{OL}	MAX	20	mA

SWITCHING CHARACTERISTICS

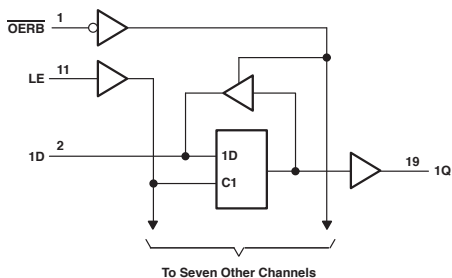
PARAMETER	INPUT	OUTPUT	MAX or MIN	AS
t _{su}	Data before PLE ,		MIN	2
t _h	Data after PLE ,			4
t _{PLH}	L / \bar{A}	P < QOUT, P > QOUT	MAX	13
t _{PHL}				13
t _{PLH}	P < QIN, P > QIN	P < QOUT, P > QOUT	MAX	8
t _{PHL}				8
t _{PLH}	Any P or Q data input	P < QOUT, P > QOUT	MAX	17.5
t _{PHL}				15

UNIT: ns

8-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- Bus-Structured Pinout

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I _{CC}		MAX	70	mA
I _{OH}	Q	MAX	-2.6	mA
	D		-0.4	mA
I _{OL}	Q	MAX	24	mA
	D		8	mA

SWITCHING CHARACTERISTICS

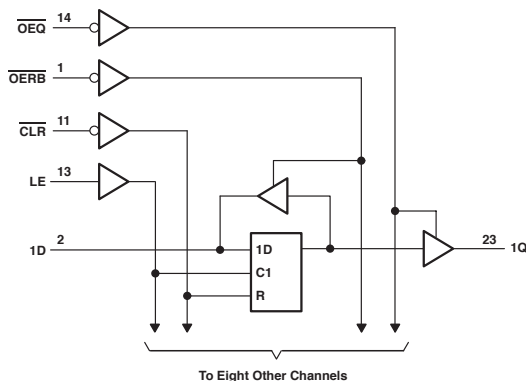
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t _w	LE high		MIN	10
t _{su}	Data before LE ,		MIN	10
	Data before $\overline{\text{OERB}}$			10
t _h	Data after LE ,		MIN	5
t _{PLH}	D	Q	MAX	17
t _{PHL}				24
t _{PLH}	LE	Q	MAX	26
t _{PHL}				26
t _{en}	$\overline{\text{OERB}}$	D	MAX	21
			MAX	19

UNIT: ns

9-BIT D-TYPE TRANSPARENT

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- Bus-Structured Pinout
- Designed with Nine Bits for Parity Applications

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I _{CC}		MAX	80	mA
I _{OH}	Q	MAX	-2.6	mA
	D		-0.4	mA
I _{OL}	Q	MAX	24	mA
	D		8	mA

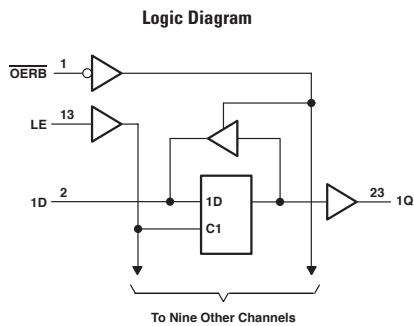
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t _w	C "H"		MIN	10
	CLR "L"			10
t _{su}	Data before LE ,		MIN	10
	Data before OERB ,			10
t _h	Data after LE ,		MIN	5
t _{PLH}	D	Q	MAX	14
t _{PHL}				16
t _{PLH}	LE	Q	MAX	20
t _{PHL}				25
t _{PLH}	CLR	Q	MAX	20
t _{PHL}		D		26
t _{en}	OERB	D	MAX	21
t _{dis}		14		
t _{en}	OEQ	Q	MAX	18
t _{dis}		14		

UNIT:ns

10-BIT D-TYPE TRANSPARENT READ-BACK LATCHES

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- Bus-Structured Pinout



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I _{CC}		MAX	82	mA
I _{OH}	Q	MAX	-2.6	mA
	D		-0.4	mA
I _{OL}	Q	MAX	24	mA
	D		8	mA

SWITCHING CHARACTERISTICS

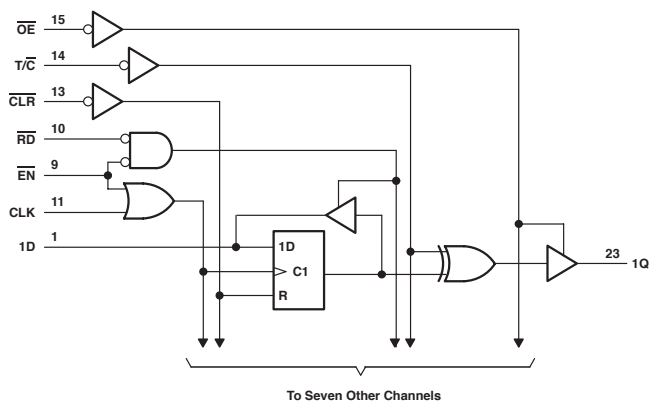
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t _w	C "H"		MIN	10
t _{su}	Data before LE ,		MIN	10
	Data before $\overline{\text{OERB}}$,			10
t _h	Data after LE ,		MIN	5
t _{PLH}	D	Q	MAX	14
t _{PHL}				18
t _{PLH}	LE	Q	MAX	21
t _{PHL}				27
t _{on}	$\overline{\text{OERB}}$	D	MAX	21
t _{ofs}				16

UNIT:ns

8-BIT D-TYPE EDGE-TRIGGERED READ-BACK LATCHES

- 3-State I/O-Type Read-Back Inputs
- True Logic Outputs
- T/C Determines True or Complementary Data at Q Outputs

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	ALS	UNIT
I _{CC}		MAX	85	mA
I _{OL}	Q	MAX	24	mA
	D		8	mA
I _{OH}	Q	MAX	-2.6	mA
	D		-0.4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t _w	CLR low		MIN	10
	CLK low			14.5
	CLK high			14.5
t _{su}	Data before CLK *		MIN	15
	EN low before CLK *			10
	CLK high before EN * ^{†1}			15
	CLR high (inactive) before CLK *			10
t _h	Data after CLK *		MIN	0
	EN low after CLK *			5
	RD high after CLK * ^{†2}			5
t _{PLH}	CLK (T/C = H or L)	Q	MAX	28
t _{PHL}				28
t _{PLH}	CLR (T/C = L)	Q	MAX	27
t _{PHL}				23
t _{PLH}	CLR (T/C = H)	Q	MAX	23
t _{PHL}				23
t _{PLH}	T / C	Q	MAX	23
t _{PHL}				23
t _{PHL}	CLR	D	MAX	30
t _{en} ^{†3}	RD	D	MAX	16
t _{dis} ^{†4}				19
t _{en} ^{†3}	EN	D	MAX	16
t _{dis} ^{†4}				19
t _{en} ^{†3}	OE	Q	MAX	15
t _{dis} ^{†4}				10

UNIT: ns

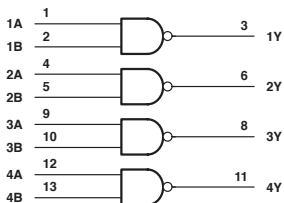
^{†1} This setup time ensures that EN will not false clock the data register.^{†2} This hold time ensures that there will be no conflict on the input data bus.^{†3} = t_{PZL} OR t_{PZL}^{†4} = t_{PHZ} OR t_{PLZ}

1000

QUAD 2-INPUT NAND BUFFERS/DRIVERS

- Buffer Version of SN74ALS00A
- Driver Version of SN74AS00
- High Capacitive-Drive Capability

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
H	H	L
L	X	H
X	L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	7.8	19	mA
I_{OH}	MAX	-2.6	-48	mA
I_{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
				t_{PLH}	A or B
t_{PHL}				7	4

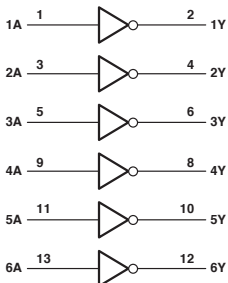
UNIT: ns

1004

HEX INVERTING DRIVERS

- Driver Version of SN74ALS04B and SN74AS04
- High Capacitive-Drive Capability

Logic Diagram



FUNCTION TABLE

INPUT	OUTPUT
A	Y
H	L
L	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	12	27	mA
I_{OH}	MAX	-15	-48	mA
I_{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t_{PLH}	A or B	Y	MAX	7	4
t_{PHL}				6	4

UNIT: ns

1005

HEX INVERTING BUFFER GATES WITH OPEN-COLLECTOR OUTPUTS

- Buffer Version of SN74ALS05A

FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

RECOMMENDED OPERATING CONDITIONS

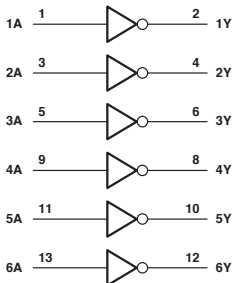
PARAMETER	MAX or MIN	ALS	UNIT
I_{CC}	MAX	12	mA
V_{OH}	MAX	5.5	V
I_{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A	Y	MAX	30
t_{PHL}				10

UNIT: ns

Logic Diagram



1008

QUADRUPLE 2-INPUT POSITIVE-AND BUFFERS/DRIVERS

- Buffer Version of SN74ALS08
- Driver Version of SN74AS08

FUNCTION TABLE

INPUTS		OUTPUT Y
A	B	
H	H	H
L	X	L
X	L	L

RECOMMENDED OPERATING CONDITIONS

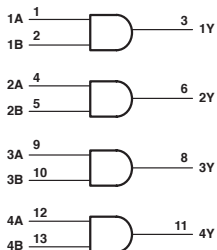
PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	9.3	22	mA
I_{OH}	MAX	-2.6	-48	mA
I_{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t_{PLH}	A or B	Y	MAX	9	6
t_{PHL}				9	6

UNIT: ns

Logic Diagram

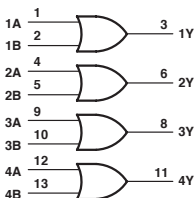


1032

QUAD 2-INPUT OR BUFFERS/DRIVERS

- $Y = A + B$
- Driver Version of SN74AS32
- High Capacitive-Drive Capability

Logic Diagram



FUNCTION TABLE

(each gate)

INPUTS		OUTPUT
A	B	Y
H	X	H
X	H	H
L	L	L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	10.6	24	mA
I_{OH}	MAX	-2.6	-48	mA
I_{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t_{PLH}	A or B	Y	MAX	9	6.3
t_{PHL}	\bar{A} or B	Y	MAX	12	6.3

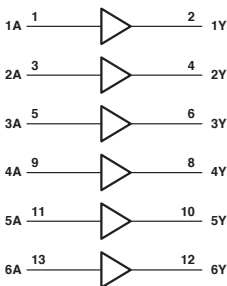
UNIT: ns

1034

HEX DRIVERS

- SN74AS1034A Offer High Capacitive-Drive Capability
- Noninverting Drivers

Logic Diagram



FUNCTION TABLE

INPUT	OUTPUT
A	Y
H	H
L	L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	14	35	mA
I_{OH}	MAX	-15	-48	mA
I_{OL}	MAX	24	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t_{PLH}	A	Y	MAX	8	6
t_{PHL}				8	6

UNIT: ns

1035

HEX BUFFERS WITH OPEN-COLLECTOR OUTPUTS

- Noninverting Buffers with Open-Collector Outputs

FUNCTION TABLE

INPUT A	OUTPUT Y
H	H
L	L

RECOMMENDED OPERATING CONDITIONS

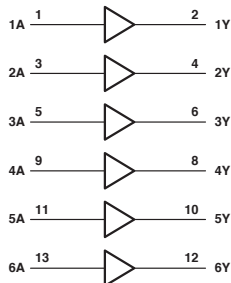
PARAMETER	MAX or MIN	ALS	UNIT
I _{CC}	MAX	14	mA
V _{OH}	MAX	5.5	V
I _{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t _{PLH}	A	Y	MAX	30
t _{PHL}				12

UNIT: ns

Logic Diagram



1240

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

- Low-Power Versions of SN74ALS240A
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers

RECOMMENDED OPERATING CONDITIONS

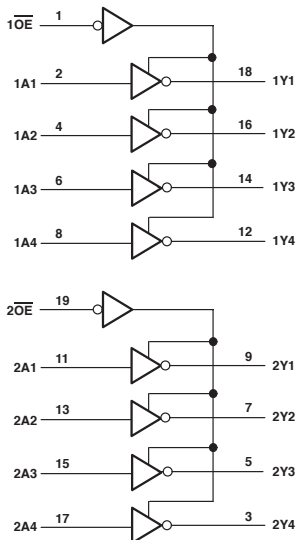
PARAMETER	MAX or MIN	ALS	UNIT
I _{CCZ}	MAX	13	mA
I _{CCL}	MAX	14	mA
I _{OH}	MAX	-15	mA
I _{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t _{PLH}	\bar{A}	Y	MAX	13
t _{PHL}				13
t _{PZH}	\overline{OE}	Y	MAX	20
t _{PZL}				22
t _{PHZ}	\overline{OE}	Y	MAX	10
t _{PLZ}				13

UNIT: ns

Logic Diagram



1244

OCTAL BUFFERS/LINE DRIVERS/LINE RECEIVERS

- 3-State Outputs Drive Bus Lines or Buffer Memory Address Registers
- pnp Inputs Reduce dc Loading
- Low-Power Versions of SN74ALS244 Series

RECOMMENDED OPERATING CONDITIONS

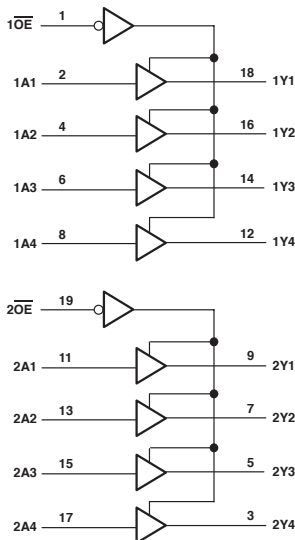
PARAMETER	MAX or MIN	ALS	UNIT
I_{CCZ}	MAX	20	mA
I_{CCL}	MAX	17	mA
I_{OH}	MAX	-15	mA
I_{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A	Y	MAX	14
t_{PHL}	A	Y	MAX	14
t_{PZH}	\overline{OE}	Y	MAX	22
t_{PZL}	\overline{OE}	Y	MAX	22
t_{PHZ}	\overline{OE}	Y	MAX	13
t_{PLZ}	\overline{OE}	Y	MAX	16

UNIT: ns

Logic Diagram



1245

OCTAL BUS TRANSCEIVERS

- Low-Power Versions of 4ALS245 Series

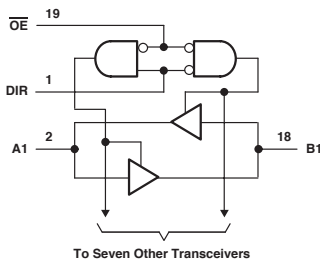
FUNCTION TABLE

CONTROL INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I_{CCZ}	MAX	36	mA
I_{CCL}	MAX	33	mA
I_{OH}	MAX	-15	mA
I_{OL}	MAX	16	mA

Logic Diagram



SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A or B	B or A	MAX	13
t_{PHL}	A or B	B or A	MAX	13
t_{PZH}	\overline{OE}	A or B	MAX	25
t_{PZL}	\overline{OE}	A or B	MAX	25
t_{PHZ}	\overline{OE}	A or B	MAX	12
t_{PLZ}	\overline{OE}	A or B	MAX	18

UNIT: ns

1640

OCTAL BUS TRANSCEIVERS

- Lower-Power Versions of SN74ALS640B
- Inverting Logic
- 3-State Outputs

FUNCTION TABLE

CONTROL INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	\bar{A} data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

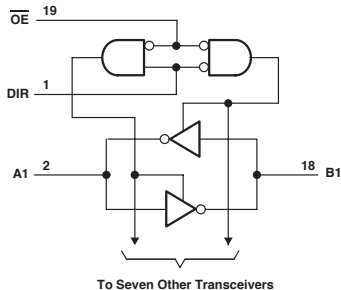
PARAMETER	MAX or MIN	ALS	UNIT
I _{CC}	MAX	32	mA
I _{OH}	MAX	-15	mA
I _{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t _{PLH}	A or B	B or A	MAX	15
				10
t _{PZH}	\overline{OE}	A or B	MAX	20
t _{PZL}				22
t _{PHZ}	\overline{OE}	A or B	MAX	10
t _{PLZ}				13

UNIT: ns

Logic Diagram



1645

OCTAL BUS TRANSCEIVERS

- Lower-Power Versions of SN74ALS645A
- 3-State Outputs

FUNCTION TABLE

CONTROL INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

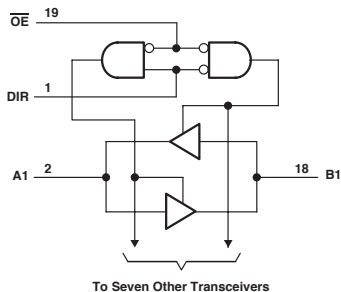
PARAMETER	MAX or MIN	ALS	UNIT
I _{CC}	MAX	38	mA
I _{OH}	MAX	-15	mA
I _{OL}	MAX	16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t _{PLH}	A or B	B or A	MAX	13
				13
t _{PZH}	\overline{OE}	A or B	MAX	25
t _{PZL}				25
t _{PHZ}	\overline{OE}	A or B	MAX	12
t _{PLZ}				18

UNIT: ns

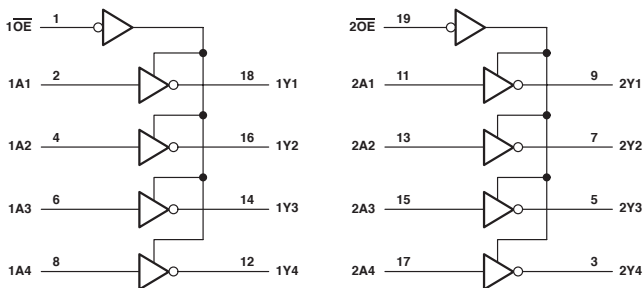
Logic Diagram



OCTAL BUFFERS AND LINE DRIVERS / MOS DRIVERS WITH 3-STATE OUTPUTS

- I/O Ports Have 25- Ω Series Resistors, So No External Resistors Are Required (SN74ALS2240, SN74ABT2240A)
- Output Ports Have Equivalent 33- Ω Series Resistors, So No External Resistors Are Required (SN74BCT2240)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	BCT	ABT	UNIT
I_{CCZ}	MAX	20	8	0.25	mA
I_{CC1}	MAX	23	76	30	mA
I_{OH}	MAX	-15	-12	-32	mA
I_{OL}	MAX	15	12	12	mA

SWITCHING CHARACTERISTICS

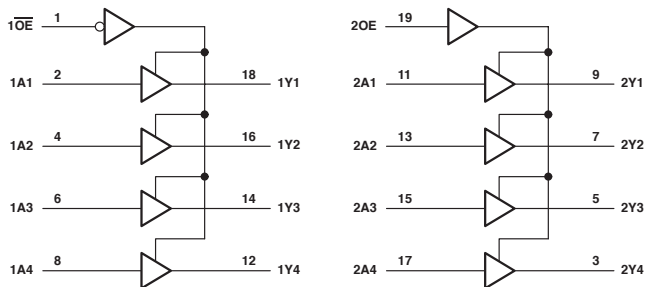
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	BCT	ABT
t_{PLH}	A	Y	MAX	10	5.7	4.8
t_{PHL}				10	4.4	5.4
t_{PZH}	\overline{OE}	Y	MAX	17	9.3	5.2
t_{PZL}				20	12.4	6.8
t_{PHZ}	\overline{OE}	Y	MAX	10	8.7	6.4
t_{PLZ}				15	10.6	6.2

UNIT: ns

OCTAL BUFFERS AND LINE DRIVERS / MOS DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25- Ω Series Resistors, So No External Resistors Are Required (SN74ABT2241A)
- Output Ports Have Equivalent 33- Ω Series Resistors, So No External Resistors Are Required (SN74BCT2241)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	ABT	UNIT
I_{CCZ}	MAX	9	0.25	mA
I_{CCL}	MAX	76	30	mA
I_{OH}	MAX	-12	-32	mA
I_{OL}	MAX	12	12	mA

SWITCHING CHARACTERISTICS

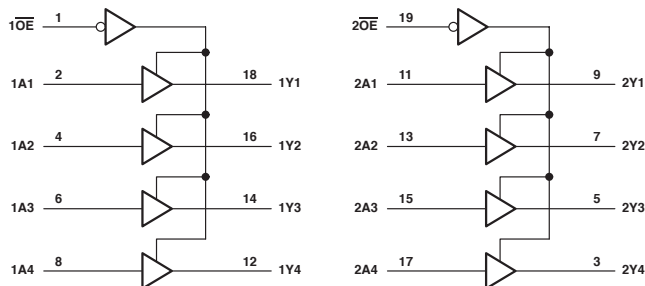
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT
t_{PLH}	A	Y	MAX	4.9	4.7
t_{PHL}				6.9	5.6
t_{PZH}	$\overline{1OE}$	Y	MAX	8.9	5.8
t_{PZL}				10.3	8.4
t_{PHZ}	$\overline{1OE}$	Y	MAX	8.7	6.6
t_{PLZ}				11.3	6.4
t_{PZH}	20E	Y	MAX	8.9	5.8
t_{PZL}				10.3	8.4
t_{PHZ}	20E	Y	MAX	8.7	6.6
t_{PLZ}				11.3	6.4

UNIT: ns

OCTAL BUFFERS AND LINE DRIVERS / MOS DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT2244A)
- Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2244)
- Output Ports Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required (SN74LVC2244A)

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
OE	A	Y
H	X	Z
L	L	L
L	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	ABT	LVC 3V	UNIT
I _{CCZ}	MAX	23	10	0.25	0.01	mA
I _{CCL}	MAX	22	77	30	0.01	mA
I _{OH}	MAX	-15	-12	-32	-12	mA
I _{OL}	MAX	15	12	12	12	mA

SWITCHING CHARACTERISTICS

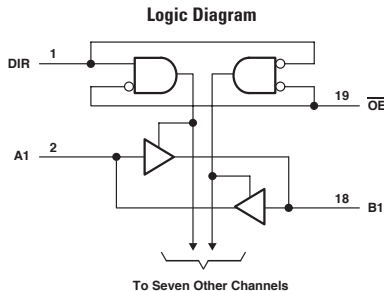
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT	ABT	LVC 3V
t _{PLH}	A	Y	MAX	16	4.9	4.7	5.5
t _{PHL}				17	6.7	5.6	5.5
t _{PZH}	\overline{OE}	Y	MAX	17	8.7	5.5	7.1
t _{PZL}				14	10.4	8.3	7.1
t _{PHZ}	\overline{OE}	Y	MAX	9	7.8	6.6	6.8
t _{PLZ}				9	9.8	5.8	6.8

UNIT: ns

2245

OCTAL TRANSCEIVER AND LINE/ MOS DRIVERS WITH 3-STATE OUTPUTS

- B Port Has Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2245)
- B-Port Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT2245)
- Outputs Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABTR2245)
- All Outputs Have Equivalent 26-Ω Series Resistors, So No External Resistors Are Required (SN74LVCR2245)
- B-Port Outputs Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required (SN74LVTH2245)



FUNCTION TABLE

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	ABT	ABTR	LVCR 3V	LVTH 3V	UNIT
I _{CCZ}	MAX	15	0.25	0.25	0.01	0.19	mA
I _{CCL}	MAX	100	32	32	0.01	5	mA
I _{OH} (A port)	MAX	-3	-32	-12	-12	-32	mA
I _{OH} (B port)	MAX	-12	-12	-12	-12	-12	mA
I _{OL} (A port)	MAX	24	64	12	12	64	mA
I _{OL} (B port)	MAX	12	12	12	12	12	mA

SWITCHING CHARACTERISTICS

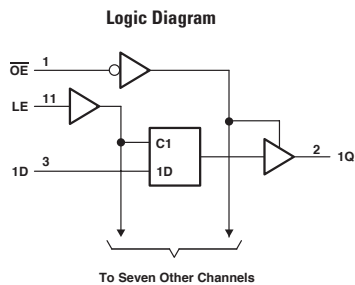
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT	ABTR	LVCR 3V	LVTH 3V
t _{PLH}	A	B	MAX	5.8	3.8	3.8	6.3	4.4
				7.8	4.5	4.5	6.3	4.4
t _{PHL}	B	A	MAX	7	3.6	3.8	6.3	3.5
				7.7	4	4.5	6.3	3.5
t _{PZH}	OE	B	MAX	9.9	6.1	6.1	8.2	6.2
				12.2	6.3	6.3	8.2	6.2
t _{PHZ}	OE	B	MAX	8.2	5.3	5.3	7.8	5.9
				9.2	4.8	4.8	7.8	5.4
t _{PZH}	OE	A	MAX	11.1	5.5	6.1	8.2	5.5
				11.4	5.7	6.3	8.2	5.5
t _{PHZ}	OE	A	MAX	9.4	5.6	5.3	7.8	5.9
				7.6	4.5	4.8	7.8	5

UNIT: ns

2373

25-Ω OCTAL TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

- 3-State True Outputs with 25-Ω Sink Resistors
- Full Parallel Access for Loading
- Buffered Control Inputs



FUNCTION TABLE

(each latch)

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	F	UNIT
I _{CC}	MAX	66	mA
I _{OH}	MAX	-3	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

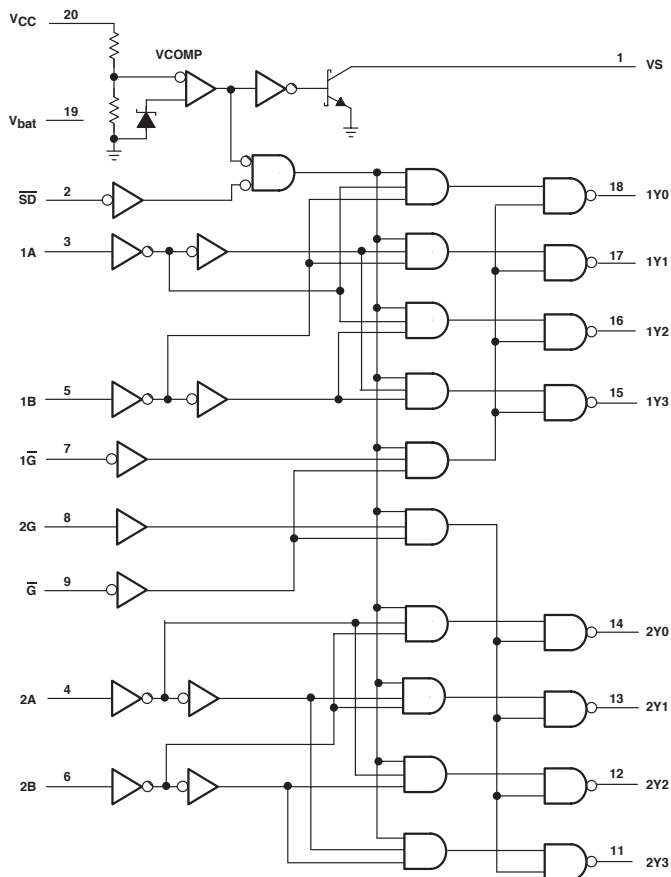
PARAMETER	INPUT	OUTPUT	MAX or MIN	F
t _w	LE high		MIN	6
t _{bu}	Data before LE =		MIN	2
t _b	Data after LE =		MIN	6
t _{PLH}	D	Q	MAX	9
t _{PHL}				7
t _{PLH}	LE	Q	MAX	13
t _{PHL}				8
t _{PZH}	\overline{OE}	Q	MAX	12
t _{PZL}				9.5
t _{PHZ}	\overline{OE}	Q	MAX	7.5
t _{PLZ}				6

UNIT:ns

MEMORY DECODER WITH ON-CHIP V_{CC} MONITOR

- Built-In Supply-Voltage Monitor for V_{CC}
- Separate Enable Inputs for Easy Cascading

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUTS			
CONTROL			SELECT		1Y0	1Y1	1Y2	1Y3
\overline{G}	1G	SD	1B	1A				
H	X	X	X	X	H	H	H	H
X	H	X	X	X	H	H	H	H
X	X	L	X	X	H	H	H	H
L	L	H	L	L	L	H	H	H
L	L	H	L	H	L	L	H	H
L	L	H	H	L	H	H	L	H
L	L	H	H	H	H	H	H	L

INPUTS						OUTPUTS			
CONTROL			SELECT			2Y0	2Y1	2Y2	2Y3
\overline{G}	2G	SD	2B	2A					
H	X	X	X	X	H	H	H	H	
X	H	X	X	X	H	H	H	H	
X	X	L	X	X	H	H	H	H	
L	H	H	L	L	L	H	H	H	
L	H	H	L	H	H	L	H	H	
L	H	H	H	L	H	H	L	H	
L	H	H	H	H	H	H	H	L	

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
I_{CC}	MAX	3	mA
I_{OH}	MAX	-0.4	mA
I_{bat} (Output low)	MAX	3	mA
I_{OL}	MAX	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
t_{PLH}	A or B	Any Y	MAX	12
t_{PHL}				12
t_{PLH}	Any \overline{G}	Any Y	MAX	10
t_{PHL}				11
t_{PLH}	\overline{SD}	Any Y	MAX	12
t_{PHL}				12
t_{PLH}	V_{CC}	Any Y	MAX	250
t_{PHL}				250
t_{PLH}	V_{CC}	VS	MAX	250
t_{PHL}				250

UNIT: ns

2541

OCTAL LINE DRIVERS/MOS DRIVERS WITH 3-STATE OUTPUTS

- Outputs Have 25-Ω Series Resistor So No External Resistors Are Required

RECOMMENDED OPERATING CONDITIONS

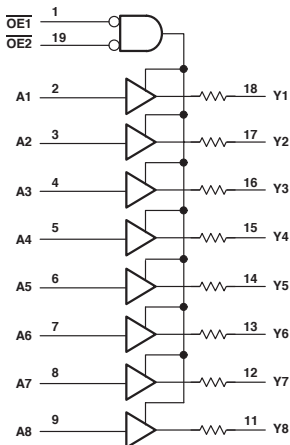
PARAMETER	MAX or MIN	ALS	UNIT
I _{CCZ}	MAX	22	mA
I _{CCL}	MAX	25	mA
I _{OH}	MAX	-0.4	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t _{PLH}	A	Y	MAX	15
t _{PHL}				12
t _{PZH}	\overline{OE}	Y	MAX	15
t _{PZL}				20
t _{PHZ}	\overline{OE}	Y	MAX	10
t _{PLZ}				12

UNIT: ns

Logic Diagram



All output resistors are 25 Ω.

2827

10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT2827)
- Output Ports Have Equivalent 25-Ω Resistors; No External Resistors Are Required (SN74BCT2827C)

RECOMMENDED OPERATING CONDITIONS

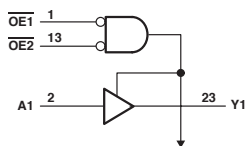
PARAMETER	MAX or MIN	SN74 BCT	ABT	UNIT
I _{CCZ}	MAX	6	0.25	mA
I _{CCL}	MAX	40	40	mA
I _{OH}	MAX	-1	-12	mA
I _{OL}	MAX	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT
t _{PLH}	A	Y	MAX	6	5.5
t _{PHL}				7.8	5.1
t _{PZH}	\overline{OE}	Y	MAX	10.7	6.7
t _{PZL}				12.9	7.8
t _{PHZ}	\overline{OE}	Y	MAX	13	7.2
t _{PLZ}				10	7.5

UNIT: ns

Logic Diagram



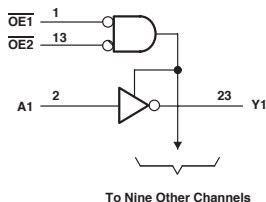
To Nine Other Channels

2828

10-BIT BUS/MOS MEMORY DRIVERS WITH 3-STATE INVERTING OUTPUTS

- Output Ports Have Equivalent 33-Ω Series Resistors, So No External Resistors Are Required (SN74BCT2828)

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
I _{CCZ}	MAX	6	mA
I _{CCL}	MAX	40	mA
I _{DH}	MAX	-1	mA
I _{DL}	MAX	12	mA

SWITCHING CHARACTERISTICS

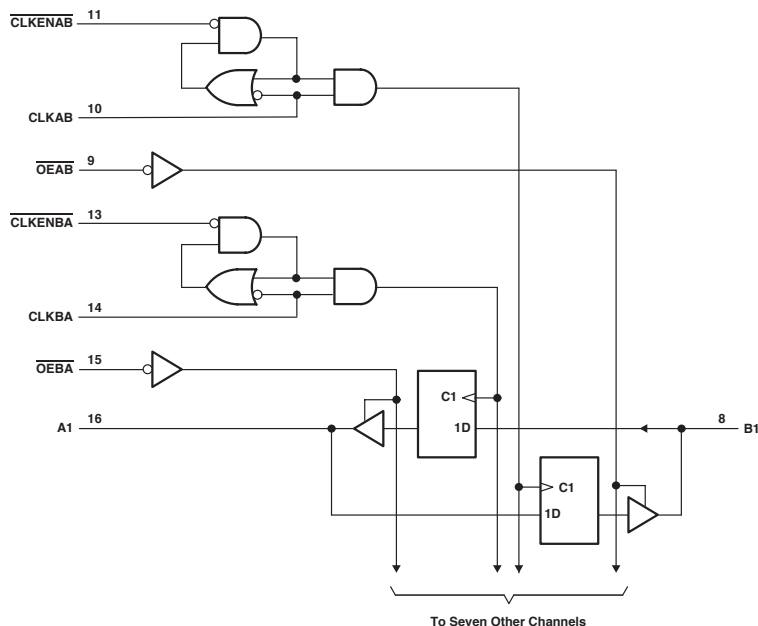
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
t _{PLH}	A	Y	MAX	6.6
t _{PHL}				5
t _{PZH}	\overline{OE}	Y	MAX	9
t _{PZL}				11.5
t _{PHZ}	\overline{OE}	Y	MAX	10.8
t _{PLZ}				8.7

UNIT: ns

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Two 8-Bit Back-to-Back Registers Store Data Flowing in Both Directions
- Noninverting Outputs
- 3-State Outputs

Logic Diagram



FUNCTION TABLE†

INPUTS				OUTPUT B
CLKENAB	CLKAB	OEAB	A	
H	X	L	X	B ₀
L	↑	L	L	L
L	↑	L	H	H
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	SN74 BCT	ABT	LVC 3V	LVT 3V	UNIT
I _{CC}		MAX	55	35	0.01	5	mA
I _{OH}	A	MAX	-3	-32	-24	-32	mA
	B		-15	-32	-24	-32	mA
I _{OL}	A	MAX	24	64	24	64	mA
	B		64	64	24	64	mA

SWITCHING CHARACTERISTICS

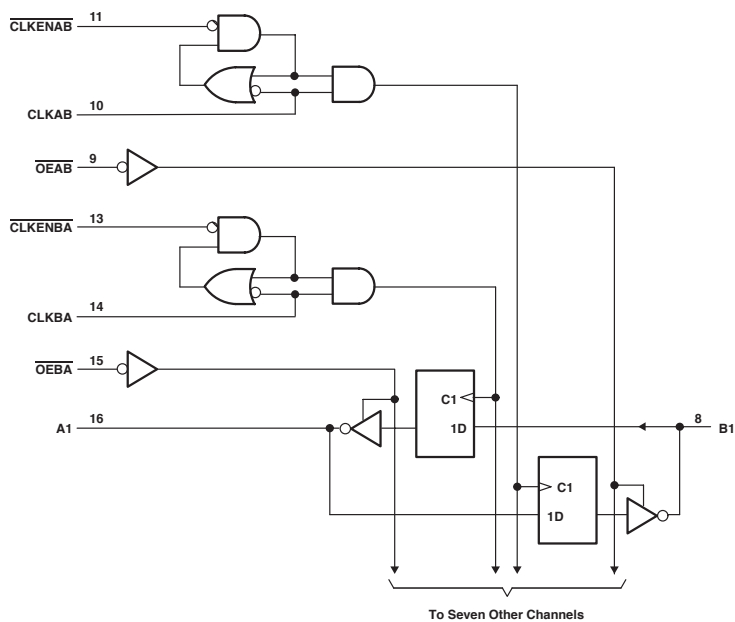
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABT	LVC 3V	LVT 3V
f _{max}			MIN	125	150	150	150
t _w	CLK "H"		MIN	4	3.3	3.3	3.3
	CLK "L"			4	3.3	3.3	3.3
t _{su}	A or B High		MIN	2.5	2.5	1.3	1.5
	A or B Low			2.5	2.5	1.3	1.5
	CLKENAB or CLKENBA High			2	3	1.1	1.5
	CLKENAB or CLKENBA Low			2	3	1.1	1.9
t _h	A or B		MIN	1.5	1.5	1.1	1
	CLKENAB or CLKENBA			2.5	2	1.1	1.2
t _{PLH}	CLKBA	A, B	MAX	9	5.9	8.2	4.6
t _{PHL}	CLKAB			10.5	6.3	8.2	4.6
t _{PLZH}	OEBA	A, B	MAX	8.2	5.6	7.8	4.6
t _{PLZL}	OEAB			12.9	6.6	7.8	4.6
t _{PHZH}	OEBA	A, B	MAX	8.4	6.4	7.8	5.4
t _{PHZL}	OEAB			7	6.2	7.8	5.1

UNIT f_{max} : MHz other : ns

OCTAL BUS TRANSCEIVERS AND REGISTERS

- Two 8-Bit, Back-to-Back Registers Store Data Flowing in Both Directions
- Inverting Outputs
- 3-State Outputs

Logic Diagram



FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	CLKAB	OEAB	A	B
H	↑	L	X	A ₀
L	↑	L	L	H
L	↑	L	H	L
X	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses OEBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	SN74 BCT	UNIT
I _{CC}		MAX	55	mA
I _{OH}	A	MAX	-3	mA
	B		-15	mA
I _{OL}	A	MAX	24	mA
	B		64	mA

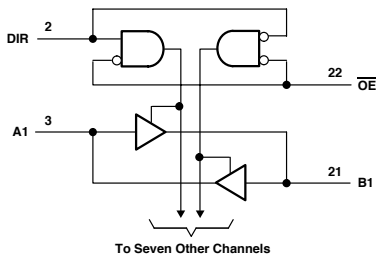
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
f _{max}			MIN	110
t _w	CLK "H"		MIN	4.5
	CLK "L"			4.5
t _{su}	A or B High		MIN	2.5
	A or B Low			2.5
	CLKENAB or CLKENBA High			2
	CLKENAB or CLKENBA Low			2
t _h	A or B		MIN	1.5
	CLKENAB or CLKENBA			2
t _{PLH}	CLKBA	A, B	MAX	9.5
t _{PHL}	CLKAB			10.2
t _{PZH}	OEBA	A, B	MAX	8.8
t _{PZL}	OEAB			14
t _{PHZ}	OEBA	A, B	MAX	9.1
t _{PLZ}	OEAB			7.6

UNIT f_{max} : MHz other : ns

OCTAL BUS TRANSCEIVER WITH ADJUSTABLE OUTPUT VOLTAGE AND 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	A bus Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER		MAX or MIN	V _{CCA} (V)	V _{CCB} (V)	LVCC	UNIT	
I _{CCA}	B to A	MAX	3.6	OPEN	0.05	mA	
				3.6	0.05	mA	
				5.5	0.05	mA	
I _{CCB}	A to B	MAX	3.6	3.6	0.05	mA	
				5.5	0.08	mA	
I _{OHA}	MAX		2.7	3	-12	mA	
			3.3		-24	mA	
I _{OHB}	MAX		2.7	3.3	-12	mA	
			3.3		3	-24	mA
I _{OLA}	MAX		2.7	3	12	mA	
			3.3		24	mA	
I _{OLB}	MAX		2.7	3.3	12	mA	
			3.3		3	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCC	
				V _{CCA} = 2.5V V _{CCB} = 3.3V	V _{CCA} = 3.6V V _{CCB} = 5V
t _{PLH}	A	B	MAX	9.4	6
t _{PHL}				9.1	5.3
t _{PLH}	B	A	MAX	11.2	5.8
t _{PHL}				9.9	7
t _{PZL}	OE	A	MAX	14.5	9.2
t _{PZH}				12.9	9.5
t _{PZL}	OE	B	MAX	13	8.1
t _{PZH}				12.8	8.4
t _{PLZ}	OE	A	MAX	7.1	7
t _{PHZ}				6.9	7.8
t _{PLZ}	OE	B	MAX	8.8	7.3
t _{PHZ}				8.9	7

UNIT: ns

4002

DUAL 4-INPUT POSITIVE-NOR GATES

$$\bullet Y = \overline{A + B + C + D}$$

FUNCTION TABLE

INPUTS				OUTPUT
A	B	C	D	Y
L	L	L	L	H
H	X	X	X	L
X	H	X	X	L
X	X	H	X	L
X	X	X	H	L

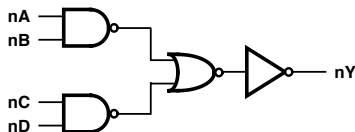
NOTES:

H = High Voltage Level

L = Low Voltage Level

X = Irrelevant

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	UNIT
I_{CC}	MAX	0.02	0.04	mA
I_{OH}	MAX	-4	-4	mA
I_{OL}	MAX	4	4	mA

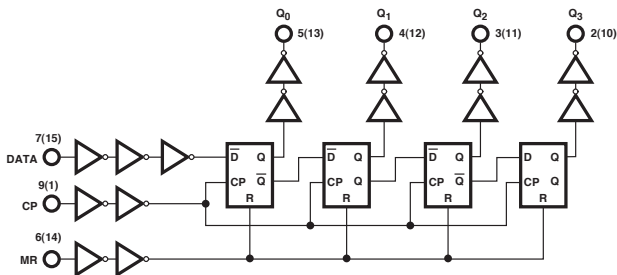
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC
t_{PLH}	A, B, C, D	Y	MAX	28	30
t_{PHL}			MAX	28	30

UNIT:ns

DUAL 4-STAGE STATIC SHIFT REGISTER

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT			
CP	D	R	Q ₀	Q ₁	Q ₂	Q ₃
↑	I	L	L	q ₀	q ₁	q ₂
↑	h	L	H	q ₀	q ₁	q ₂
↓	X	L	q ₀	q ₁	q ₂	q ₃
X	X	H	L	L	L	L

NOTES:

- H = High Voltage Level
 h = High Voltage Level One Set-up Time Prior to the Low to High Clock Transition
 L = Low Voltage Level
 l = Low Voltage Level One Set-up Time Prior to the Low to High Clock Transition
 X = Don't Care.
 ↑ = Low to High Clock Transition
 ↓ = High to Low Clock Transition
 q_n = Lower case letters indicate the state of the referenced output one set-up time prior to the Low to High clock transition.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I _{CC}	MAX	0.16	mA
I _{OH}	MAX	-4	mA
I _{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

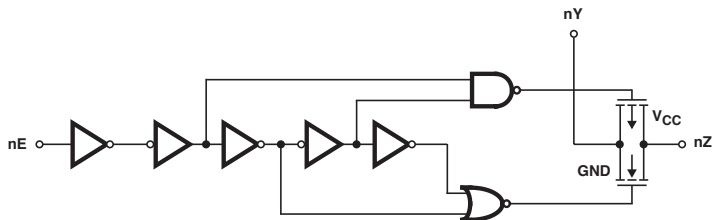
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
f _{max}			MIN	45
t _W	Clock		MIN	24
	MR			45
t _{SUL}	Data-In to CP		MIN	18
t _{SUH}	Data-In to CP		MIN	18
t _H	Data-In to CP		MIN	0
t _{PLH}	Clock	Q _n	MAX	54
t _{PHL}				54
t _{PLH}	MR	Q _n (Clock High)	MAX	83
t _{PHL}				83
t _{PLH}	MR	Q _n (Clock Low)	MAX	98
t _{PHL}				98

UNIT f_{max}: MHz other: ns

4016

QUAD BILATERAL SWITCH

Logic Diagram



FUNCTION TABLE

INPUT nE	SWITCH
L	OFF
H	ON

NOTES:

H = High Level Voltage
L = Low Level Voltage

RECOMMENDED OPERATING CONDITIONS

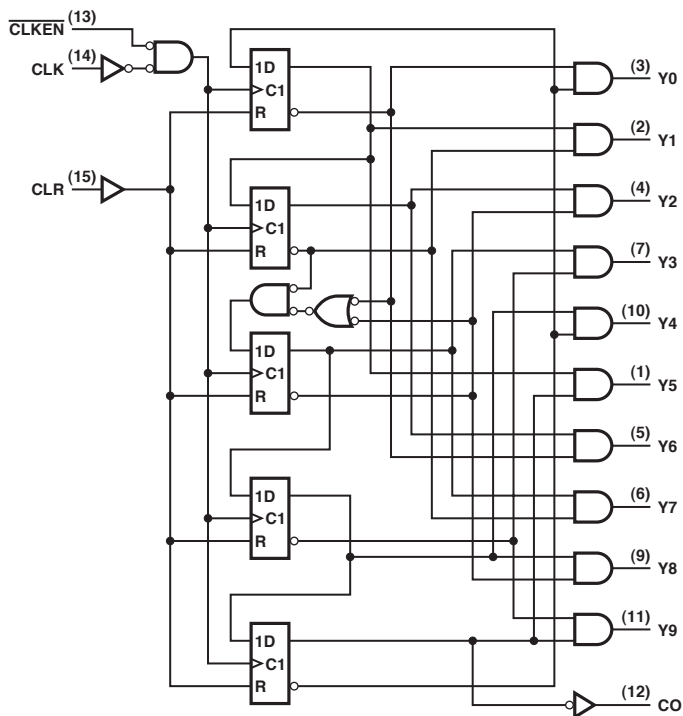
PARAMETER	MAX or MIN	CD74 HC	UNIT
I _{CC}	MAX	0.32	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t _{PLH}	Switch In	Switch Out	MAX	18
t _{FHL}				18
t _{PZH}	En	Z	MAX	57
t _{PZL}				57
t _{PHZ}	En	Z	MAX	44
t _{PLZ}				44

UNIT:ns

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT STATE†
CLK	CLKEN	CLR	
L	X	L	No Change
X	H	L	No Change
X	X	H	"0" = H, "1"- "9" = L
↑	L	L	Increments Counter
↓	X	L	No Change
X	↑	L	No Change
H	↓	L	Increments Counter

NOTES:

H = High Level

L = Low Level

↑ = High to Low Transition

↓ = Low to High Transition

X = Don't Care

 † If $n < 5$ TC = H, Otherwise = L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	UNIT
I _{CC}	MAX	0.08	0.16	mA
I _{DH}	MAX	-4	-4	mA
I _{OL}	MAX	4	4	mA

SWITCHING CHARACTERISTICS

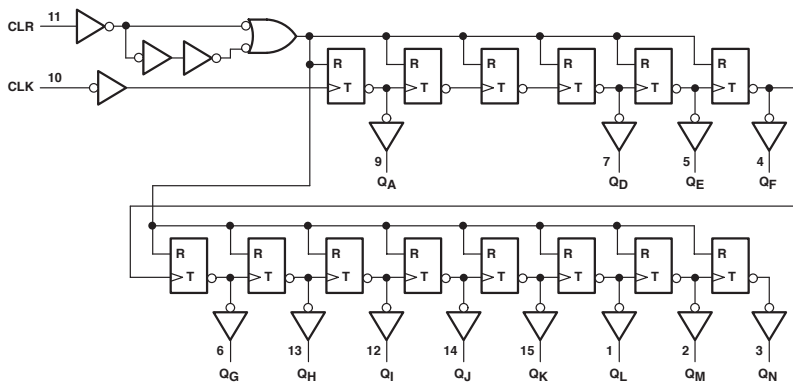
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC
f _{max}			MIN	25	20
t _w	CLK (CP)		MIN	20	24
	CLR (MR) H			20	24
t _{su}	CLKEN to CLK (CE to CP)		MIN	13	22
	CLK Inactive			13	-
t _h	CLKEN to CLK (CE to CP)		MIN	5	0
t _{PLH}	CLK (CP)	Y, C0 (0 to 9, TC)	MAX	58	69
t _{PHL}				58	69
t _{PLH}	CLKEN (CE)	Y, C0 (0 to 9, TC)	MAX	63	75
t _{PHL}				63	75
t _{PLH}	CLR (MR)	Y (0 to 9)	MAX	58	69
t _{PHL}				58	69
t _{PLH}	CLR (MR)	C0 (TC)	MAX	-	69
t _{PHL}				58	69

 UNIT f_{max}: MHz, other: ns

14-STAGE BINARY COUNTERS

- Same Pinouts as CMOS4020
- V_{CC} : 2V to 6V

Logic Diagram



FUNCTION TABLE

CLK	CLR	OUTPUT
↑	L	No Change
↓	L	Advance to Next State
X	H	All Outputs Are Low

NOTE: H = High Voltage Level, L = Low Voltage Level,
 X = Don't Care, = Transition from Low to High Level,
 = Transition from High to Low.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.08	0.16	0.16	mA
I_{OH}	MAX	-4	-4	-4	mA
I_{OL}	MAX	4	4	4	mA

SWITCHING CHARACTERISTICS

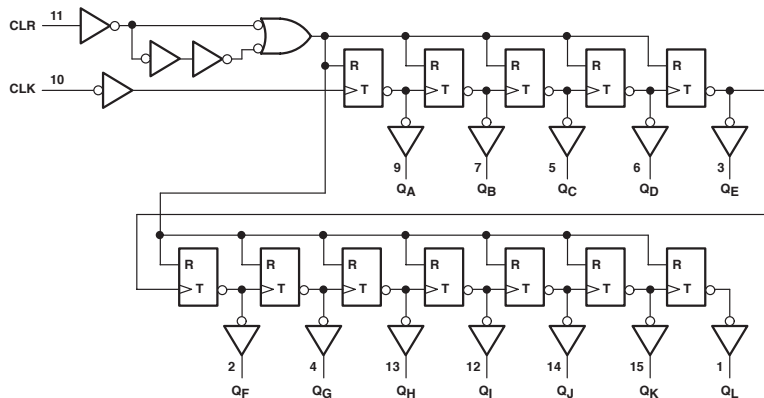
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
f_{max}			MIN	22	20	16
t_w	CLK		MIN	23	24	30
	CLK high		MIN	18	24	30
t_{su}	CLK	CLR inactive before CLK =	MIN	15	-	-
t_{PLH}	CLK	Q_A	MAX	38	42	60
t_{PHL}				38	42	60
t_{PHL}	CLR	Any	MAX	35	51	60

UNIT f_{max} : MHz other : ns

12-STAGE BINARY COUNTERS

- Same Pinouts as CMOS4040
- V_{CC} : 2V to 6V

Logic Diagram



FUNCTION TABLE

CLK	CLR	OUTPUT
↑	L	No Change
↓	L	Advance to Next State
X	H	All Outputs Are Low

NOTE: H = High Voltage Level, L = Low Voltage Level,
 X = Don't Care, ↑ = Transition from Low to High Level,
 ↓ = Transition from High to Low.

RECOMMENDED OPERATING CONDITIONS

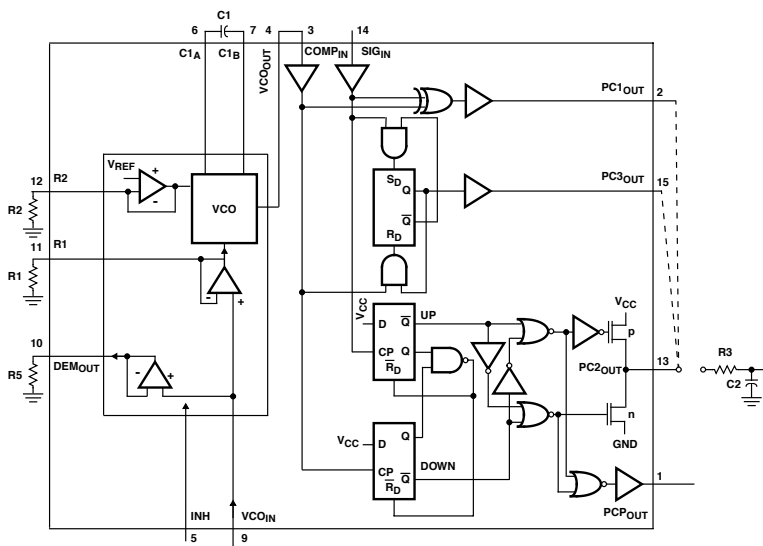
PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.08	0.16	0.16	-	0.02	mA
I_{OH}	MAX	-4	-4	-4	-6	-12	mA
I_{OL}	MAX	4	4	4	6	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
f_{max}			MIN	22	20	16	50	80
t_w	CLK		MIN	23	24	30	5	5
	CLR high			18	24	30	5	5
t_{su}	CLK	CLR inactive before CLK ↓	MIN	15	-	-	5	5
t_{PLH}	CLK	QA	MAX	38	42	60	17.5	10.5
t_{PHL}				38	42	60	17.5	10.5
t_{PHL}	CLR	Any	MAX	35	51	60	18.5	12

UNIT f_{max} : MHz other : ns

Logic Diagram



Pin Descriptions

PIN NUMBER	SYMBOL	NAME AND FUNCTION
1	PCP_OUT	Phase Comparator Pulse Output
2	PC1_OUT	Phase Comparator 1 Output
3	COMP_IN	Comparator Input
4	VCO_OUT	VCO Output
5	INH	Inhibit Input
6	C1A	Capacitor C1 Connection A
7	C1B	Capacitor C1 Connection B
8	GND	Ground (0V)
9	VCO_IN	VCO Input
10	DEM_OUT	Demodulator Output
11	R1	Resistor R1 Connection
12	R2	Resistor R2 Connection
13	PC2_OUT	Phase Comparator 2 Output
14	SIG_IN	Signal Input
15	PC3_OUT	Phase Comparator 3 Output
16	VCC	Positive Supply Voltage

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	0.16	0.16	mA
I _{OH}	MAX	-4	-4	mA
I _{OL}	MAX	4	4	mA

SWITCHING CHARACTERISTICS

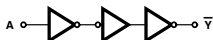
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t _{PLH}	SIG_IN	PC1_OUT	MAX	60	68
t _{PHL}	COMP_IN	PC1_OUT	MAX	60	68
t _{PLH}	SIG_IN	PCP_OUT	MAX	90	102
t _{PHL}	COMP_IN	PCP_OUT	MAX	90	102
t _{PLH}	SIG_IN	PC3_OUT	MAX	74	87
t _{PHL}	COMP_IN	PC3_OUT	MAX	74	87
t _{TTL}			MAX	22	22
t _{TTL}	A	\bar{V}	MAX	22	22
t _{F2H}	SIG_IN	PC2_OUT	MAX	80	90
t _{F2L}	COMP_IN	PC2_OUT	MAX	80	90
t _{PLZ}	SIG_IN	PC2_OUT	MAX	95	102
t _{PHZ}	COMP_IN	PC2_OUT	MAX	95	102

UNIT:ns

4049

HEX INVERTING BUFFERS

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

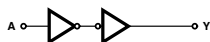
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t_{PLH}	nA	$n\bar{Y}$	MAX	26
t_{PHL}				26

UNIT:ns

4050

HEX NON-INVERTING BUFFERS

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

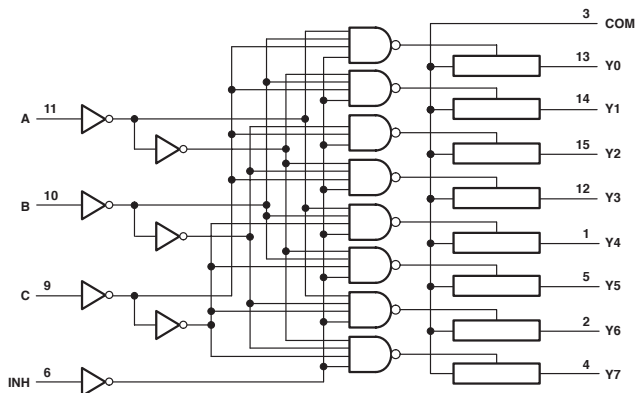
PARAMETER	MAX or MIN	CD74 HC	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t_{PLH}	nA	nY	MAX	26
t_{PHL}				26

UNIT:ns

Logic Diagram



FUNCTION TABLE

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	Y0
L	L	L	H	Y1
L	L	H	L	Y2
L	L	H	H	Y3
L	H	L	L	Y4
L	H	L	H	Y5
L	H	H	L	Y6
L	H	H	H	Y7
H	X	X	X	None

RECOMMENDED OPERATING CONDITIONS

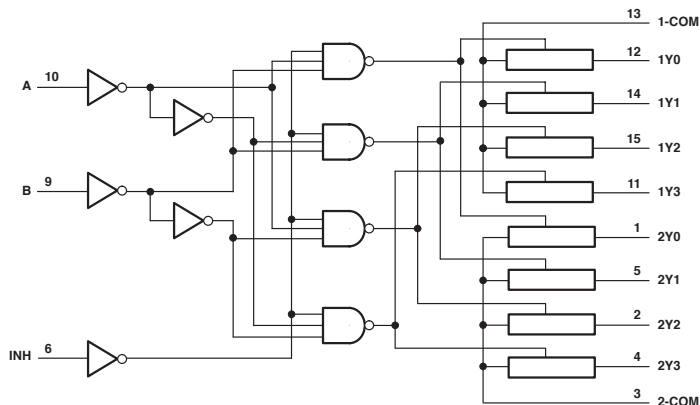
PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I _{CC}	MAX	0.16	0.16	-	0.02	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V
t _{PLH}	COM or Y _n	Y _n or COM	MAX	18	18	12	8
				18	18	12	8
t _{PHL}	INH	COM or Y _n	MAX	68	83	25	18
t _{PZL}				68	83	25	18
t _{PHZ}	INH	COM or Y _n	MAX	68	68	25	18
t _{PLZ}				68	68	25	18

UNIT: ns

Logic Diagram



FUNCTION TABLE

INPUTS			ON
INH	B	A	CHANNEL
L	L	L	1Y0, 2Y0
L	L	H	1Y1, 2Y1
L	H	L	1Y2, 2Y2
L	H	H	1Y3, 2Y3
H	X	X	None

RECOMMENDED OPERATING CONDITIONS

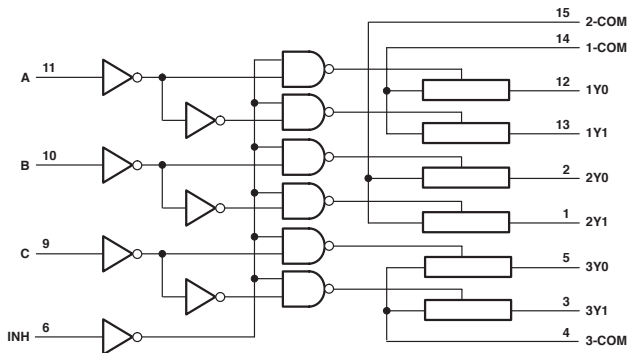
PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.16	0.16	-	0.02	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V
t_{PLH}	COM or Yn	Yn or COM	MAX	18	18	12	8
t_{PHL}				18	18	12	8
t_{PZH}	INH	COM or Yn	MAX	98	105	25	18
t_{PZL}				98	105	25	18
t_{PHZ}	INH	COM or Yn	MAX	75	75	25	18
t_{PLZ}				75	75	25	18

TRIPLE 2-CHANNEL ANALOG MULTIPLEXERS/DEMULTIPLEXERS

Logic Diagram



FUNCTION TABLE

INPUTS				ON CHANNEL
INH	C	B	A	
L	L	L	L	1Y0, 2Y0, 3Y0
L	L	L	H	1Y1, 2Y0, 3Y0
L	L	H	L	1Y0, 2Y1, 3Y0
L	L	H	H	1Y1, 2Y1, 3Y0
L	H	L	L	1Y0, 2Y0, 3Y1
L	H	L	H	1Y1, 2Y0, 3Y1
L	H	H	L	1Y0, 2Y1, 3Y1
L	H	H	H	1Y1, 2Y1, 3Y1
H	X	X	X	None

RECOMMENDED OPERATING CONDITIONS

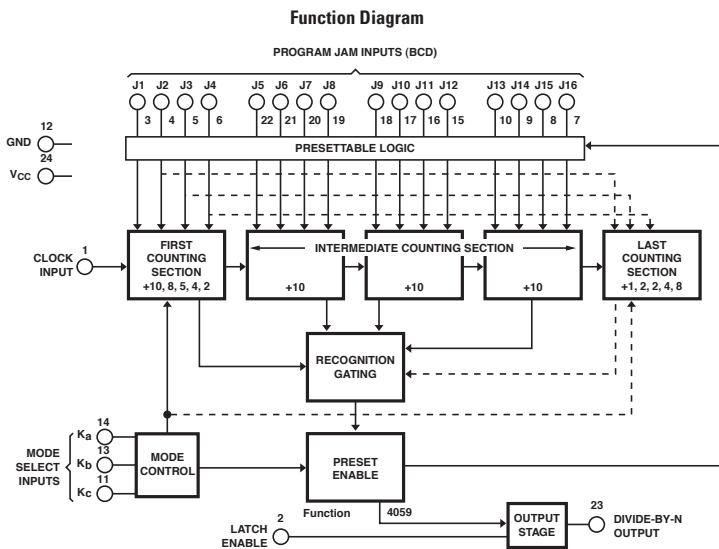
PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I _{CC}	MAX	0.16	0.16	-	0.02	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT	LV 3V	LV 5V
t _{PLH}	COM or Y _n	Y _n or COM	MAX	18	18	12	8
t _{PHL}				18	18	12	8
t _{PZH}	INH	COM or Y _n	MAX	66	72	25	18
t _{PZL}				66	72	25	18
t _{PHZ}	INH	COM or Y _n	MAX	63	66	25	18
t _{PLZ}				63	66	25	18

UNIT: ns

CMOS PROGRAMMABLE DIVIDE-BY-N COUNTER



FUNCTION TABLE

MODE SELECT INPUT	MODE SELECT INPUT		
	Ka	Kb	Kc
H	H	H	H
L	H	L	H
L	L	L	H
H	H	H	L
X	L	L	L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I _{CC}	MAX	0.16	mA
I _{QH}	MAX	-4	mA
I _{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

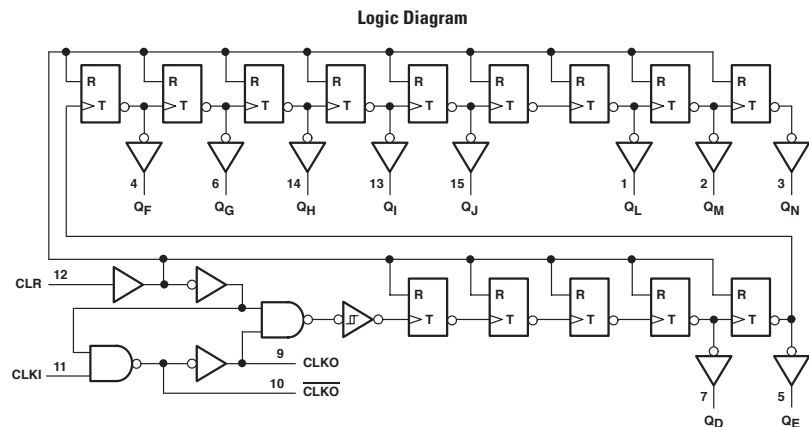
PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
f _{max}	CP		MIN	18
t _w	CP		MIN	27
t _{su}	Kb, Kc to CP		MIN	22
t _{PLH}	CP	Q	MAX	60
t _{PHL}				60
t _{PLH}	LE	Q	MAX	53
t _{PHL}				53

UNIT f_{max} : MHz other : ns

4060

ASYNCHRONOUS 14-STAGE BINARY COUNTERS AND OSCILLATORS

- Same Pinouts as CMOS4060
- Allow Design of Either RC or Crystal Oscillator Circuits
- V_{CC} : 2V to 6V



FUNCTION TABLE

INPUTS		OUTPUTS		
CLKI	CLR	Q _D to Q _N	CLKO	CLKO
1	L	No Change	1	↓
↓	L	Advance to Next State	↓	↑
X	H	All Outputs are Low	L	H

OPERATING CONDITIONS

MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
MAX	0.08	0.16	0.16	mA
MAX	-4	-4	-4	mA
MAX	4	4	4	mA

SWITCHING CHARACTERISTICS

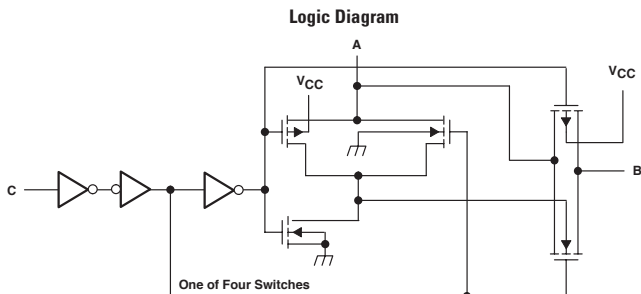
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
f_{max}			MIN	22	20	20
t_w	CLKI		MIN	23	24	24
	CLR high			23	24	38
t_{su}	CLR inactive before CLK ↓		MIN	40	-	-
t_{PLH}	CLKI	Q _D	MAX	123	90	100
t_{PHL}				123	90	100
t_{PHL}	CLR	Any	MAX	35	53	66

UNIT f_{max} : MHz other : ns

4066

QUADRUPLE BILATERAL SWITCHES

- Same Pinouts as CMOS4016, 4066
- Low On-State Impedance: 50-Ω TYP at $V_{CC} = 6V$
- Individual Switch Controls
- Extremely Low Input Current
- High On-Off Output Voltage Ratio
- Low Crosstalk Between Switches



FUNCTION TABLE

INPUT (C)	SWITCH
L	OFF
H	ON

NOTE:

H = High Level

L = Low Level

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V	UNIT
I_{CC}	MAX	0.02	0.04	0.04	-	0.02	mA

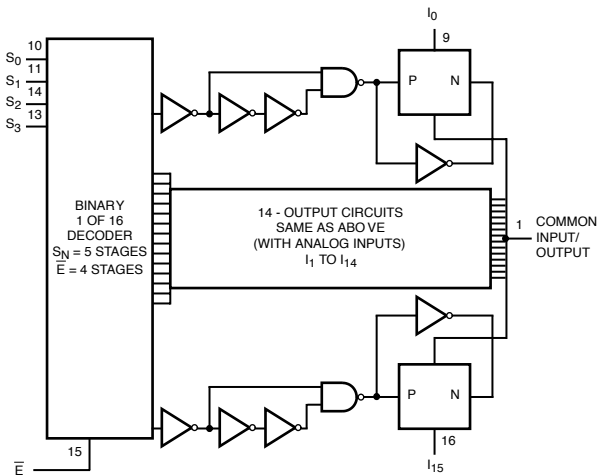
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	LV 3V	LV 5V
t_{PLH}	A or B	B or A	MAX	15	18	18	12	8
t_{PHL}				15	18	18	12	8
t_{PZH}	C	A or B	MAX	45	30	36	22	16
t_{PZL}				45	30	36	22	16
t_{PHZ}	C	A or B	MAX	50	45	53	22	16
t_{PLZ}				50	45	53	22	16

UNIT: ns

16-CHANNEL ANALOG MULTIPLEXER/DEMULTIPLEXER

Function Diagram



FUNCTION TABLE

S0	S1	S2	S3	\bar{E}	SELECTED CHANNEL
X	X	X	X	X	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

NOTES:

H = High Level
L = Low Level

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	0.16	0.16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t _{PLH}	Switch In	COMON I/O	MAX	22	22
t _{PHL}				83	90
t _{PZH}	\bar{E}	COMON I/O	MAX	83	90
t _{PZL}				90	90
t _{PZH}	S _n	COMON I/O	MAX	90	90
t _{PZL}				87	87
t _{PHZ}	\bar{E}	COMON I/O	MAX	83	83
t _{PLZ}				83	83
t _{PHZ}	S _n	COMON I/O	MAX	87	87
t _{PLZ}				87	87

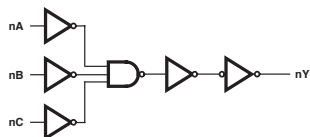
UNIT:ns

4075

TRIPLE 3-INPUT OR GATES

● $Y = A + B + C$

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
A	B	C	Y
L	L	L	L
H	X	X	H
X	H	X	H
X	X	H	H

NOTES:

H = High Voltage Level

L = Low Voltage Level

X = Don't Care

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.02	0.04	0.04	mA
I_{OH}	MAX	-4	-4	-4	mA
I_{OL}	MAX	4	4	4	mA

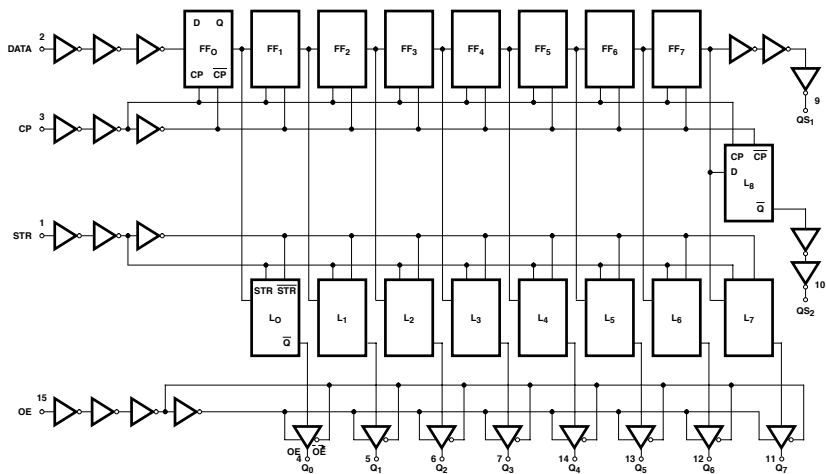
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
t_{PLH}	A, B or C	Y	MAX	25	30	36
t_{PHL}	A, B or C	Y	MAX	25	30	36

UNIT:ns

8-STAGE SHIFT AND STORE BUS REGISTER, THREE-STATE

Logic Diagram



FUNCTION TABLE

INPUTS				PALALLEL OUTPUT		SERIAL OUTPUT	
CP	OE	STR	D	Q ₀	Q _n	Q _{S1} ‡	Q _{S2}
↑	L	X	X	Z	Z	Q ₆	NC
↓	L	X	X	Z	Z	NC	Q ₇
↑	H	L	X	NC	NC	Q ₆	NC
↑	H	H	L	L	Q _{n-1}	Q ₆	NC
↑	H	H	H	H	Q _{n-1}	Q ₆	NC
↓	H	H	H	NC	NC	NC	Q ₇

NOTES:

1. H = High Voltage Level, L = Low Voltage Level, X = Don't Care.

NC = No change, Z = High Impedance Off-state.

↑ = Transition from Low to High Level, ↓ = Transition from High Low.

‡ At the positive clock edge the information in the seventh register stage is transferred to the 8th register stage and Q_{S1} output.

RECOMMENDED OPERATING CONDITIONS

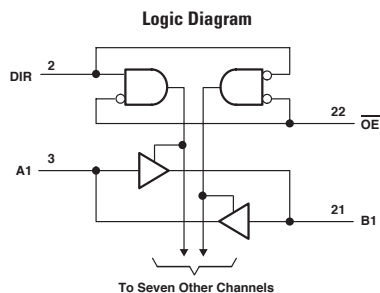
PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	0.16	0.16	mA
I _{OL}	MAX	4	4	mA
I _{OH}	MAX	-4	-4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t _W	CP		MIN	24	24
t _{WH}	STR		MIN	24	24
t _{SU}	Data		MIN	15	15
	STR			30	30
t _H	Data		MIN	3	4
	STR			0	0
t _{PLH}	CP	Q _{S1}	MAX	45	-
t _{PHL}				45	-
t _{PLH}	CP	Q _{S2}	MAX	41	-
t _{PHL}				41	-
t _{PLH}	CP	Q _n	MAX	59	-
t _{PHL}				59	-
t _{PLH}	STR	Q _n	MAX	54	-
t _{PHL}				54	-
t _{PZH}	OE	Q _n	MAX	53	-
t _{PZL}				53	-
t _{PLZ}	OE	Q _n	MAX	38	-
t _{PHZ}				38	-

UNIT:ns

OCTAL BUS TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

**FUNCTION TABLE**

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVC	LVCC	UNIT
I_{CCA}	MAX	0.08	0.08	mA
I_{CCB}	MAX	0.05	0.08	mA
I_{OH}	MAX	-24	-24	mA
I_{OL}	MAX	24	24	mA

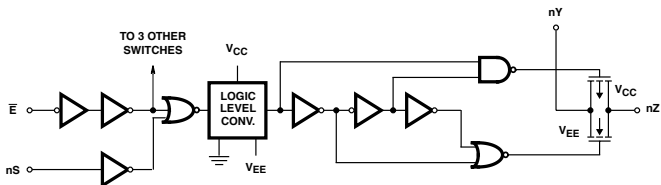
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC	LVCC V_{CC} 3.3V
t_{PLH}	A	B	MAX	6.3	7
t_{PHL}				6.7	7
t_{PLH}	B	A	MAX	6.1	6.2
t_{PHL}				5	5.3
t_{PZL}	\overline{OE}	A	MAX	9	9
t_{PZH}				8.1	8
t_{PZL}	\overline{OE}	B	MAX	8.8	10
t_{PZH}				9.8	10.2
t_{PLZ}	\overline{OE}	A	MAX	7	5.2
t_{PHZ}				5.8	5.2
t_{PLZ}	\overline{OE}	B	MAX	7.7	5.4
t_{PHZ}				7.8	7.4

UNIT: ns

QUAD ANALOG SWITCH WITH LEVEL TRANSLATION

Logic Diagram



FUNCTION TABLE

INPUTS		SWITCH
E	S	
L	L	OFF
L	H	ON
H	X	OFF

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	0.16	0.16	mA

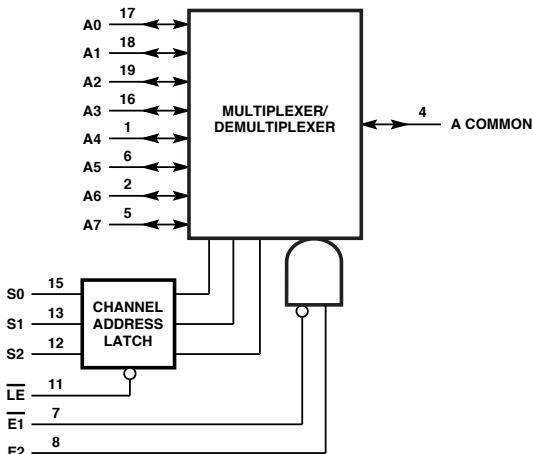
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t _{PLH}	Switch in	Switch out	MAX	18	18
t _{PHL}				18	18
t _{PZH}	E-bar	Z	MAX	62	66
t _{PZL}				62	85
t _{PZH}	nS	Z	MAX	53	60
t _{PZL}				53	75
t _{PLZ}	E-bar	Z	MAX	62	75
t _{PHZ}				62	-
t _{PLZ}	nS	Z	MAX	53	-
t _{PHZ}				53	66

UNIT:ns

ANALOG MULTIPLEXERS/DEMULTIPLEXERS WITH LATCH

Logic Diagram



FUNCTION TABLE

INPUTS					"ON"† SWITCHES LE = H
$\overline{E1}$	E2	S2	S1	S0	
L	H	L	L	L	A ₀
L	H	L	L	H	A ₁
L	H	L	H	L	A ₂
L	H	L	H	H	A ₃
L	H	H	L	L	A ₄
L	H	H	L	H	A ₅
L	H	H	H	L	A ₆
L	H	H	H	H	A ₇
H	L	X	X	X	None

NOTES:

† When LE is low S₀-S₂ data are latched and switches cannot change state.
H = High Voltage Level, L = Low Voltage Level, X = Don't Care

RECOMMENDED OPERATING CONDITIONS

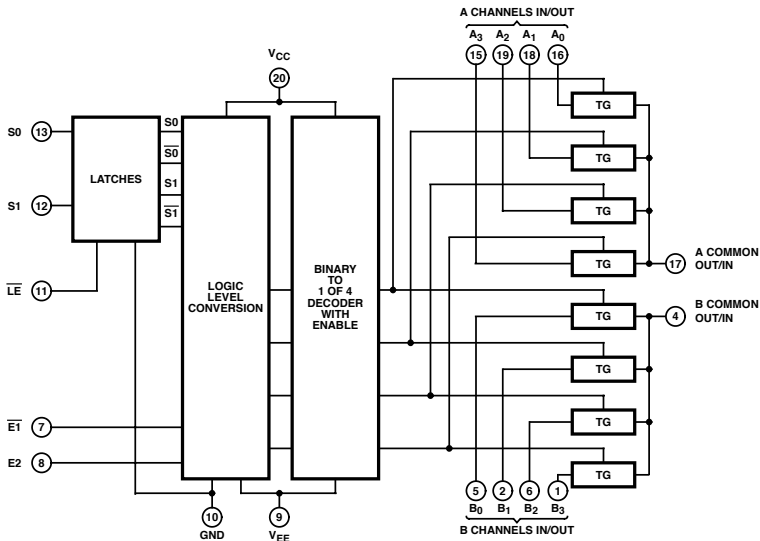
PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	0.16	0.16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t _W	\overline{LE}		MIN	30	28
t _{su}	S _n to \overline{LE}		MIN	-	-
t _h	S _n to \overline{LE}		MIN	5	5
t _{PLH}	Switch In	Switch Out	MAX	11	11
t _{PHL}				11	11
t _{PZH}	$\overline{E1}$, E2, \overline{LE}	V _{os}	MAX	90	113
t _{PZL}				90	113
t _{PZH}	S _n	V _{os}	MAX	90	113
t _{PZL}				90	113
t _{PLZ}	$\overline{E1}$	V _{os}	MAX	75	83
t _{PHZ}				75	83
t _{PLZ}	E2	V _{os}	MAX	75	90
t _{PHZ}				75	90
t _{PLZ}	\overline{LE}	V _{os}	MAX	83	90
t _{PHZ}				83	90
t _{PLH}	S _n	V _{os}	MAX	83	98
t _{PHL}				83	98

UNIT:ns

Function Diagram



FUNCTION TABLE

INPUTS				"ON"†
E1	E2	S1	S0	SWITCHES LE = H
L	H	L	L	A ₀ , B ₀
L	H	L	H	A ₁ , B ₁
L	H	H	L	A ₂ , B ₂
L	H	H	H	A ₃ , B ₃
H	L	X	X	None

NOTES:

† When LE is low S0-S2 data are latched and switches cannot change state.

H = High Voltage Level, L = Low Voltage Level, X = Don't Care

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I _{CC}	MAX	0.16	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
t _w	LE		MIN	30
t _{su}	S _n to LE		MIN	-
t _h	S _n to LE		MIN	5
t _{PLH}	Switch In	Switch Out	MAX	11
t _{PHL}			11	
t _{PZH}	E1, E2, LE	V _{os}	MAX	105
t _{PZL}			105	
t _{PZH}	S _n	V _{os}	MAX	113
t _{PZL}			113	
t _{PLZ}	E1, E2, LE	V _{os}	MAX	83
t _{PHZ}			83	

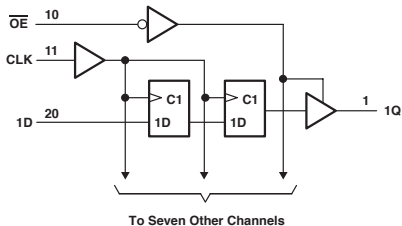
UNIT:ns

4374

OCTAL EDGE-TRIGGERED D-TYPE DUAL-RANK FLIP-FLOP WITH 3-STATE OUTPUTS

- 3-State Outputs Drive Bus Lines Directly

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q _O
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

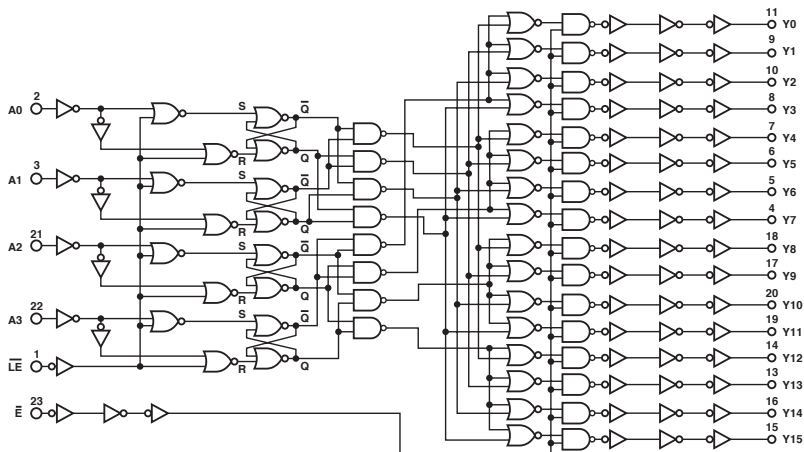
PARAMETER	MAX or MIN	AS	UNIT
I _{CC}	MAX	150	mA
I _{OH}	MAX	-15	mA
I _{OL}	MAX	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AS
f _{max}			MIN	125
t _w			MIN	4
t _{su}			MIN	4
t _h			MIN	1
t _{PLH}	CLK	Q	MAX	8
t _{PHL}				8
t _{PZH}	OE	Q	MAX	6
t _{PZL}				8
t _{PHZ}	OE	Q	MAX	6.5
t _{PLZ}				7

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

 ($\overline{LE} = H$)

\overline{E}	DECODER INPUTS				ADDRESSED OUTPUT H
	A3	A2	A1	A0	
L	L	L	L	L	Y0
L	L	L	L	H	Y1
L	L	L	H	L	Y2
L	L	L	H	H	Y3
L	L	H	L	L	Y4
L	L	H	L	H	Y5
L	L	H	H	L	Y6
L	L	H	H	H	Y7
L	H	L	L	L	Y8
L	H	L	L	H	Y9
L	H	L	H	L	Y10
L	H	L	H	H	Y11
L	H	H	L	L	Y12
L	H	H	L	H	Y13
L	H	H	H	L	Y14
L	H	H	H	H	Y15
H	X	X	X	X	All outputs = L

H = high, L = low, X = don't care

RECOMMENDED OPERATING CONDITIONS

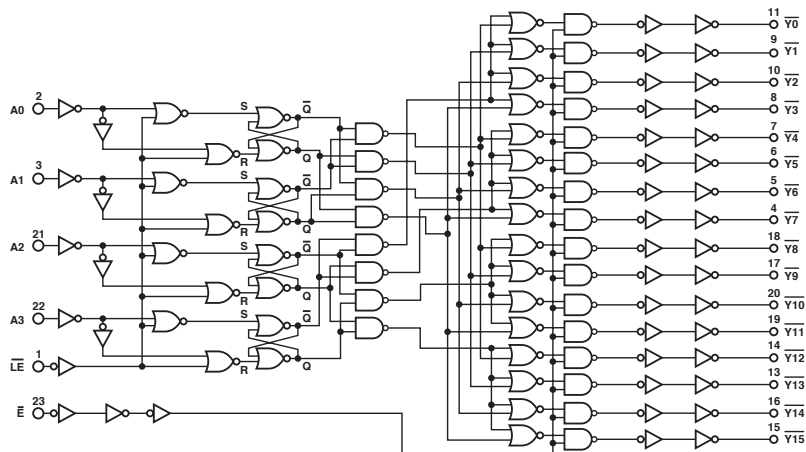
PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	0.08	0.16	0.08	mA
I _{DH}	MAX	-4	-4	-6	mA
I _{OL}	MAX	4	4	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
t _w	LE (\overline{LE})		MIN	20	22	38
t _{su}	LE (\overline{LE})		MIN	25	30	25
t _h	LE (\overline{LE})		MIN	5	0	5
t _{PLH}	A, B, C, D (A1, 2, 3, 4)	Y	MAX	58	83	69
t _{PHL}				58	83	69
t _{PLH}	LE (\overline{LE})	Y	MAX	58	68	63
t _{PHL}				58	68	63
t _{PLH}	\overline{E} (E)	Y	MAX	44	53	50
t _{PHL}				44	53	50

UNIT:ns

Logic Diagram



FUNCTION TABLE
($\overline{LE} = H$)

\overline{E}	DECODER INPUTS				ADDRESSED OUTPUT L
	A3	A2	A1	A0	
L	L	L	L	L	Y0
L	L	L	L	H	Y1
L	L	L	H	L	Y2
L	L	L	H	H	Y3
L	L	H	L	L	Y4
L	L	H	L	H	Y5
L	L	H	H	L	Y6
L	L	H	H	H	Y7
L	H	L	L	L	Y8
L	H	L	L	H	Y9
L	H	L	H	L	Y10
L	H	L	H	H	Y11
L	H	H	L	L	Y12
L	H	H	L	H	Y13
L	H	H	H	L	Y14
L	H	H	H	H	Y15
H	X	X	X	X	All outputs = H

H = high, L = low, X = don't care

RECOMMENDED OPERATING CONDITIONS

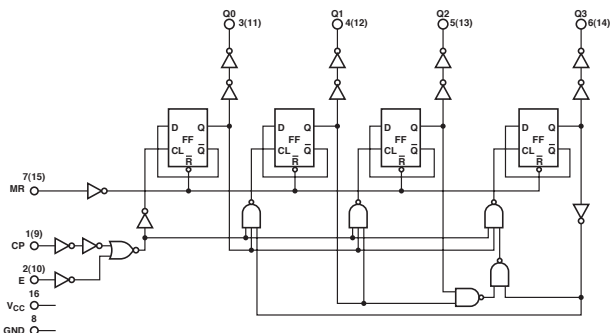
PARAMETER	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	0.08	0.16	0.08	mA
I _{DH}	MAX	-4	-4	-6	mA
I _{OL}	MAX	4	4	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC	CD74 HCT
t _w	LE (\overline{LE})		MIN	20	22	38
t _{su}	LE (\overline{LE})		MIN	25	30	25
t _h	LE (\overline{LE})		MIN	5	0	5
t _{PLH}	A, B, C, D (A1, 2, 3, 4)	\overline{Y}	MAX	58	83	69
t _{PHL}		(CD74HCT:Y)		58	83	69
t _{PLH}	\overline{LE} (\overline{LE})	\overline{Y}	MAX	58	68	63
t _{PHL}		(CD74HCT:Y)		58	68	63
t _{PLH}	\overline{E} (\overline{E})	\overline{Y}	MAX	44	53	50
t _{PHL}		(CD74HCT:Y)		44	53	50

UNIT:ns

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT STATE
CP	E	MR	
↑	H	L	Increment Counter
↓	X	L	Increment Counter
↓	X	L	No Change
H	↑	L	No Change
↑	L	L	No Change
H	↓	L	No Change
L	X	H	Q ₀ thru Q ₃ = L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	UNIT
I _{CC}	MAX	0.16	mA
I _{DH}	MAX	-4	mA
I _{OL}	MAX	4	mA

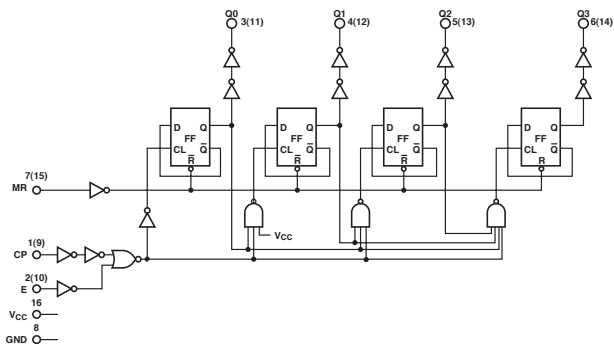
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC
f _{max}			MIN	20
t _w	CP		MIN	24
	MR			30
t _{su}	Enable to CP		MIN	24
	CP to Enable			24
t _{PLH}	CP	Q _n	MAX	72
t _{PHL}				72
t _{PLH}	Enable	Q _n	MAX	72
t _{PHL}				72
t _{PLH}	MR	Q _n	MAX	45
t _{PHL}				45

UNIT f_{max} : MHz other : ns

DUAL SYNCHRONOUS COUNTERS

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT STATE
CP	E	MR	
↑	H	L	Increment Counter
↓	↓	L	Increment Counter
↓	X	L	No Change
X	↑	L	No Change
↑	L	L	No Change
H	↓	L	No Change
X	X	H	Q ₀ thru Q ₃ = L

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	0.16	0.16	mA
I _{OH}	MAX	-4	-4	mA
I _{OL}	MAX	4	4	mA

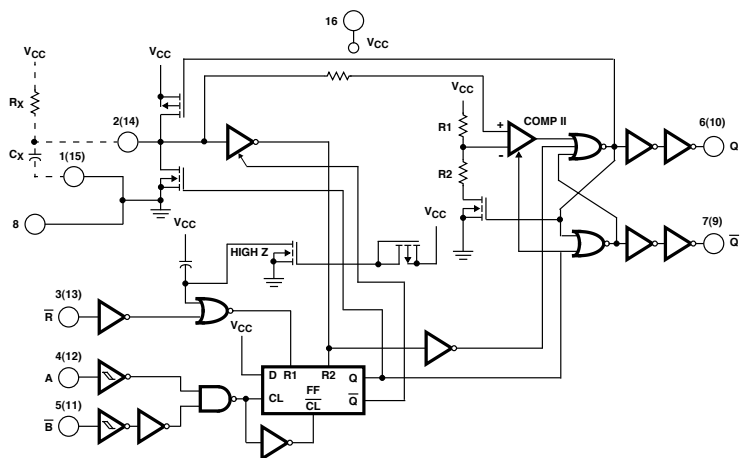
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t _{max}			MIN	20	17
t _w	CP		MIN	24	30
	MR			30	30
t _{su}	Enable to CP		MIN	24	24
	CP to Enable			24	-
t _{PLH}	CP	Q _n	MAX	72	80
t _{PHL}				72	80
t _{PLH}	Enable	Q _n	MAX	72	83
t _{PHL}				72	83
t _{PLH}	MR	Q _n	MAX	45	53
t _{PHL}				45	53

UNIT f_{max} : MHz other : ns

DUAL RETRIGGERABLE PRECISION MONO STABLE MULTIVIBRATOR

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
R	A	B	E	Q
L	X	X	L	H
X	H	X	L	H
X	X	L	L	H
H	L	L	JL	JH
H	H	H	JL	JH

RECOMMENDED OPERATING CONDITIONS

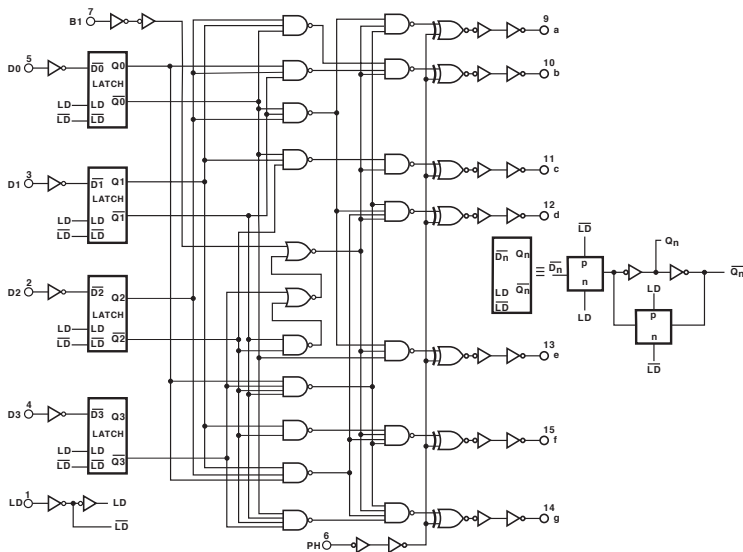
PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	0.16	0.16	mA
I _{OH}	MAX	-4	-4	mA
I _{OL}	MAX	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t _W ⁺	A, B		MIN	24	24
t _{WL}	A, B			24	24
t _{WL}	R			24	30
t _{PLH}	A, B	Q	MAX	75	83
t _{PHL}		Q		75	83
t _{PLH}	R	Q	MAX	-	75
t _{PHL}		Q		75	60

UNIT:ns

Logic Diagram



FUNCTION TABLE

LD	B1	PH	D3	D2	D1	D0	a	b	c	d	e	f	g	Display
X	H	L	X	X	X	X	L	L	L	L	L	L	L	Blank
H	L	L	L	L	L	L	H	H	H	H	H	H	L	0
H	L	L	L	L	L	H	L	H	H	L	L	L	L	1
H	L	L	L	L	H	H	H	H	L	H	H	L	H	2
H	L	L	L	L	H	H	H	H	H	H	L	L	H	3
H	L	L	L	H	L	L	L	H	H	L	L	H	H	4
H	L	L	L	H	L	H	H	L	H	H	L	H	H	5
H	L	L	L	H	H	L	H	L	H	H	H	H	H	6
H	L	L	L	H	H	H	H	H	H	L	L	L	L	7
H	L	L	H	L	L	L	H	H	H	H	H	H	H	8
H	L	L	H	L	L	H	H	H	L	H	L	H	H	9
H	L	L	H	L	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	L	H	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	L	L	L	L	L	L	L	L	Blank
H	L	L	H	H	H	X	L	L	L	L	L	L	L	Blank
L	as above	N	X	X	X	X	inverse above							as above

NOTES:

Depends open the BCD code previously applied when LE = High

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I _{CC}	MAX	0.16	0.16	mA
I _{OH}	MAX	-1	-1	mA
I _{OL}	MAX	1	1	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t _W	Latch Disable		MIN	13	13
t _{su}	Dn to LD		MIN	15	15
t _h	Dn to LD		MIN	8	10
t _{PLH}	Dn	a to g	MAX	85	100
t _{PHL}				85	100
t _{PLH}	LD	a to g	MAX	93	96
t _{PHL}				93	96
t _{PLH}	B1	a to g	MAX	66	83
t _{PHL}				66	83
t _{PLH}	PH	a to g	MAX	50	83
t _{PHL}				50	83

UNIT:ns

5400

11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT5400A)

FUNCTION TABLE

INPUTS			INPUT
OE1	OE2	D	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

RECOMMENDED OPERATING CONDITIONS

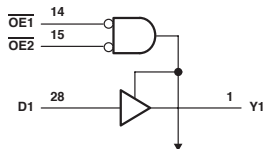
PARAMETER	MAX or MIN	ABT	UNIT
I _{CC}	MAX	45	mA
I _{OH}	MAX	-12	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t _{PLH}	D	Y	MAX	6.2
t _{PHL}				5.6
t _{PDH}	\overline{OE}	Y	MAX	8.7
t _{PZL}				7.5
t _{PHZ}	\overline{OE}	Y	MAX	5.2
t _{PLZ}				6.9

UNIT: ns

Logic Diagram



To Ten Other Channels

5401

11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT5401)

FUNCTION TABLE

INPUTS			OUTPUT
OE1	OE2	D	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

RECOMMENDED OPERATING CONDITIONS

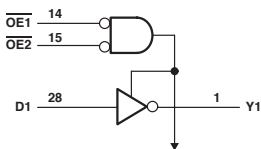
PARAMETER	MAX or MIN	ABT	UNIT
I _{CC}	MAX	45	mA
I _{OH}	MAX	-12	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t _{PLH}	D	Y	MAX	6.9
t _{PHL}				5.7
t _{PDH}	\overline{OE}	Y	MAX	8.5
t _{PZL}				6.8
t _{PHZ}	\overline{OE}	Y	MAX	5.2
t _{PLZ}				6.9

UNIT: ns

Logic Diagram



To Ten Other Channels

5402

12-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT5402A)

FUNCTION TABLE

INPUTS			OUTPUT
OE1	OE2	D	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

RECOMMENDED OPERATING CONDITIONS

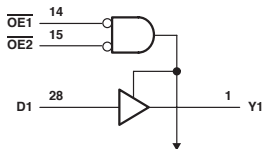
PARAMETER	MAX or MIN	ABT	UNIT
I _{CC}	MAX	48	mA
I _{OH}	MAX	-12	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t _{PLH}	D	Y	MAX	6.2
t _{PHL}				5.6
t _{PZH}	\overline{OE}	Y	MAX	8.7
t _{PZL}				7.5
t _{BPHZ}	\overline{OE}	Y	MAX	5.2
t _{BPLZ}				6.9

UNIT: ns

Logic Diagram



To Eleven Other Channels

5403

11-BIT LINE/MEMORY DRIVERS WITH 3-STATE OUTPUTS

- Output Ports Have Equivalent 25-Ω Series Resistors, So No External Resistors Are Required (SN74ABT5403)

FUNCTION TABLE

INPUTS			OUTPUT
OE1	OE2	D	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

RECOMMENDED OPERATING CONDITIONS

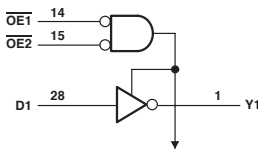
PARAMETER	MAX or MIN	ABT	UNIT
I _{CC}	MAX	45	mA
I _{OH}	MAX	-12	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t _{PLH}	D	Y	MAX	6.9
t _{PHL}				5.7
t _{PZH}	\overline{OE}	Y	MAX	8.5
t _{PZL}				6.8
t _{BPHZ}	\overline{OE}	Y	MAX	5.2
t _{BPLZ}				6.9

UNIT: ns

Logic Diagram



To 11 Other Channels

7001

QUADRUPLE POSITIVE-AND GATES WITH SCHMITT-TRIGGER INPUTS

- Same Pinouts as SN74HC08
- V_{CC} : 2V to 6V
- Schmitt-Triggered Inputs
- $Y = A \cdot B$

RECOMMENDED OPERATING CONDITIONS

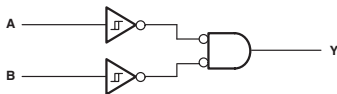
PARAMETER	MAX or MIN	HC	UNIT
I_{CC}	MAX	0.02	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	HC
t_{PLH}	A or B	Y	MAX	33
t_{PHL}				33

UNIT: ns

Logic Diagram



7002

QUADRUPLE POSITIVE-NOR GATES WITH SCHMITT-TRIGGER INPUTS

- Same Pinouts as SN74HC36
- V_{CC} : 2V to 6V
- Schmitt-Triggered Inputs
- $Y = \overline{A + B}$

RECOMMENDED OPERATING CONDITIONS

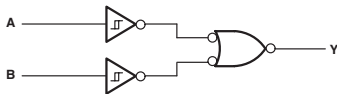
PARAMETER	MAX or MIN	HC	UNIT
I_{CC}	MAX	0.02	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	HC
t_{PLH}	A or B	Y	MAX	33
t_{PHL}				33

UNIT: ns

Logic Diagram

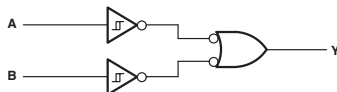


7032

QUADRUPLE 2-INPUT POSITIVE-OR GATES WITH SCHMITT-TRIGGER INPUTS

- Same Pinouts as SN74HC32
- V_{CC} : 2V to 6V
- Schmitt-Triggered Inputs
- $Y = A + B$

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	HC	UNIT
I_{CC}	MAX	0.02	mA
I_{OH}	MAX	-4	mA
I_{OL}	MAX	4	mA

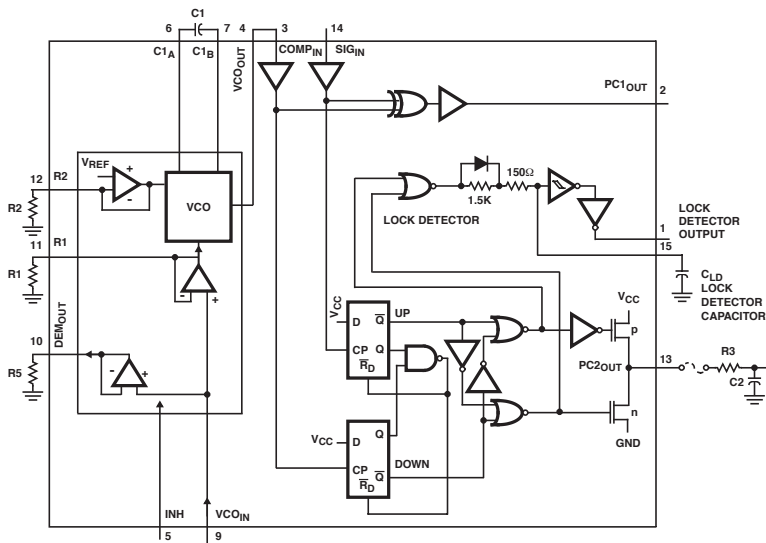
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	HC
t_{PLH}	A or B	Y	MAX	33
t_{PHL}				33

UNIT: ns

PHASE-LOCKED LOOP WITH VCO AND LOCK DETECTOR

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA
I_{OH}	MAX	-4	-4	mA
I_{OL}	MAX	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_{PLH}	SIG _{IN} , COMP _{IN}	PC1 _{OUT}	MAX	60	68
t_{PHL}				60	68
t_{PZH}	SIG _{IN} , COMP _{IN}	PC2 _{OUT}	MAX	84	90
t_{PZL}				84	90
t_{PHZ}	SIG _{IN} , COMP _{IN}	PC2 _{OUT}	MAX	98	105
t_{PLZ}				98	105

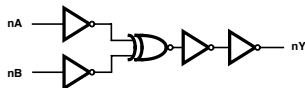
UNIT:ns

7266

QUAD 2-INPUT EXCLUSIVE-NOR GATES

$$Y = \overline{A \oplus B}$$

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
A	B	Y
L	L	H
L	H	L
H	L	L
H	H	H

NOTES:

H = High Voltage Level
L = Low Voltage Level

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 HC	CD74 HC	UNIT
I_{CC}	MAX	0.02	0.04	mA
I_{OH}	MAX	-4	-4	V
I_{OL}	MAX	4	4	V

SWITCHING CHARACTERISTICS

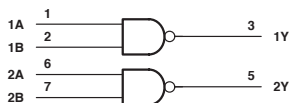
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 HC	CD74 HC
t_{PLH}	A or B	Y	MAX	25	35
t_{PHL}		Y	MAX	25	35

UNIT: ns

8003

DUAL 2-INPUT POSITIVE-NAND GATES

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

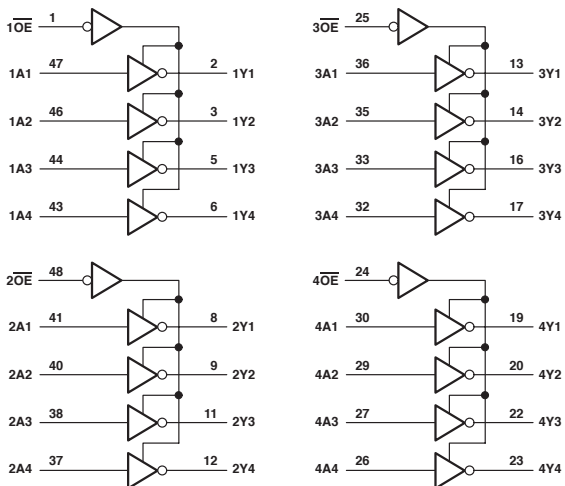
PARAMETER	MAX or MIN	ALS	AS	UNIT
I_{CC}	MAX	1.5	8.7	mA
I_{OH}	MAX	-0.4	-2	mA
I_{OL}	MAX	8	20	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	AS
t_{PLH}	A or B	Y	MAX	11	4.5
t_{PHL}				8	4

UNIT: ns

Logic Diagram



FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
OE	A	Y
L	H	L
L	L	H
H	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVT 3V	AC	ACT	AHC	AHCT	LVCH 3V	LVCZ 3V	ALVCH 3V	UNIT
I _{CC}	MAX	34	5	5	5	0.08	0.08	0.04	0.04	0.02	0.1	0.04	mA
I _{OH}	MAX	-32	-32	-32	-32	-24	-24	-8	-8	-24	-24	-24	mA
I _{OL}	MAX	64	64	64	64	24	24	8	8	24	24	24	mA

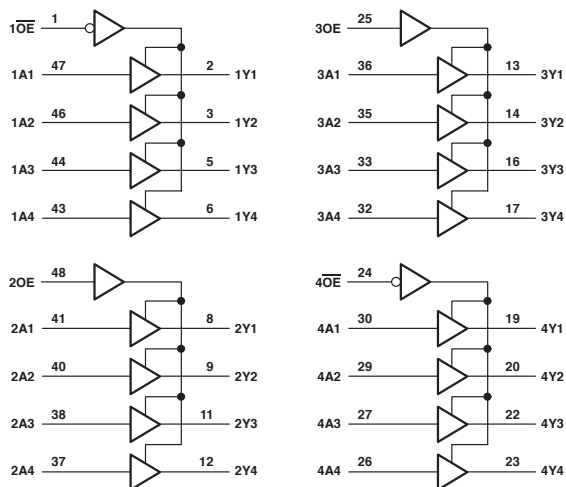
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVT 3V	AC	ACT	AHC	AHCT
t _{PLH}	A	Y	MAX	4.7	3.5	3.5	3.3	5.8	8.5	8.5	10.5
t _{PHL}				4.8	3.5	3.5	3.2	7.1	10.2	8.5	10.5
t _{PZH}	OE	Y	MAX	5.3	4	4	3.7	6.6	9.4	10.5	13
t _{PZL}				7.1	4.4	4.4	3.1	8.1	11.4	10.5	13
t _{PHZ}	OE	Y	MAX	6.1	4.5	4.5	5	8.1	12	10.5	13
t _{PLZ}				5.6	4.2	4.2	4.1	7.3	10.7	10.5	13

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCH 3V	LVCZ 3V	ALVCH 3V
t _{PLH}	A	Y	MAX	4.2	4.2	3.9
t _{PHL}				4.2	4.2	3.9
t _{PZH}	OE	Y	MAX	4.7	4.7	5
t _{PZL}				4.7	4.7	5
t _{PHZ}	OE	Y	MAX	5.9	5.9	4.4
t _{PLZ}				5.9	5.9	4.4

UNIT: ns

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
1OE, 4OE	1A, 4A		1Y, 4Y	
L	H		L	
L	L		H	
H	X		Z	

INPUTS			OUTPUTS	
2OE, 3OE	2A, 3A		2Y, 3Y	
H	H		H	
H	L		L	
L	X		Z	

RECOMMENDED OPERATING CONDITIONS

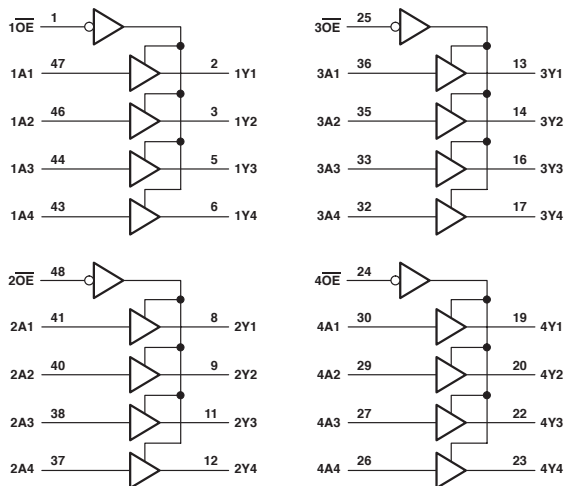
PARAMETER	MAX or MIN	ABT	LVTH 3V	ACT	UNIT
I _{CC}	MAX	34	5	0.08	mA
I _{OH}	MAX	-32	-32	-24	mA
I _{OL}	MAX	64	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ACT
t _{PLH}	A	Y	MAX	3.7	3.5	9.5
t _{PHL}				4.5	3.5	9.1
t _{PZH}	$\overline{0E}$ or OE	Y	MAX	5	4.5	9.4
t _{PZL}				6.9	4.5	10.5
t _{PHZ}	$\overline{0E}$ or OE	Y	MAX	6.2	5.3	11.6
t _{PLZ}				5.6	4.9	10.7

UNIT: ns

Logic Diagram



FUNCTION TABLE
(each buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT	LVC 3V	LVCH 3V	UNIT
I_{CC}	MAX	32	32	5	5	5	0.08	0.08	0.04	0.04	0.02	0.02	mA
I_{OH}	MAX	-32	-32	-32	-32	-32	-24	-24	-8	-8	-24	-24	mA
I_{OL}	MAX	64	64	64	64	64	24	24	8	8	24	24	mA

PARAMETER	MAX or MIN	LVCZ 3V	ALVC 3V	ALVCH 3V	AVC 3V	UNIT
I_{CC}	MAX	0.1	0.04	0.04	0.04	mA
I_{OH}	MAX	-24	-24	-24	-12	mA
I_{OL}	MAX	24	24	24	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALVTH 3V	AC	ACT	AHC
t_{PLH}	A	Y	MAX	3.5	3.5	3.2	3.2	2.4	7.1	9.4	8.5
t_{PHL}				4.1	4.1	3.2	3.2	2.5	7.9	9.5	8.5
t_{PZH}	\overline{OE}	Y	MAX	4.8	4.8	4	4	3.8	7.5	8.9	10.5
t_{PZL}				4.8	4.8	4	4	2.9	9	10.3	10.5
t_{PHZ}	\overline{OE}	Y	MAX	4.8	4.8	4.5	4.5	4.2	8.4	11.3	10.5
t_{PLZ}				4.1	4.1	4.2	4.2	3.6	7.6	10.3	10.5

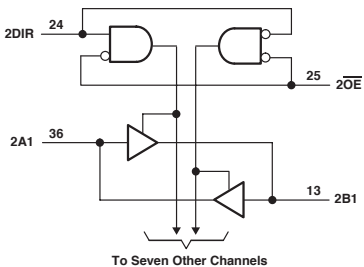
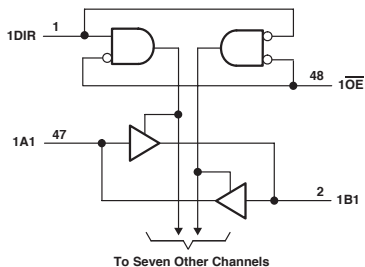
PARAMETER	INPUT	OUTPUT	MAX or MIN	AHCT	LVC 3V	LVCH 3V	LVCZ 3V	ALVC 3V	ALVCH 3V	AVC 3V
t_{PLH}	A	Y	MAX	10.5	4.1	4.1	4.1	3	3	1.7
t_{PHL}				10.5	4.1	4.1	4.1	3	3	1.7
t_{PZH}	\overline{OE}	Y	MAX	13	4.6	4.6	4.6	4.4	4.4	3.5
t_{PZL}				13	4.6	4.6	4.6	4.4	4.4	3.5
t_{PHZ}	\overline{OE}	Y	MAX	13	5.8	5.8	5.8	4.1	4.1	3.5
t_{PLZ}				13	5.8	5.8	5.8	4.1	4.1	3.5

UNIT: ns

16245

16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALVTH 3V	AC	ACT	AHCT	UNIT
I _{CC}	MAX	32	32	5	5	5	0.08	0.08	0.04	mA
I _{OH}	MAX	-32	-32	-32	-32	-32	-24	-24	-8	mA
I _{OL}	MAX	64	64	64	64	64	24	24	8	mA

PARAMETER	MAX or MIN	LVC 3V	LVCH 3V	LVCHR 3V	LVCZ 3V	ALVCH 3V	ALVCH HR 3V	AVC 3V	UNIT
I _{CC}	MAX	0.02	0.02	0.02	0.06	0.04	0.04	0.04	mA
I _{OH}	MAX	-24	-24	-12	-24	-24	-12	-12	mA
I _{OL}	MAX	24	24	12	24	24	12	12	mA

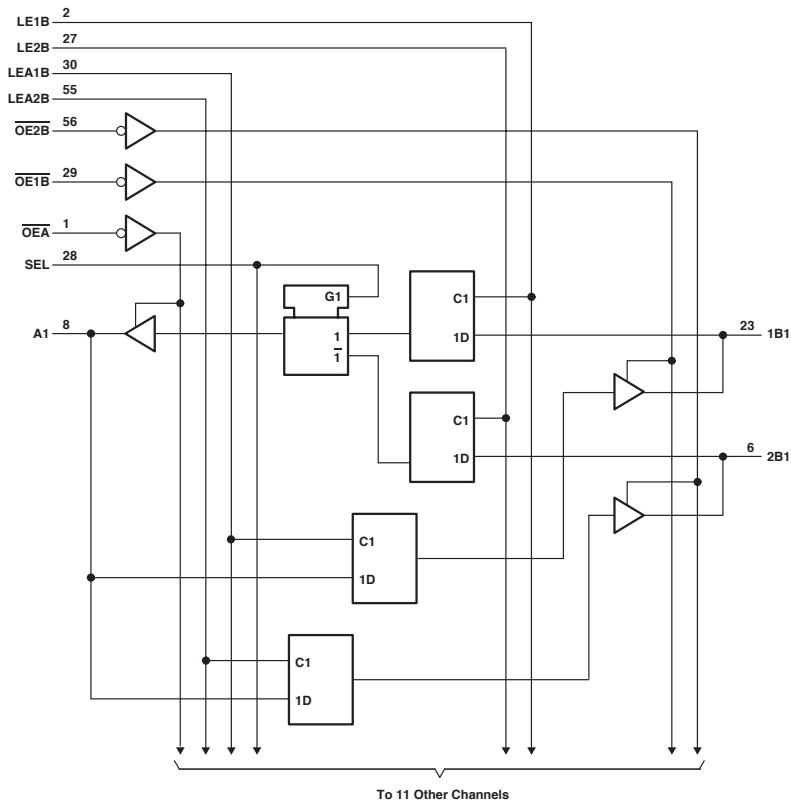
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALVTH 3V	AC	ACT	AHCT
t _{PLH}	A or B	B or A	MAX	3.9	3.9	3.3	3.3	3.1	7.9	10.5	10.5
t _{PHL}				4.2	4.2	3.3	3.3	2.9	8.9	10.2	10.5
t _{PZH}	\overline{OE}	B or A	MAX	6.3	6.3	4.5	4.5	4.2	8.6	10	15
t _{PZL}				6.4	6.4	4.6	4.6	3.5	10.7	11.6	15
t _{PHZ}	\overline{OE}	B or A	MAX	6.3	6.3	5.1	5.1	5.3	9.8	12.6	15
t _{PLZ}				5.2	5.2	5.1	5.1	5	8.7	11.8	15

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 3V	LVCH 3V	LVCHR 3V	LVCZ 3V	ALVCH 3V	ALVCH HR 3V	AVC 3V
t _{PLH}	A or B	B or A	MAX	4	4	4.8	4	3	4.2	1.7
t _{PHL}				4	4	4.8	4	3	4.2	1.7
t _{PZH}	\overline{OE}	B or A	MAX	5.5	5.5	6.3	5.6	4.4	5.6	3.7
t _{PZL}				5.5	5.5	6.3	5.6	4.4	5.6	3.7
t _{PHZ}	\overline{OE}	B or A	MAX	6.6	6.6	7.4	6.6	4.1	5.5	3.9
t _{PLZ}				6.6	6.6	7.4	6.6	4.1	5.5	3.9

UNIT: ns

Logic Diagram



FUNCTION TABLE
B TO A ($\overline{OE}B = H$)

INPUTS						OUTPUT
1B	2B	SEL	LE1B	LE2B	$\overline{OE}A$	A
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A ₀
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A ₀
X	X	X	X	X	H	Z

A TO B ($\overline{OE}A = H$)

INPUTS					OUTPUTS	
1B	LEA1B	LEA2B	$\overline{OE}1B$	$\overline{OE}2B$	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	2B ₀
L	H	L	L	L	L	2B ₀
H	L	H	L	L	1B ₀	H
L	L	H	L	L	1B ₀	L
X	L	L	L	L	1B ₀	2B ₀
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

RECOMMENDED OPERATING CONDITIONS

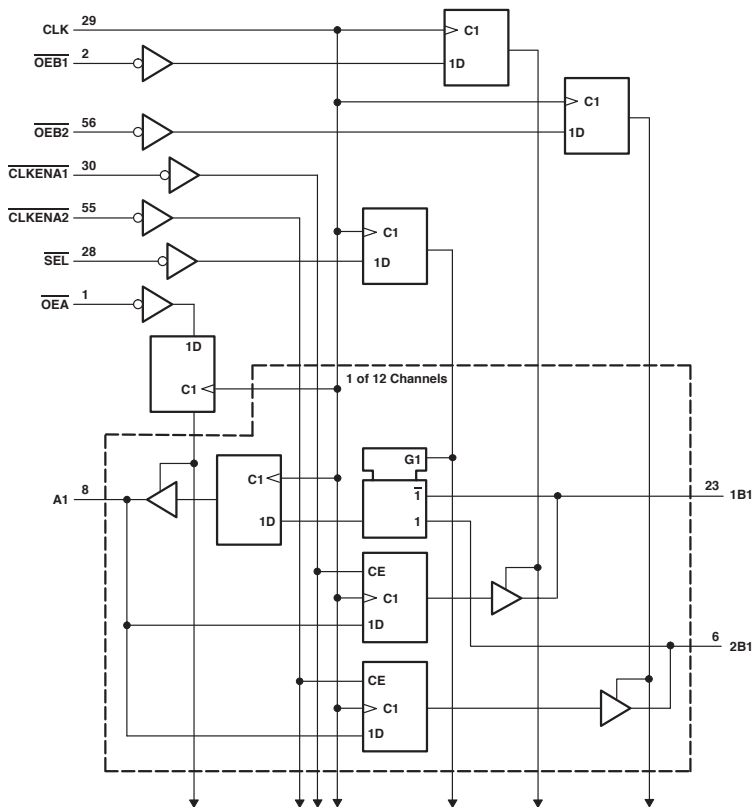
PARAMETER	MAX or MIN	ABTH	ALVCH 3V	UNIT
I _{CC}	MAX	63	0.04	mA
I _{OH}	MAX	-32	-24	mA
I _{OL}	MAX	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH	ALVCH 3V
t _w	Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high		MIN	3.3	3.3
t _{su}	Setup time, data before LE1B, LE2B, LEA1B, or LEA2B		MIN	1.5	1.1
t _h	Hold time, data after LE1B, LE2B, LEA1B, or LEA2B		MIN	1	1.5
t _{PLH}	A or B	B or A	MAX	5.6	4.3
t _{PHL}				5.9	4.3
t _{PLH}	LE	A or B	MAX	5.8	4.4
t _{PHL}				5.3	4.4
t _{PLH}	SEL (B1)	A	MAX	5.3	5.6
	SEL (B2)			6	5.6
t _{PHL}	SEL (B1)			4.4	5.6
	SEL (B2)			5.9	5.6
t _{PZH}	\overline{OE}	A or B	MAX	5.7	5.4
t _{PZL}				5.8	5.4
t _{PHZ}	\overline{OE}	A or B	MAX	6.4	4.6
t _{PLZ}				4.8	4.6

UNIT: ns

Logic Diagram



FUNCTION TABLE
OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	OEA	OEB	A	1B,2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB} = L$)

INPUTS				OUTPUTS	
CLKENA1	CLKENA2	CLK	A	1B	2B
H	H	X	X	1B ₀ †	2B ₀ †
L	X	↑	L	L	X
L	X	↑	H	H	X
X	L	↑	L	X	L
X	L	↑	H	X	H

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEA} = L$)

INPUTS				OUTPUT
CLK	SEL	1B	2B	A
X	H	X	X	A ₀ †
X	L	X	X	A ₀ †
↑	H	H	X	L
↑	H	L	X	H
↑	L	X	L	L
↑	L	X	H	H

† Output level before the indicated steady-state input conditions were established

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	ALVCHR 3V	AVC 3V	UNIT
I _{CC}	MAX	0.04	0.04	0.04	mA
I _{OH}	MAX	-24	-12	-12	mA
I _{OL}	MAX	24	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	ALVCHR 3V	AVC 3V
f _{max}			MIN	135	135	175
t _w Pulse duration, CLK high or low			MIN	3.3	3.3	3.5
t _{su} Setup time	A data before CLK *		MIN	1.7	1	1.9
	B data before CLK *		MIN	1.8	1.1	1.9
	SEL before CLK *		MIN	1.3	1.3	1.3
	CLKENA1 or CLKENA2 before CLK *		MIN	0.9	0.8	1.1
	\overline{OE} before CLK *		MIN	1.3	1.2	1.1
t _h Hold time	A data after CLK *		MIN	0.6	1.2	1
	B data after CLK *		MIN	0.6	1	0.7
	SEL after CLK *		MIN	0.7	1.7	0.4
	CLKENA1 or CLKENA2 after CLK *		MIN	1.1	1.6	1
	\overline{OE} after CLK *		MIN	0.8	1.2	0.3
t _{pd}	CLK	B	MAX	6.2	5.8	3
		A		5	5.2	2.7
t _{en}	CLK	B	MAX	6.1	5.8	3.8
		A		5.9	5.3	3.4
t _{fis}	CLK	B	MAX	6.1	6	3.7
		A		5.6	6	3.4

UNIT f_{max}: MHz other: ns

FUNCTION TABLE
OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	OEA	OEB	A	1B,2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB} = L$)

INPUTS				OUTPUTS	
CLKENA1	CLKENA2	CLK	A	1B	2B
L	H	↑	L	L [†]	2B ₀ [‡]
L	H	↑	H	H [†]	2B ₀ [‡]
L	L	↑	L	L [†]	L
L	L	↑	H	H [†]	H
H	L	↑	L	1B ₀ [‡]	L
H	L	↑	H	1B ₀ [‡]	H
H	H	X	X	1B ₀ [‡]	2B ₀ [‡]

[†] Two CLK edges are needed to propagate data.

[‡] Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEA} = L$)

INPUTS					OUTPUT	
CLKEN1B	CLKEN2B	CLK	SEL	1B	2B	A
H	X	X	H	X	X	A ₀ [‡]
X	H	X	L	X	X	A ₀ [‡]
L	X	↑	H	H	X	L
L	X	↑	H	L	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

[‡] Output level before the indicated steady-state input conditions were established

RECOMMENDED OPERATING CONDITIONS

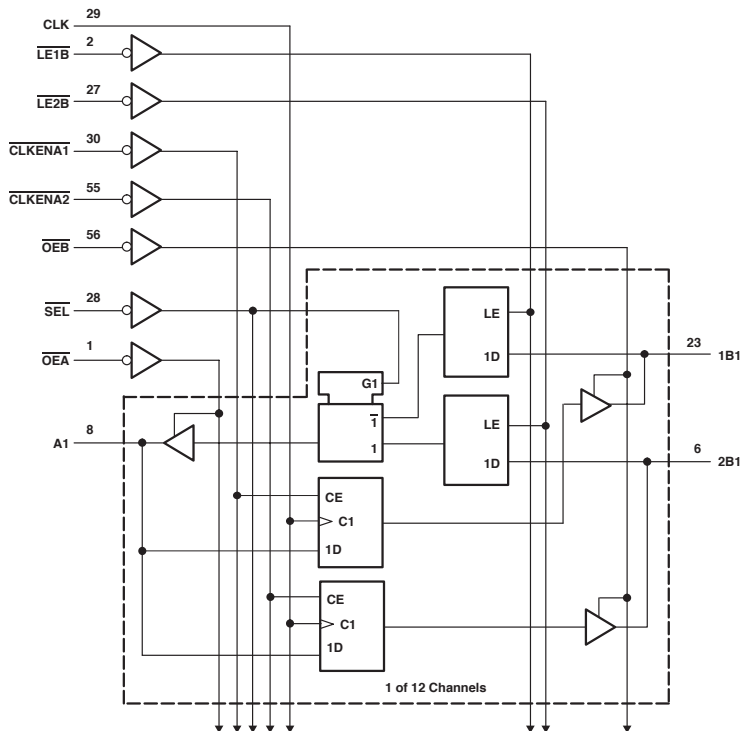
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH}	MAX	-24	mA
I _{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f _{max}			MIN	150
t _w Pulse duration, CLK high or low			MIN	3.3
t _{su} Setup time	A data before CLK *		MIN	3.1
	B data before CLK *		MIN	0.9
	CLKENA1 or CLKENA2 before CLK *		MIN	2.7
	CLKEN1B or CLKEN2B before CLK *		MIN	2.6
	OE before CLK *		MIN	3.2
t _h Hold time	A data after CLK *		MIN	0.2
	B data after CLK *		MIN	1.7
	CLKENA1 or CLKENA2 after CLK *		MIN	0.3
	CLKEN1B or CLKEN2B after CLK *		MIN	0.6
	OE after CLK *		MIN	0.1
t _{pd}	CLK	A or B	MAX	5.1
	SEL	A	MAX	4.7
t _{en}	CLK	A or B	MAX	5.5
				6
t _{dis}	CLK	A or B	MAX	5.8
				5.8

 UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

OUTPUT ENABLE

INPUTS		OUTPUTS	
OEA	OEB	A	1B, 2B
H	X	Z	Z
L	L	Z	Active
L	H	Active	Z
L	L	Active	Active

A-TO-B STORAGE ($\overline{OEB} = L$)

INPUTS				OUTPUTS	
CLKENA1	CLKENA2	CLK	A	1B	2B
H	H	X	X	1B ₀ †	2B ₀ †
L	L	X	†	L	X
L	X	†	H	H	X
X	L	†	L	X	L
X	L	†	H	A ₀	H

B-TO-A STORAGE ($\overline{OEA} = L$)

INPUTS				OUTPUTS	
LE	SEL	1B	2B	A ₀ †	A ₀ †
H	X	X	X	A ₀ †	A ₀ †
H	X	X	X	A ₀ †	A ₀ †
L	H	L	X	L	L
L	H	H	X	L	H
L	L	X	L	L	L
L	L	X	H	L	H

† Output level before the indicated steady-state input conditions were established

RECOMMENDED OPERATING CONDITIONS

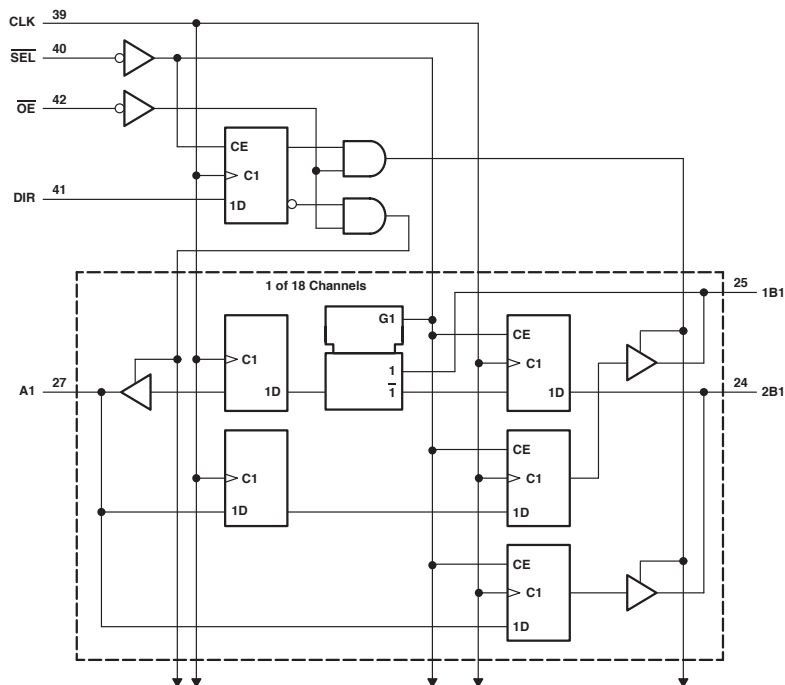
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH}	MAX	-24	mA
I _{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
t _{max}			MIN	130
t _w	Pulse duration, CLK high or low		MIN	3.3
t _{su}	A before CLK *		MIN	1.7
	B before \overline{LE}		MIN	1.3
	CLKEN before CLK *		MIN	1
t _h	A after CLK *		MIN	0.7
	B after \overline{LE}		MIN	1.1
	CLKEN after CLK *		MIN	0.9
t _{pd}	CLK	B	MAX	4.3
	B	A	MAX	4
	\overline{LE}			4.8
	SEL			5.2
t _{en}	\overline{OEB} or \overline{OEA}	B or A	MAX	5.1
t _{dis}	\overline{OEB} or \overline{OEA}	B or A	MAX	4.2

UNIT f_{max}: MHz other: ns

Logic Diagram



FUNCTION TABLE

A-TO-B STORAGE ($\overline{OE} = L$, DIR = H)

INPUTS			OUTPUTS	
SEL	CLK	A	1B	2B
H	X	X	1B ₀ †	2B ₀ †
L	↑	L	L‡	X
L	↑	H	H‡	X

† Output level before the indicated steady-state input conditions were established

‡ Two CLK edges are needed to propagate the data.

B-TO-A STORAGE ($\overline{OE} = L$, DIR = L)

INPUTS				OUTPUT
CLK	SEL	1B	2B	A
↑	H	X	L	L§
↑	H	X	H	H§
↑	L	L	X	L
↑	L	H	X	H

§ Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	\overline{OE}	DIR	A	1B, 2B
↑	H	X	Z	Z
↑	L	L	Z	Active
↑	L	H	Active	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH}	MAX	-24	mA
I _{OL}	MAX	24	mA

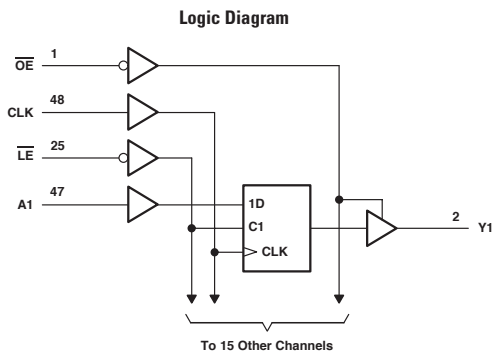
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f _{max}			MIN	150
t _w	Pulse duration, CLK high or low		MIN	3.3
t _{su}	Setup time	A data before CLK *	MIN	2
		B data before CLK *	MIN	1.8
		DIR before CLK *	MIN	1.7
		SEL before CLK *	MIN	1.8
t _h	Hold time	A data after CLK *	MIN	0.7
		B data after CLK *	MIN	0.6
		DIR after CLK *	MIN	0.5
		SEL after CLK *	MIN	0.8
t _{pd}	CLK	A	MAX	5
		B		5.3
t _{en}	\overline{OE}	A	MAX	5.7
		B		7.4
t _{dis}	\overline{OE}	A	MAX	5.7
		B		6.4

UNIT f_{max} : MHz other : ns

16334

16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS



FUNCTION TABLE

INPUTS				OUTPUT
OE	LE	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y _{0f}

↑ Output level before the indicated steady-state input conditions were established

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	AVC 3V	UNIT
I _{CC}	MAX	0.04	0.04	0.04	mA
I _{OH}	MAX	-24	-24	-12	mA
I _{OL}	MAX	24	24	12	mA

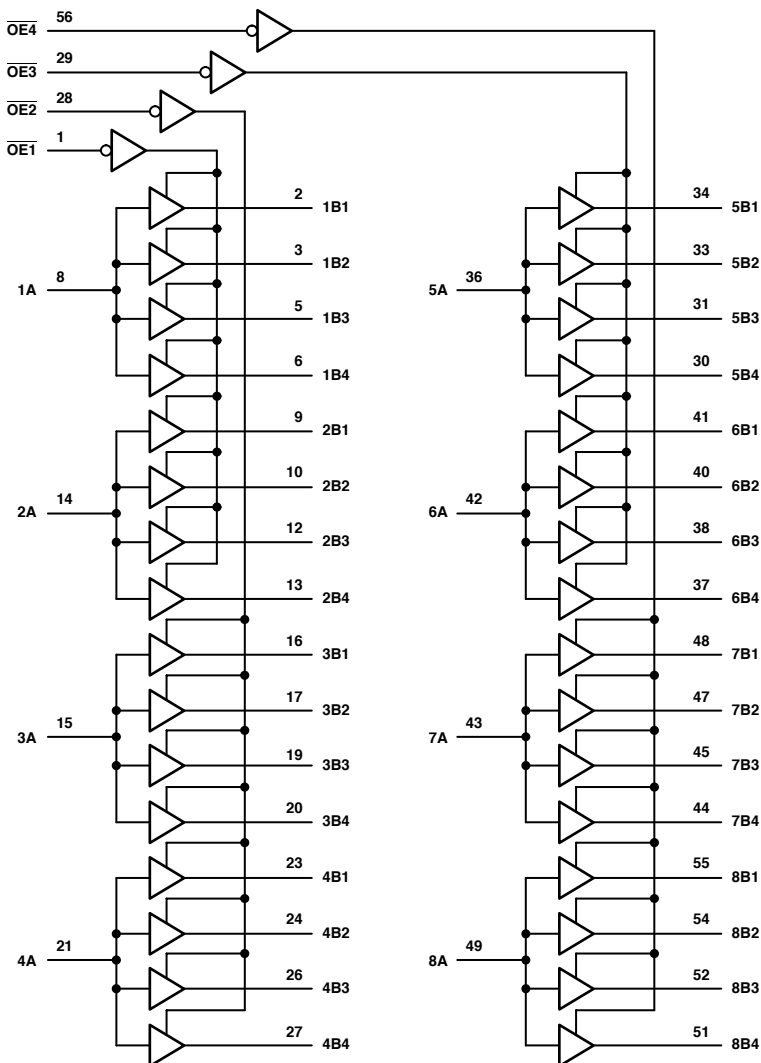
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V	AVC 3V
f _{max}			MIN	150	150	150
t _w Pulse duration	LE low			3.3	3.3	3.3
	CLK high or low		MIN	3.3	3.3	3.3
t _{su} Setup time	Data before CLK *		MIN	1.5	1.5	0.7
	Data before LE * CLK high		MIN	1.3	1.3	0.9
	Data before LE * CLK low		MIN	1.2	1.2	1
t _h Hold time	Data after CLK *		MIN	0.9	0.9	0.7
	Data after LE * CLK high		MIN	1.1	1.1	1.5
	Data after LE * CLK low		MIN	1.1	1.1	1.3
t _{pd}	A		MAX	3.3	3.3	2.5
	LE	Y		4.4	4.4	4
	CLK		MAX	4.1	4.1	3.1
t _{en}	OE	Y		4.6	4.6	6.2
t _{dis}	OE	Y	MAX	4.4	4.4	5.3

UNIT f_{max} : MHz other : ns

1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
OE	A	Bn
L	H	H
L	L	L
H	H	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH}	MAX	-24	mA
I _{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

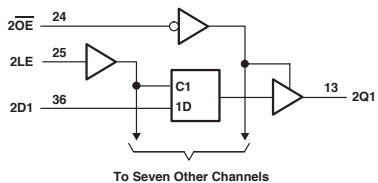
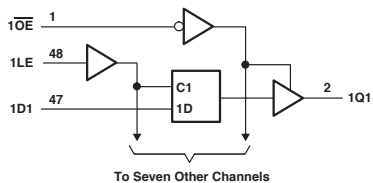
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
t _{PLH}	A	B	MAX	4
t _{PHL}				4
t _{PZH}	\overline{OE}	B	MAX	5.1
t _{PZL}				5.1
t _{PHZ}	\overline{OE}	B	MAX	4
t _{PLZ}				4

UNIT: ns

16373

16-BIT TRANSPARENT LATCHES WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each latch)

INPUTS			OUTPUT
\overline{OE}	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT	LVC 3V	LVCH 3V	ALVCH 3V	AVC 3V	UNIT
I _{CC}	MAX	85	5	5	0.08	0.08	0.04	0.04	0.02	0.02	0.04	0.04	mA
I _{OH}	MAX	-32	-32	-32	-24	-24	-8	-8	-24	-24	-24	-12	mA
I _{OL}	MAX	64	64	64	24	24	8	8	24	24	24	12	mA

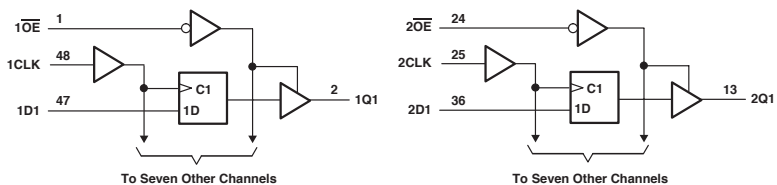
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT
t _w Pulse duration, LE high or low			MIN	3.3	3	1.5	4	1	5	6.5
t _{su} Setup time	Data before LE , data high		MIN	1.5	1	1.4	1.5	1	4	1.5
	Data before LE , data low		MIN	1.5	1	0.9	1.5	1	4	1.5
t _h Hold time	Data after LE , data high		MIN	1	1	0.9	2.4	5	1	3.5
	Data after LE , data low		MIN	1	1	1.4	2.4	5	1	3.5
t _{PLH}	D	Q	MAX	6.3	3.8	3.1	9.7	11.1	10.5	10.5
				6.2	3.6	3.3	10.1	12.3	10.5	10.5
t _{PHL}	LE	Q	MAX	6.7	4.3	3.3	11.9	12.8	10.5	10.5
				6.1	4	3.5	10.9	12.2	10.5	10.5
t _{PZH}	\overline{OE}	Q	MAX	6.1	4.3	4	10.8	12.1	11.5	11.5
				5.6	4.3	3.4	12.8	14.2	11.5	11.5
t _{PHZ}	\overline{OE}	Q	MAX	8.1	5	4.9	8.8	10.7	11.5	12
				6.5	4.7	4.5	8.1	9.4	11.5	12

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 3V	LVCH 3V	ALVCH 3V	AVC 3V
t _w Pulse duration, LE high or low			MIN	3.3	3.3	3.3	1.8
t _{su} Setup time	Data before LE , data high		MIN	1.7	1.7	1.1	0.8
	Data before LE , data low		MIN	1.7	1.7	1.1	0.8
t _h Hold time	Data after LE , data high		MIN	1.2	1.2	1.4	1
	Data after LE , data low		MIN	1.2	1.2	1.4	1
t _{PLH}	D	Q	MAX	4.2	4.2	3.6	2.8
				4.2	4.2	3.6	2.8
t _{PHL}	LE	Q	MAX	4.6	4.6	3.9	3.2
				4.6	4.6	3.9	3.2
t _{PZH}	\overline{OE}	Q	MAX	4.7	4.7	4.7	3.4
				4.7	4.7	4.7	3.4
t _{PHZ}	\overline{OE}	Q	MAX	5.9	5.9	4.1	3.9
				5.9	5.9	4.1	3.9

UNIT: ns

Logic Diagram



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q_D
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT	LVC 3V	LVCH 3V	ALVCH 3V	AVC 3V	UNIT
I _{CC}	MAX	72	5	5	0.08	0.08	0.04	0.04	0.02	0.02	0.04	0.04	mA
I _{OH}	MAX	-32	-32	-32	-24	-24	-8	-8	-24	-24	-24	-12	mA
I _{OL}	MAX	64	64	64	24	24	8	8	24	24	24	12	mA

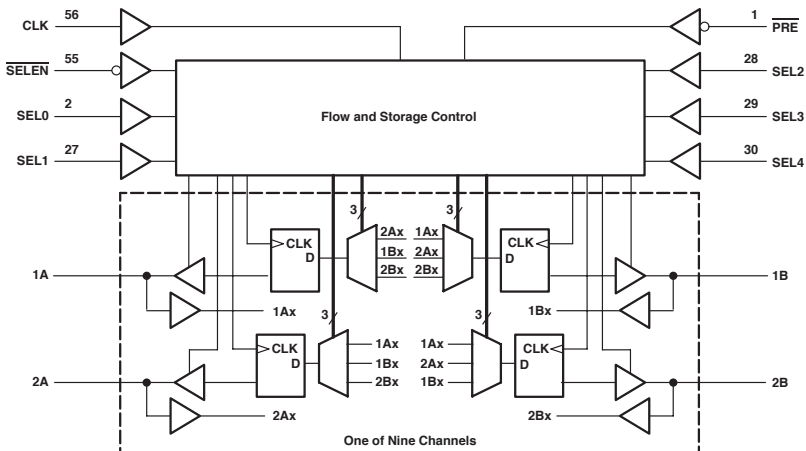
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVTH 3V	AC	ACT	AHC	AHCT
f _{max}			MIN	150	160	250	100	65	110	110
t _w Pulse duration	CLK high		MIN	3.3	3	1.5	5	7.5	5	6.5
	CLK low			3.3	3	1.5	5	4.5	5	6.5
t _{su} Setup time	Data before CLK ↑, data high		MIN	1.1	1.8	1	5	4.5	3	2.5
	Data before CLK ↑, data low			1.1	1.8	1.5	5	4.5	3	2.5
t _h Hold time	Data after CLK ↑, data high		MIN	1.3	0.8	0.5	0	6.5	2	2.5
	Data after CLK ↑, data low			1.3	0.8	1	0	6.5	2	2.5
t _{PLH}	CLK	Q	MAX	6.2	4.5	3.2	10.8	12.4	11.5	11.5
t _{PHL}				5.9	4	3.2	10.6	12.2	11.5	11.5
t _{PZH}	\overline{OE}	Q	MAX	5.6	4.5	3.8	10.2	11.9	11.5	11.5
t _{PZL}				5.3	4.4	3.3	12.1	13.4	11.5	11.5
t _{PHZ}	\overline{OE}	Q	MAX	8.2	5	4.6	8.2	10.4	11.5	12
t _{PLZ}				6.6	4.6	4.2	7.9	9.8	11.5	12

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVC 3V	LVCH 3V	ALVCH 3V	AVC 3V
f _{max}			MIN	150	150	150	200
t _w Pulse duration	CLK high		MIN	3.3	3.3	3.3	2.5
	CLK low			3.3	3.3	3.3	2.5
t _{su} Setup time	Data before CLK ↑, data high		MIN	1.9	1.9	1.9	1.4
	Data before CLK ↑, data low			1.9	1.9	1.9	1.4
t _h Hold time	Data after CLK ↑, data high		MIN	1.9	1.1	0.5	1.1
	Data after CLK ↑, data low			1.9	1.1	0.5	1.1
t _{PLH}	CLK	Q	MAX	4.5	4.5	4.2	3.3
t _{PHL}				4.5	4.5	4.2	3.3
t _{PZH}	\overline{OE}	Q	MAX	4.6	4.6	4.8	3.4
t _{PZL}				4.6	4.6	4.8	3.4
t _{PHZ}	\overline{OE}	Q	MAX	5.5	5.5	4.3	3.9
t _{PLZ}				5.5	5.5	4.3	3.9

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
CLK	SEND PORT	RECEIVE PORT
X	X	B ₀ †
X	L	L
X	H	H
↑	L	L
↑	H	H
H	X	B ₀ †
L	X	B ₀ †

† Output level before the indicated steady-state input conditions were established

DATA-FLOW CONTROL

INPUTS								DATA FLOW
PRE	SELEN	CLK	SEL0	SEL1	SEL2	SEL3	SEL4	
H	X	X	X	X	X	X	X	All outputs disabled
L	H	↑	X	X	X	X	X	No change
L	L	↑	0	0	0	0	0	None, all I/Os off
L	L	↑	0	0	0	0	1	Not used
L	L	↑	0	0	0	1	0	Not used
L	L	↑	0	0	0	1	1	Not used
L	L	↑	0	0	1	0	0	Not used
L	L	↑	0	0	1	0	1	Not used
L	L	↑	0	0	1	1	0	Not used
L	L	↑	0	0	1	1	1	Not used
L	L	↑	0	1	0	0	0	2A to 1A and 1B to 2B
L	L	↑	0	1	0	0	1	2A to 1A
L	L	↑	0	1	0	1	0	2B to 1B
L	L	↑	0	1	0	1	1	2A to 1A and 2B to 1B
L	L	↑	0	1	1	0	0	1A to 2A and 1B to 2B
L	L	↑	0	1	1	0	1	1A to 2A
L	L	↑	0	1	1	1	0	1B to 2B
L	L	↑	0	1	1	1	1	1A to 2A and 2B to 1B
L	L	↑	1	0	0	0	0	1A to 1B and 2B to 2A
L	L	↑	1	0	0	0	1	1A to 1B
L	L	↑	1	0	0	1	0	2A to 2B
L	L	↑	1	0	0	1	1	1A to 1B and 2A to 2B
L	L	↑	1	0	1	0	0	1B to 1A and 2A to 2B
L	L	↑	1	0	1	0	1	1B to 1A
L	L	↑	1	0	1	1	0	2B to 2A
L	L	↑	1	0	1	1	1	1B to 1A and 2B to 2A
L	L	↑	1	1	0	0	0	2B to 1A and 2A to 1B
L	L	↑	1	1	0	0	1	1B to 2A
L	L	↑	1	1	0	1	0	2B to 1A
L	L	↑	1	1	0	1	1	2B to 1A and 1B to 2A
L	L	↑	1	1	1	0	0	1A to 2B and 1B to 2A
L	L	↑	1	1	1	0	1	1A to 2B
L	L	↑	1	1	1	1	0	2A to 1B
L	L	↑	1	1	1	1	1	1A to 2B and 2A to 1B

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	ALVCR 3V	UNIT
I _{CC}	MAX	0.04	0.04	mA
I _{OH}	MAX	-24	-12	mA
I _{OL}	MAX	24	12	mA

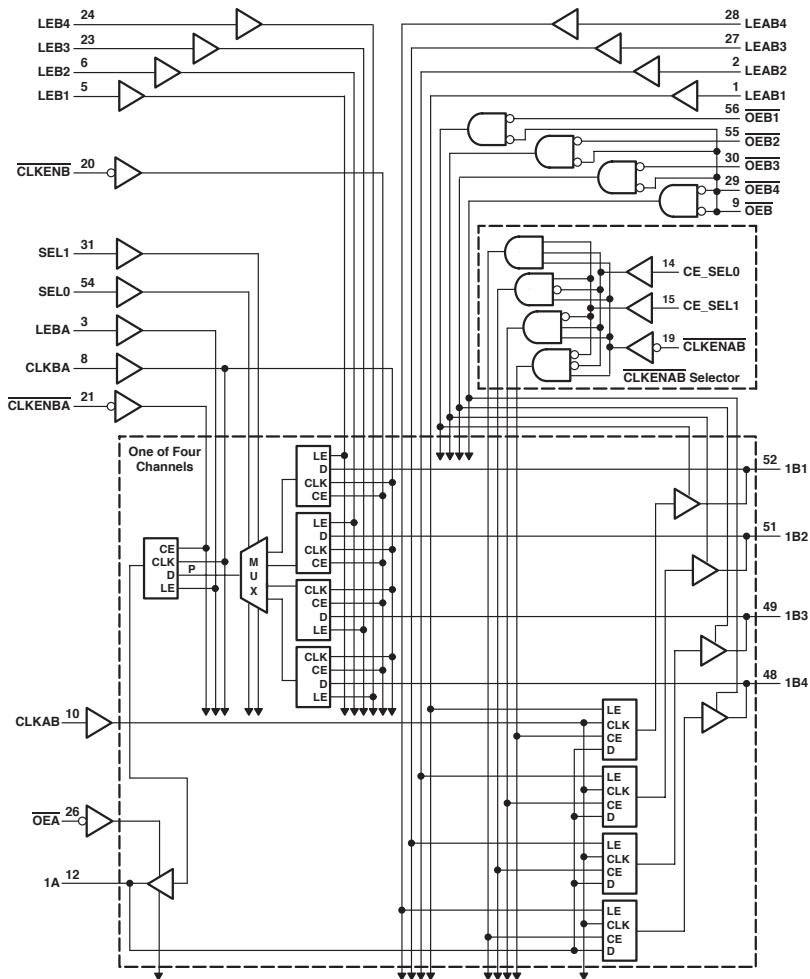
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	ALVCR 3V
f _{max}			MIN	120	120
t _w Pulse duration, CLK high or low			MIN	3	3
t _{su} Setup time	A or B data before CLK *		MIN	1.4	1.4
	SEL before CLK *		MIN	3.5	3.5
	SELEN before CLK *		MIN	1.8	1.8
	PRE before CLK *		MIN	0.7	0.7
t _h Hold time	A or B data after CLK *		MIN	1	1
	SEL after CLK *		MIN	0	0
	SELEN after CLK *		MIN	0.8	0.8
t _{pd}	CLK	A or B	MAX	5.1	6.2
	CLK	A or B	MAX	5.7	6.8
t _{ris}	PRE	A or B	MAX	5.7	6.1
				6.1	6.4

UNIT f_{max}: MHz other: ns

4-TO-1 MULTIPLEXED/DEMULTIPLEXED TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
A-TO-B OUTPUT ENABLE

INPUTS		OUTPUT
OEB	OEBn	Bn
H	H	Z
H	L	Z
L	H	Z
L	L	Active

Tn = 1, 2, 3, 4

A-TO-B OUTPUT ENABLE
 (assuming OEB = L, OEBn = L) ‡

INPUTS								OUTPUTS			
CLKENAB	CE_SEL1	CE_SELO	CLKAB	LEAB1	LEAB2	LEAB3	LEAB4	B1	B2	B3	B4
X	X	X	H or L	H	L	L	L	A	A ₀	A ₀	A ₀
X	X	X	H or L	L	H	L	L	A	A	A	A ₀
L	X	X	L	L	L	L	L	A ₀	A ₀	A ₀	A ₀
L	L	L	†	L	L	L	L	A	A ₀	A ₀	A ₀
L	L	H	†	L	L	L	L	A ₀	A ₀	A ₀	A ₀
L	H	L	†	L	L	L	L	A ₀	A ₀	A ₀	A ₀
L	H	H	†	L	L	L	L	A ₀	A ₀	A ₀	A ₀
H	X	X	†	L	L	L	L	A ₀	A ₀	A ₀	A ₀

B-TO-A STORAGE

(after point P)

INPUTS							P
CLKENB	CLKBA	LEB1	LEB2	LEB3	LEB4	SEL1	SELO
X	X	H	L	L	L	L	L
X	X	L	H	L	L	L	H
X	X	L	L	H	L	H	L
X	X	L	L	L	H	H	H
L	†	L	L	L	L	L	L
L	†	L	L	L	L	L	L
L	†	L	L	L	L	L	L
L	†	L	L	L	L	L	L
L	†	L	L	L	L	L	L
L	†	L	L	L	L	L	L
L	†	L	L	L	L	L	L

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE

(after point P)

INPUTS						OUTPUT
CLKENBA	CLKBA	LEBA	OEA	B		A
X	X	X	H	X		Z
X	X	H	L	L		L
X	X	H	L	H		H
H	X	L	L	X		A ₀ †
L	†	L	L	L		L
L	†	L	L	H		H
L	L	L	L	X		A ₀ †

RECOMMENDED OPERATING CONDITIONS

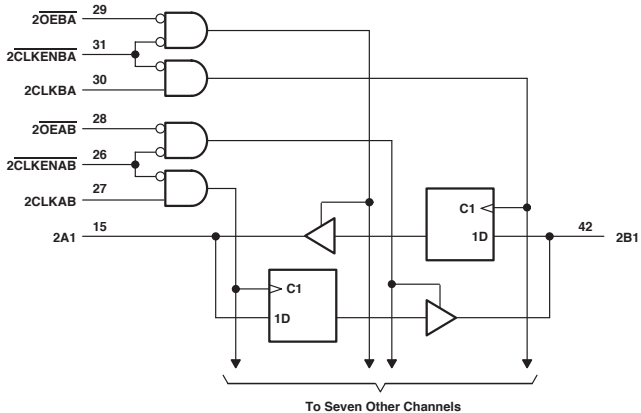
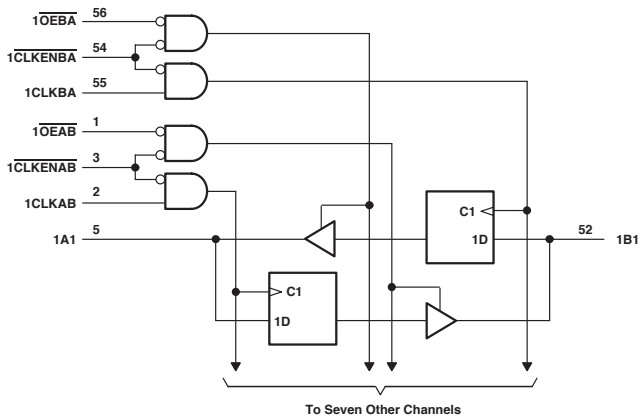
PARAMETER	MAX or MIN	ABTH	UNIT
I _{CC}	MAX	32	mA
I _{OH}	MAX	-32	mA
I _{OL}	MAX	64	mA

SWITCHING CHARACTERISTICS

PARAMETER		MAX or MIN	ABTH	PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH	
t _{max}		MIN	160	EPHL	B	A	MAX	6.5	
		MIN	3.8	EPHL				6.5	
t _w Pulse duration	CLKAB high or low	MIN	3.8	EPZH	OEA	A	MAX	5.6	
	CLKBA high or low	MIN	4.5	EPZH				5.2	
	LEAB1, 2, 3 or 4 high	MIN	2.2	EPZH				5.9	
	LEBA high	MIN	2.1	EPZH				6.5	
	LEB1, 2, 3 or 4 high	MIN	2.4	EPZH				6.5	
t _{su} Setup time	Before CLKAB *	A bus	MIN	2.5	A	B	MAX	5.7	
		CE_SELO/1	MIN	3.2				5.7	
		CLKENAB	MIN	3.2				6.4	
	Before LEAB1, 2, 3, or 4, A bus	A bus	MIN	3.6	OEB	B	MAX	6.3	
		B bus	MIN	3.8				7	
		CLKENB	MIN	2.3				6.1	
	Before CLKBA *	CLKENBA	MIN	2.5	OEB1, 2, 3, 4	B	MAX	5.8	
		LEB1, 2, 3 or 4	MIN	4.3				5.6	
		SELO/1	MIN	4.5				6.1	
	Before LEB1, 2, 3, or 4, B bus	B bus	MIN	3.2	OEB1, 2, 3, 4	B	MAX	5.3	
		B bus	MIN	4				7.4	
		LEB1, 2, 3 or 4	MIN	4.4				7.7	
	t _h Hold time	Before CLKBA *	SELO/1	MIN	4.3	CLKBA	A	MAX	6.2
			A bus	MIN	0.5				5.9
			CE_SELO/1	MIN	1.1				5.6
after CLKAB *		CLKENAB	MIN	0.5	LEBA	A	MAX	5.3	
		A bus	MIN	1.2				5.8	
		B bus	MIN	1.3				5.6	
after CLKBA *		CLKENB	MIN	1	LEAB1, 2, 3, 4	B	MAX	7.2	
		CLKENBA	MIN	1				6.8	
		SELO/1	MIN	0				7.5	
after LEB1, 2, 3, or 4, B bus		B bus	MIN	1.5	SEL	A	MAX	6.9	
		B bus	MIN	0.4					
		SELO/1	MIN	0.1					

 UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
CLKENAB	CLKAB	OEAB	A	B
H	X	X	X	Z
X	X	X	H	Z
L	L	L	X	B ₀ †
L	†	L	L	L
L	†	L	H	H

† A-to-B data flow is shown: B-to-A flow is similar but uses CLKENBA, CLKBA, and OEBA.

‡ Output level before the indicated steady-state input conditions were established.

RECOMMENDED OPERATING CONDITIONS

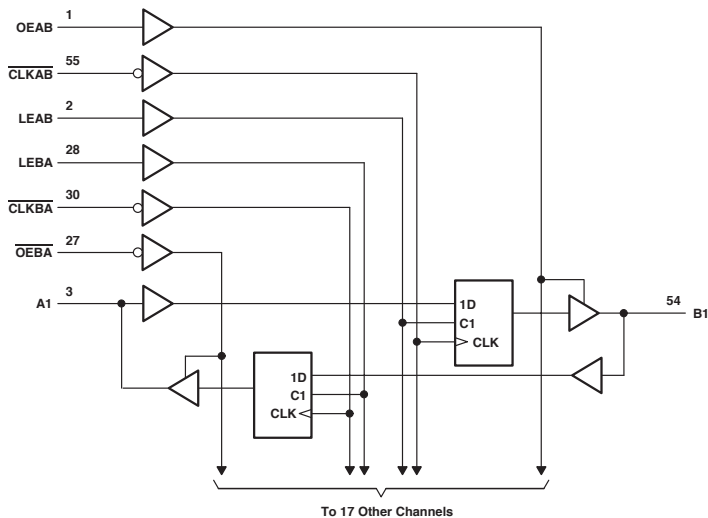
PARAMETER	MAX or MIN	ABT	ACT	UNIT
I _{CC}	MAX	35	0.08	mA
I _{DH}	MAX	-32	-24	mA
I _{OL}	MAX	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT
t _{max}			MIN	150	55
t _w Pulse duration, CLKAB or CLKBA high			MIN	3.3	4
t _w Pulse duration, CLKAB or CLKBA low				3.3	8.5
t _{su} Setup time, data before CLKAB ' or CLKBA '			MIN	4	6
t _h Hold time, data after CLKAB ' or CLKBA '			MIN	1	1
t _{PLH}	CLK	A or B	MAX	4.9	11.8
t _{PHL}				4.9	11.7
t _{PZH}	\overline{OE}	A or B	MAX	4.9	11.9
t _{PZL}				6.8	13.4
t _{PHZ}	\overline{OE}	A or B	MAX	5.5	9.9
t _{PLZ}				5.3	9.5
t _{PZH}	\overline{CLKEN}	A or B	MAX	5.7	12.5
t _{PZL}				7.2	14.3
t _{PHZ}	\overline{CLKEN}	A or B	MAX	5.8	11.2
t _{PLZ}				5.4	10.9

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT	
OEAB	LEAB	CLKAB	A	B	Z
L	X	X	X		Z
H	H	X	L		L
H	H	X	H		H
H	L	↓	L		L
H	L	↓	H		H
H	L	H	X		B ₀ †
H	L	L	X		B ₀ ‡

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVCH 3V	UNIT
I _{CC}	MAX	36	5	0.04	mA
I _{DH}	MAX	-32	-32	-24	mA
I _{OL}	MAX	64	64	24	mA

SWITCHING CHARACTERISTICS

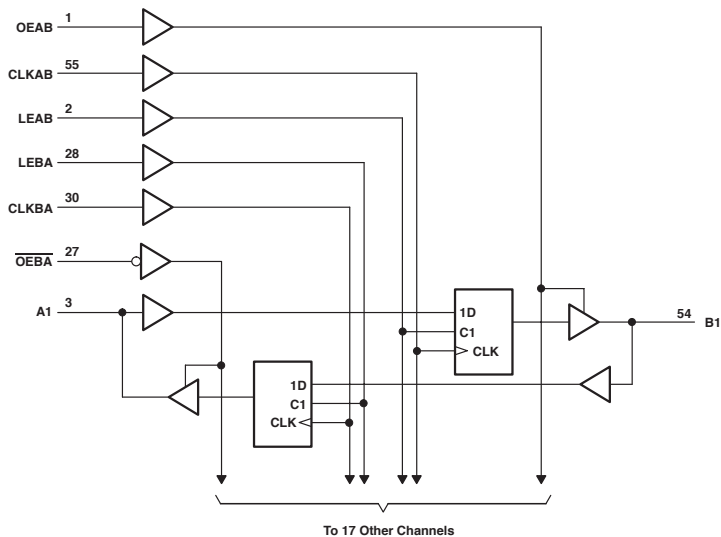
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVCH 3V
t _{max}			MIN	150	150	150
t _w Pulse duration	LEAB or LEBA high		MIN	2.5	3.3	3.3
	CLKAB or CLKBA high or low			3	3.3	3.3
t _{su} Setup time	A before CLKAB,		MIN	3	2.9	1.3
	B before CLKAB,			3	2.9	1.3
	A before LEAB, or LEBA, CLK high			1	1.4	1
	A before LEAB, or LEBA, CLK low			2.5	2.9	1.4
t _h Hold time	A after CLKAB, or B after CLKBA,		MIN	0	0.4	1.3
	A after LEAB, or B after LEBA, high			2	1.6	1.5
	A after LEAB, or B after LEBA, low			2	1.6	1.2
t _{PLH}	A or B	B or A	MAX	4	3.7	3.9
t _{PHL}				4.9	3.7	3.9
t _{PZH}	LEAB or LEBA	B or A	MAX	5	5.1	4.7
t _{PZL}				5	5.1	4.7
t _{PHZ}	CLKAB or CLKBA	B or A	MAX	5.3	5	5.5
t _{PLZ}				5.3	5	5.5
t _{PZH}	OEAB	B	MAX	5.1	4.8	4.6
t _{PZL}				5.4	4.8	4.6
t _{PHZ}	OEAB	B	MAX	6.5	5.8	5
t _{PLZ}				5.4	5.8	5
t _{PZH}	OEBA	A	MAX	5.1	4.8	5.2
t _{PZL}				5.4	4.8	5.2
t _{PHZ}	OEBA	A	MAX	6.5	5.8	4.3
t _{PLZ}				5.4	5.8	4.3

UNIT f_{max} : MHz other : ns

16501

18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	†	L	L
H	L	†	H	H
H	L	H	X	B ₀ ‡
H	L	L	X	B ₀ §

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

RECOMMENDED OPERATING CONDITIONS

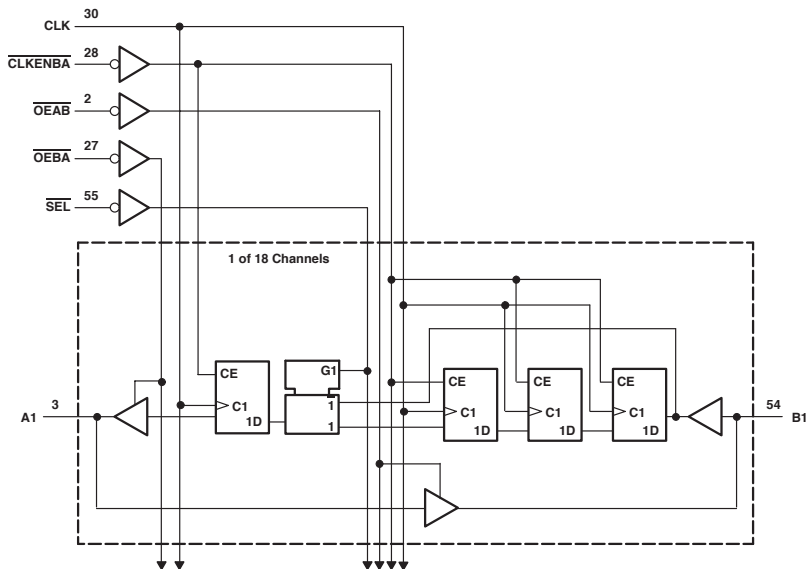
PARAMETER	MAX or MIN	ABT	LVTH 3V	ALVCH 3V	UNIT
I _{CC}	MAX	76	5	0.04	mA
I _{DH}	MAX	-32	-32	-24	mA
I _{OL}	MAX	64	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ALVCH 3V
f _{max}			MIN	105	150	150
t _w Pulse duration	LEAB or LEBA high		MIN	3.3	3.3	3.3
	CLKAB or CLKBA high or low		MIN	4.7	3.3	3.3
t _{su} Setup time	A before CLKAB *		MIN	3.5	2.1	1.7
	B before CLKBA *		MIN	3.5	2.1	1.7
	A before LEAB , or LEBA , CLK high		MIN	4	2.4	1.5
	A before LEAB , or LEBA , CLK low		MIN	1.5	1.4	1
t _h Hold time	A after CLKAB * or B after CLKBA *		MIN	1	1	0.7
	A after LEAB , or B after LEBA ,		MIN	2.5	1.7	1.4
†P _{LH}	A or B	B or A	MAX	3.7	3.7	3.9
†P _{HL}				4	3.7	3.9
†P _{ZH}	LEAB or LEBA	B or A	MAX	5.1	5.1	4.6
†P _{ZL}				4.4	5.1	4.6
†P _{HZ}	CLKAB or CLKBA	B or A	MAX	5	5.1	4.9
†P _{LZ}				4.4	5.1	4.9
†P _{ZH}	OEAB	B	MAX	4.7	4.8	4.6
†P _{ZL}				6.5	4.8	4.6
†P _{HZ}	OEAB	B	MAX	5.8	5.8	5
†P _{LZ}				4.9	5.8	5
†P _{ZH}	OEBA	A	MAX	4.7	4.8	5
†P _{ZL}				6.5	4.8	5
†P _{HZ}	OEBA	A	MAX	5.8	5.8	4.2
†P _{LZ}				4.9	5.8	4.2

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE
B-TO-A STORAGE ($\overline{OEBA} = L$)

CLKENBA	INPUTS			B	OUTPUT A
	CLK	SEL			
H	X	X	X		Ag†
L	†	H	L		L
L	†	H	H		H
L	†	L	L		L‡
L	†	L	H		H‡

† Output level before the indicated steady-state input conditions were established

‡ Four positive CLK edges are needed to propagate data from B to A when SEL is low.

RECOMMENDED OPERATING CONDITIONS

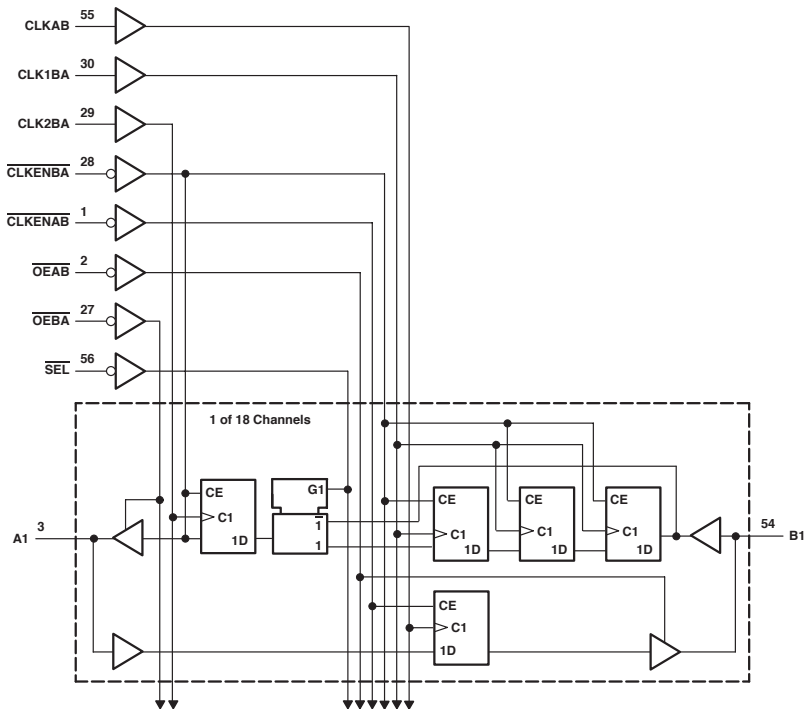
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
Icc	MAX	0.04	mA
Ioh	MAX	-24	mA
Iol	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
fmax			MIN	150
tw	Pulse duration, CLK high or low		MIN	3
tsu	Setup time	B data before CLK *	MIN	1.1
		SEL before CLK *	MIN	2.1
		CLKENBA before CLK *	MIN	2
th	Hold time	B data after CLK *	MIN	1.2
		SEL after CLK *	MIN	0.8
		CLKENBA after CLK *	MIN	0.3
tpd	A	B	MAX	3.2
	CLK	A		5.2
ten	\overline{OEAB} or \overline{OEBA}	A or B	MAX	5.1
tfst	\overline{OEAB} or \overline{OEBA}	A or B		4.9

UNIT fmax : MHz other : ns

Logic Diagram



FUNCTION TABLE

A-TO-B STORAGE ($\overline{OEAB} = L$)

INPUTS			OUTPUT
CLKENAB	CLKAB	A	B
H	X	X	B ₀ †
L	↑	L	L
L	↑	H	H

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($\overline{OEBA} = L$)

INPUTS					OUTPUT
CLKENA	CLK2BA	CLK1BA	SEL	B	A
H	X	X	X	X	A ₀ †
L	↑	X	H	L	L
L	↑	X	H	H	H
L	↑	↑	L	L	L‡
L	↑	↑	L	H	H‡

† Output level before the indicated steady-state input conditions were established

‡ Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when SEL is low.

RECOMMENDED OPERATING CONDITIONS

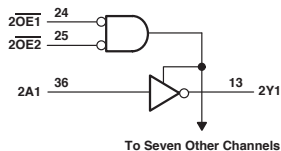
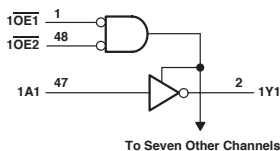
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH}	MAX	-24	mA
I _{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f _{max}			MIN	150
t _w Pulse duration, CLK high or low			MIN	3
t _{su} Setup time	A data before CLKAB *		MIN	1.3
	B data before CLK2BA *		MIN	1.7
	B data before CLK1BA *		MIN	1.1
	SEL before CLK2BA *		MIN	3.3
	CLKENAB before CLKAB *		MIN	1.6
	CLKENBA before CLK1BA *		MIN	2.1
t _h Hold time	CLKENBA before CLK2BA *		MIN	2.2
	A data after CLKAB *		MIN	0.9
	B data after CLK2BA *		MIN	0.6
	B data after CLK1BA *		MIN	1
	SEL after CLK2BA *		MIN	0.1
	CLKENAB after CLKAB *		MIN	0.3
t _{dis}	CLKENBA after CLK1BA *		MIN	0.1
	CLKENBA after CLK2BA *		MIN	0
t _{pd}	CLKAB or CLK2BA	A or B		4.2
t _{en}	\overline{OEAB} or \overline{OEBA}	A or B	MAX	5.1
t _{dis}	\overline{OEAB} or \overline{OEBA}	A or B		4.9

UNIT f_{max}: MHz other: ns

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	H
L	L	H	L
H	X	X	Z
X	H	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	AHC	AHCT	LVCH 3V	UNIT
I _{CC}	MAX	34	0.08	0.04	0.04	0.02	mA
I _{OH}	MAX	-32	-24	-8	-8	-24	mA
I _{OL}	MAX	64	24	8	8	24	mA

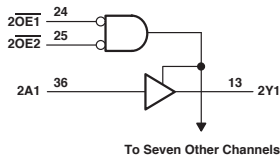
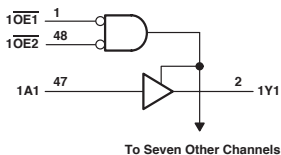
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	AHC	AHCT	LVCH 3V
t _{PLH}	A	Y	MAX	4.1	7.5	8.5	10.5	3.7
t _{PHL}				4.3	9.5	8.5	10.5	3.7
t _{PZH}	\overline{OE}	Y	MAX	5.1	8.9	10.5	13	4.8
t _{PZL}				5.9	10.5	10.5	13	4.8
t _{PHZ}	\overline{OE}	Y	MAX	5.7	11.9	10.5	13	5.9
t _{PLZ}				4.7	11.1	10.5	13	5.9

UNIT: ns

16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

RECOMMENDED OPERATING CONDITIONS

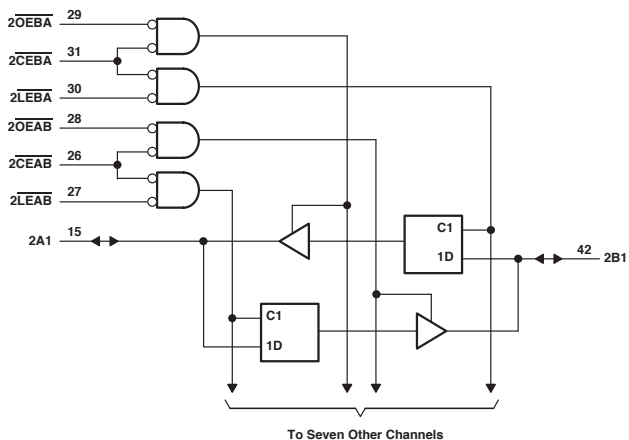
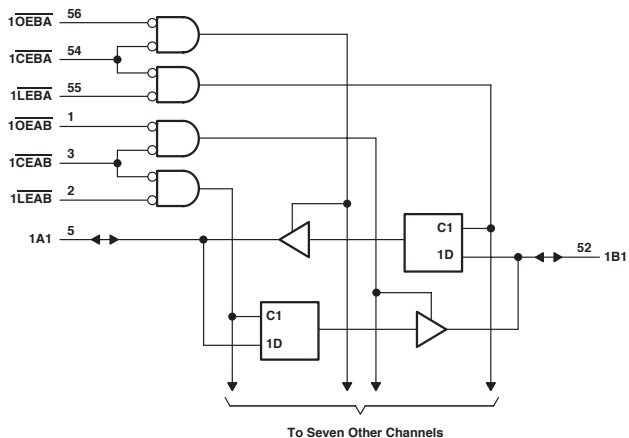
PARAMETER	MAX or MIN	ABT	LVTH 3V	ACT	AHC	AHCT	LVCH 3V	UNIT
I _{CC}	MAX	34	5	0.08	0.04	0.04	0.02	mA
I _{DH}	MAX	-32	-32	-24	-8	-8	-24	mA
I _{OL}	MAX	64	64	24	8	8	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	ACT	AHC	AHCT	LVCH 3V
t _{PLH}	A	Y	MAX	3.4	3.5	9	8.5	10.5	4.2
t _{PHL}				4.2	3.5	9.2	8.5	10.5	4.2
t _{PZH}	OE	Y	MAX	5.2	4.6	9.7	10.5	13	5.6
t _{PZL}				6	4.6	11	10.5	13	5.6
t _{PHZ}	OE	Y	MAX	5.4	5.9	11.3	10.5	13	6.8
t _{PLZ}				4.3	5.4	10.7	10.5	13	6.8

UNIT: ns

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS				OUTPUT
OEAB	LEAB	OEAB	A	B
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B ₀ [†]
L	L	L	X	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow control is the same except that it uses CEBA, LEBA, and OEBA.

‡ Output level before the indicated steady-state input conditions were established.

RECOMMENDED OPERATING CONDITIONS

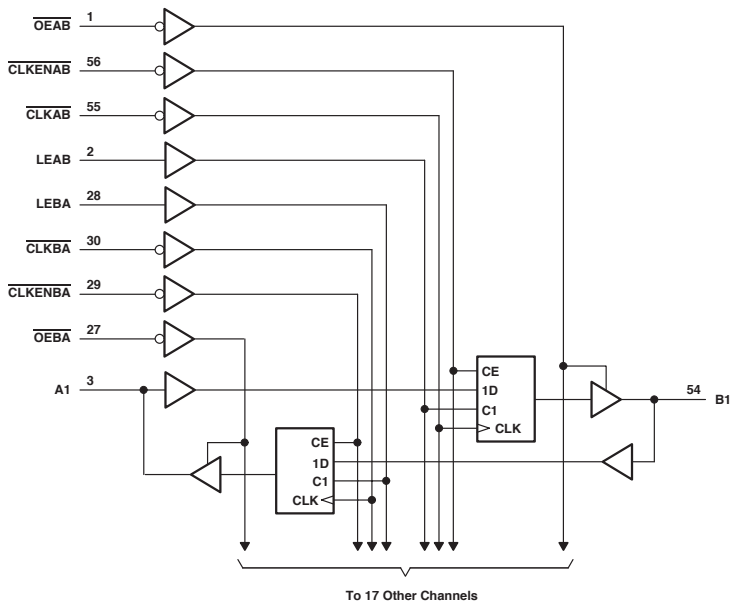
PARAMETER	MAX or MIN	ABT	LVTH 3V	AC	ACT	LVC 3V	LVCH 3V	ALVCH 3V	UNIT
I _{CC}	MAX	35	5	0.08	0.08	0.04	0.02	0.04	mA
I _{OH}	MAX	-32	-32	-24	-24	-24	-24	-24	mA
I _{OL}	MAX	64	64	24	24	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	AC	ACT	LVC 3V	LVCH 3V	ALVCH 3V
t _w Pulse duration, LEAB or LEBA low			MIN	4	3.3	4	7.5	4	3.3	3.3
t _{su} Setup time	Data before LEAB [*] or LEBA [*] , high		MIN	1.5	0.5	1	2.5	2	1.1	1.2
	Data before LEAB [*] or LEBA [*] , low		MIN	3.5	0.8	1	2.5	2	1.1	1.2
	Data before CEAB [*] or CEBA [*] , high		MIN	-	0	-	-	2	1.1	1.2
	Data before CEAB [*] or CEBA [*] , low		MIN	-	0.6	-	-	2	1.1	1.2
t _h Hold time	Data after LEAB [*] or LEBA [*] , high		MIN	1.5	1.5	3	4	2	1.9	1.3
	Data after LEAB [*] or LEBA [*] , low		MIN	2	1.2	3	4	2	1.9	1.3
	Data after CEAB [*] or CEBA [*] , high		MIN	-	1.7	-	-	2	1.9	1.3
	Data after CEAB [*] or CEBA [*] , low		MIN	-	1.6	-	-	2	1.9	1.3
IP _{LH}	A or B	B or A	MAX	3.8	3.2	8.8	10.5	8	5.4	4.3
IP _{HL}				5.1	3.2	9.2	11.6	8	5.4	4.3
IP _{LH}	\overline{LE}	A or B	MAX	5.2	3.9	11.5	13.8	9	6.1	5
IP _{HL}				5.6	3.9	10.9	13.5	9	6.1	5
IP _{ZH}	\overline{OE}	A or B	MAX	5.2	4.3	9.6	11.4	8.5	6.3	5.3
IP _{ZL}				7	4.3	11.3	13.2	8.5	6.3	5.3
IP _{HZ}	\overline{OE}	A or B	MAX	5.7	4.7	8.9	11.1	8.5	6.3	4.6
IP _{LZ}				4.6	4.4	8.4	9.6	8.5	6.3	4.6
IP _{ZH}	\overline{CE}	A or B	MAX	6.2	4.5	9.8	11.7	9	6.6	5.6
IP _{ZL}				7.8	4.5	11.5	13.5	9	6.6	5.6
IP _{HZ}	\overline{CE}	A or B	MAX	6.6	4.9	9.3	11.6	9	6.6	5.1
IP _{LZ}				5.4	4.7	8.8	10.5	9	6.6	5.1

UNIT: ns

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ₀ †
H	L	L	X	X	B ₀ †
L	L	L	↓	L	L
L	L	L	↓	H	H
L	L	L	H	X	B ₀ †
L	L	L	L	X	B ₀ §

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, CLKBA and CLKENBA.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

RECOMMENDED OPERATING CONDITIONS

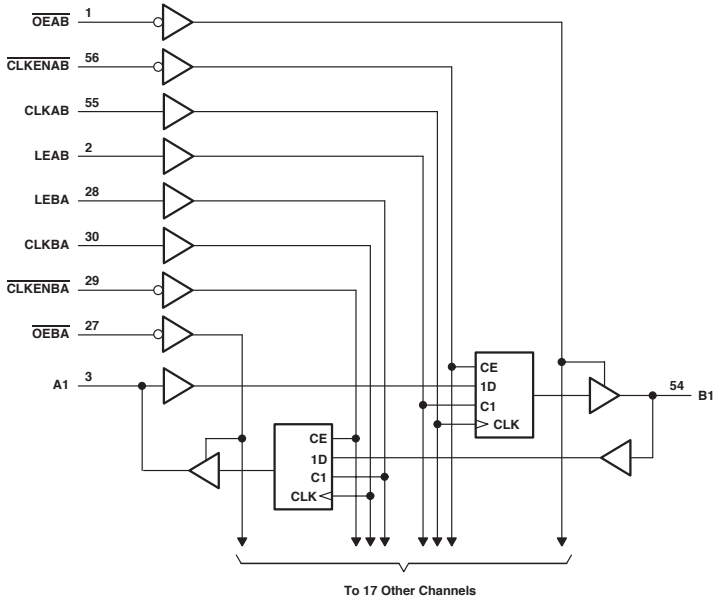
PARAMETER	MAX or MIN	ABT	ALVCH 3V	UNIT
I _{CC}	MAX	36	0.04	mA
I _{DH}	MAX	-32	-24	mA
I _{OL}	MAX	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVCH 3V	
t _{max}			MIN	150	150	
t _w Pulse duration	LEAB or LEBA high		MIN	2.5	3.3	
	CLKAB or CLKBA high or low		MIN	3	3.3	
t _{su} Setup time	A before $\overline{\text{CLKAB}}$, or B before $\overline{\text{CLKBA}}$,		MIN	3	-	
	Data before $\overline{\text{CLK}}$ *			-	1.2	
	A before LEAB, or B before LEBA, $\overline{\text{CLK}}$ high		MIN	2.5	1.1	
	A before LEAB, or B before LEBA, $\overline{\text{CLK}}$ low		MIN	2.5	1.5	
	$\overline{\text{CLKEN}}$ after $\overline{\text{CLK}}$,				2.5	-
	$\overline{\text{CLKEN}}$ after $\overline{\text{CLK}}$ *		MIN	2.5	0.8	
t _h Hold time	A after $\overline{\text{CLKAB}}$, or B after $\overline{\text{CLKBA}}$,		MIN	0	-	
	Data after $\overline{\text{CLK}}$ *			-	1.5	
	A after LEAB, or B after LEBA, $\overline{\text{CLK}}$ high		MIN	2	1.6	
	A after LEAB, or B after LEBA, $\overline{\text{CLK}}$ low		MIN	2	1.3	
	$\overline{\text{CLKEN}}$ after $\overline{\text{CLK}}$,				1	-
	$\overline{\text{CLKEN}}$ after $\overline{\text{CLK}}$ *		MIN	-	1.4	
t _{PLH}	A or B	B or A	MAX	4	4	
t _{PHL}				4.9	4	
t _{PLH}	LEAB or LEBA	B or A	MAX	5	4.8	
t _{PHL}				5	4.8	
t _{PLH}	$\overline{\text{CLKAB}}$ or $\overline{\text{CLKBA}}$	B or A	MAX	5.3	5.7	
t _{PHL}				5	5.7	
t _{PZH}	$\overline{\text{OEAB}}$	B	MAX	5.1	5.2	
t _{PZL}				5.4	5.2	
t _{PHZ}	$\overline{\text{OEAB}}$	B	MAX	6.2	4.4	
t _{PLZ}				5.4	4.4	
t _{PZH}	$\overline{\text{OEBA}}$	A	MAX	5.1	5.2	
t _{PZL}				5.4	5.2	
t _{PHZ}	$\overline{\text{OEBA}}$	A	MAX	6.2	4.4	
t _{PLZ}				5.4	4.4	

UNIT f_{max}: MHz other: ns

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT B
CLKENAB	OEAB	LEAB	CLKAB	A	
X	H	X	X	X	Z
X	L	L	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ₀ †
H	L	L	X	X	B ₀ †
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B ₀ †
L	L	L	H	X	B ₀ §

† A-to-B data flow is shown; B-to-A flow is similar but uses OEAB, LEBA, CLKBA and CLKENBA.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

RECOMMENDED OPERATING CONDITIONS

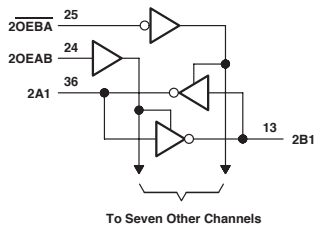
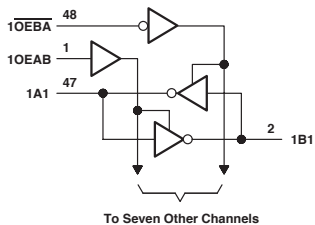
PARAMETER	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V	ALVCHR 3V	UNIT
I _{CC}	MAX	36	5	0.04	0.04	mA
I _{OH}	MAX	-32	-32	-24	-12	mA
I _{OL}	MAX	64	64	24	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V	ALVCHR 3V
f _{max}			MIN	150	150	150	150
t _w Pulse duration	LEAB or LEBA high		MIN	2.5	1.8	3.3	3.3
	CLKAB or CLKBA high or low		MIN	3	2.3	3.3	3.3
t _{su} Setup time	Data before CLK * high		MIN	4	2.4	2.1	2.1
	Data before CLK * low			4	3.8	2.1	2.1
	A before LEAB , or B before LEBA , , CLK high		MIN	2.5	1	1.6	1.6
	A before LEAB , or B before LEBA , , CLK low		MIN	1	0.6	1.1	1.1
	CLKEN before * high		MIN	2.5	1.4	1.7	1.7
CLKEN before * low		2.5		1.9	1.7	1.7	
t _h Hold time	Data after CLK * high		MIN	0	0.5	0.8	0.8
	Data after CLK * low			0	0.5	0.8	0.8
	A after LEAB , or B after LEBA , , CLK high		MIN	2	2	1.4	1.4
	A after LEAB , or B after LEBA , , CLK low		MIN	2	2.3	1.7	1.7
	CLKEN after * high		MIN	0	0.6	0.6	0.6
	CLKEN after * low			0	0.5	0.6	0.6
t _{PLH}	A or B	B or A	MAX	4	3.9	4.1	4.4
t _{PHL}				4.9	3.9	4.1	4.4
t _{PLH}	LEAB or LEBA	B or A	MAX	5	4.6	4.7	5.1
t _{PHL}				5.2	4.6	4.7	5.1
t _{PLH}	CLKAB or CLKBA	B or A	MAX	4.7	4.5	5	5.4
t _{PHL}				4.6	4.6	5	5.4
t _{PZH}	OEAB	B	MAX	5.5	4.2	5.2	5.6
t _{PZL}				5.8	4.4	5.2	5.6
t _{PHZ}	OEAB	B	MAX	6.2	5.3	4.4	4.7
t _{PLZ}				5.4	4.6	4.4	4.7
t _{PZH}	OEBA	A	MAX	5.5	4.2	5.2	5.6
t _{PZL}				5.8	4.4	5.2	5.6
t _{PHZ}	OEBA	A	MAX	6.2	5.3	4.4	4.7
t _{PLZ}				5.4	4.6	4.4	4.7

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

INPUTS		OPERATION
OEBA	OEAB	
L	L	\overline{B} data to A bus
L	H	\overline{B} data to A bus, \overline{A} data to B bus
H	L	Isolation
H	H	\overline{A} data to B bus

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AC	ACT	UNIT
I _{CC}	MAX	0.08	0.08	mA
I _{DH}	MAX	-24	-24	mA
I _{OL}	MAX	24	24	mA

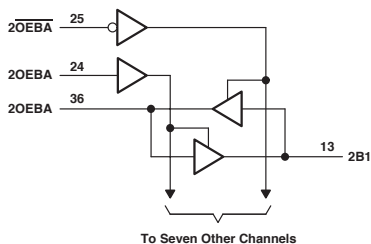
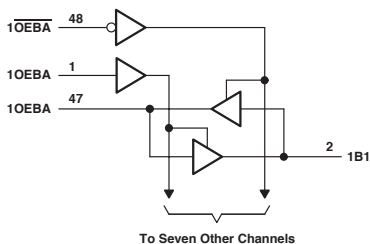
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AC	ACT
t _{PLH}	A	B	MAX	6.8	8.5
t _{PHL}				8.2	10.5
t _{PLH}	B	A	MAX	6.8	8.5
t _{PHL}				8.2	10.5
t _{PZH}	\overline{OEBA}	A	MAX	7.9	9.1
t _{PZL}				9.4	10.9
t _{PHZ}	\overline{OEBA}	A	MAX	9.2	11.9
t _{PLZ}				8.3	10.6
t _{PZH}	OEAB	B	MAX	7.3	8.9
t _{PZL}				9.1	10.5
t _{PHZ}	OEAB	B	MAX	9	10.8
t _{PLZ}				8	9.6

UNIT: ns

16-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
OEBA	OEAB	
L	L	B data to A bus
L	H	B data to A bus, A data to B bus
H	L	Isolation
H	H	A data to B bus

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	UNIT
I _{CC}	MAX	35	0.08	mA
I _{OH}	MAX	-32	-24	mA
I _{OL}	MAX	64	24	mA

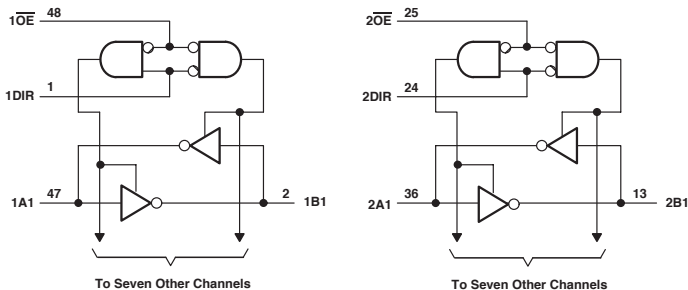
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT
t _{PLH}	A or B	B or A	MAX	3.6	7.7
				4.3	8.6
t _{PHL}	OEBA	A	MAX	4.9	9.5
				6	11.1
t _{PLZ}	OEBA	A	MAX	6	12
				5.4	10.7
t _{PHZ}	OEAB	B	MAX	4.9	9.3
				6	10.6
t _{PLZ}	OEAB	B	MAX	6	10.4
				5.4	9.5

UNIT: ns

16-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
OE	DIR	
L	L	\bar{B} data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

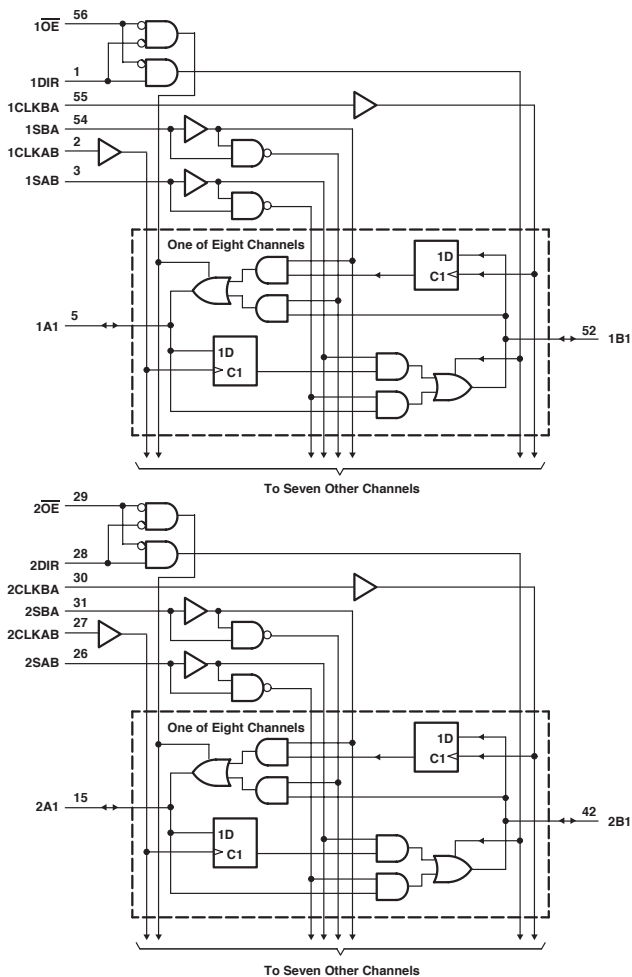
PARAMETER	MAX or MIN	ABT	AC	ACT	UNIT
I_{CC}	MAX	32	0.08	0.08	mA
I_{OH}	MAX	-32	-24	-24	mA
I_{OL}	MAX	64	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	AC	ACT
t_{PLH}	A or B	B or A	MAX	4.3	7.3	9.1
t_{PHL}				3.9	8.6	10.5
t_{PZH}	\bar{OE}	A or B	MAX	5.5	8	9.8
t_{PZL}				6.3	9.9	11.5
t_{PHZ}	\bar{OE}	A or B	MAX	6.3	9.9	12.5
t_{PLZ}				4.2	9	11

UNIT: ns

Logic Diagram



FUNCTION TABLE

INPUTS						DATA I/O		OPERATION OR FUNCTION
OE	DIR	CLKAB	CLKBA	SAB	SBA	A1 THRU A8	B1 THRU B8	
X	X	↑	X	X	X	Input	Unspecified †	Store A, B unspecified †
X	X	↑	↑	X	X	Unspecified †	Input	Store B, A unspecified †
H	X	↑	↑	X	X	Input	Input	Store A and B data
H	X	H or L	H or L	X	X	Input disabled	Input disabled	Isolation, hold storage
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Stored B data to A bus
L	H	X	X	L	X	Input	Output	Real-time A data to B bus
L	H	H or L	X	H	X	Input	Output	Stored A data to B bus

† The data output functions may be enabled or disabled by various signals at the OE and DIR inputs. Data input functions are always enabled; i.e., data at the bus pins will be stored on every low-to-high transition of the clock inputs.

RECOMMENDED OPERATING CONDITIONS

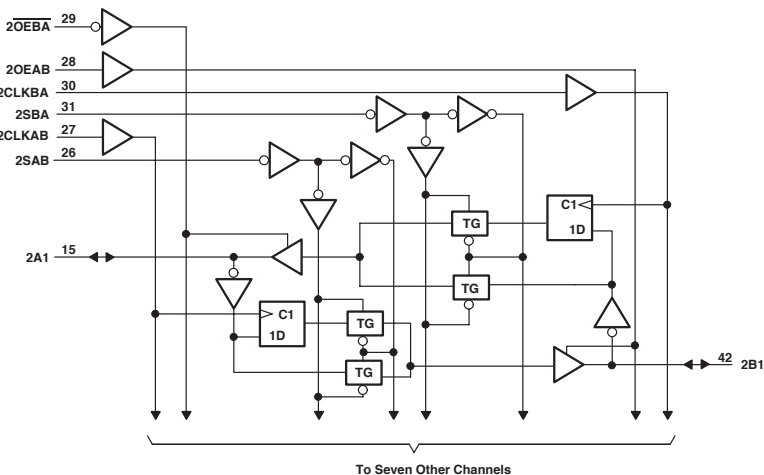
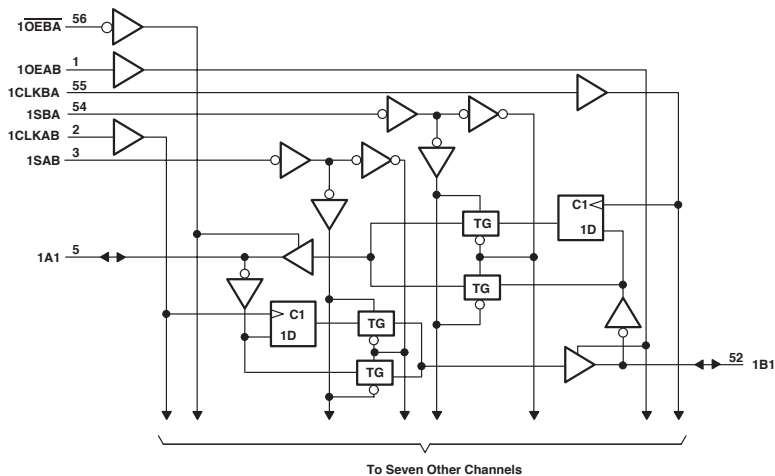
PARAMETER	MAX or MIN	ABT	LVTH 3V	AC	ACT	LVCH 3V	ALVCH 3V	AVC	UNIT
Icc	MAX	32	5	0.08	0.08	0.02	0.04	0.04	mA
Ioh	MAX	-32	-32	-24	-24	-24	-24	-12	mA
Iol	MAX	64	64	24	24	24	24	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	AC	ACT	LVCH 3V	ALVCH 3V	AVC
fmax			MIN	125	150	75	90	150	150	350
t _w Pulse duration	CLKAB or CLKBA high or low		MIN	4.3	3.3	6.5	5.5	3.3	3.3	1.4
t _{su} Setup time	A or B before CLKAB ' or CLKBA ', data high		MIN	3	1.2	5	4	2.9	1.4	0.8
	A or B before CLKAB ' or CLKBA ', data low		MIN	3	2	5	6	2.9	1.4	0.8
t _h Hold time	A or B after CLKAB ' or CLKBA ', data high		MIN	0	0.5	1	1.5	0.3	0.7	0.6
	A or B after CLKAB ' or CLKBA ', data low		MIN	0	0.5	1	1.5	0.3	0.7	0.6
t _{PLH}	CLKAB or CLKBA	B or A	MAX	4.9	4.2	12.1	12.2	6.7	4.5	3.3
t _{PHL}				4.7	4.2	11.9	12.3	6.7	4.5	3.3
t _{PLH}	A or B	B or A	MAX	3.9	3.4	9.5	10.6	5.7	3.9	2.6
t _{PHL}				4.6	3.4	9.7	11.4	5.7	3.9	2.6
t _{PLH}	SAB or SBA	B or A	MAX	5	4.5	12.5	15.6	7.7	5.3	4
t _{PHL}				5	4.5	13.1	16.7	7.7	5.3	4
t _{PLZ}	OE	A or B	MAX	5.5	4.3	10.5	11.9	6.9	5.1	4
t _{PZL}				5.7	4.3	12.2	13.5	6.9	5.1	4
t _{PHZ}	OE	A or B	MAX	5.4	5.6	8.9	10.2	6.9	4.7	4.2
t _{PLZ}				4.5	5.4	8.6	9.9	6.9	4.7	4.2
t _{PLZ}	DIR	A or B	MAX	5.4	4.4	10.9	15.2	7.2	5.1	4.3
t _{PZL}				5.6	4.4	12.2	13.1	7.2	5.1	4.3
t _{PHZ}	DIR	A or B	MAX	6.7	5.7	9.4	10.8	7	5.3	4.3
t _{PLZ}				5.9	5.2	8.8	10.4	7	5.3	4.3

UNIT fmax : MHz other : ns

Logic Diagram



FUNCTION TABLE

INPUTS						DATA I/O †		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1-A8	B1-B8	
L	H	L	L	X	X	Input	Input	Isolation
L	H	†	†	X	X	Input	Input	Store A and B data
X	H	†	L	X	X	Input	Unspecified‡	Store A, hold B
H	H	†	†	X‡	X	Input	Output	Store A in both registers
L	X	L	†	X	X	Unspecified‡	Input	Hold A, store B
L	L	†	†	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	L	X	H	Output	Input	Store B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	L	X	H	X	Input	Output	Store A data to B bus
H	L	L	L	H	H	Output	Output	Store A data to B bus and Store B data to A bus

† The data-output functions may be enabled or disabled by a variety of level combinations at OEAB or OEBA. Data-input functions are always enabled; i.e., data at the bus terminals is stored on every low-to-high transition of the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

Select control = H; clocks must be staggered to load both registers.

RECOMMENDED OPERATING CONDITIONS

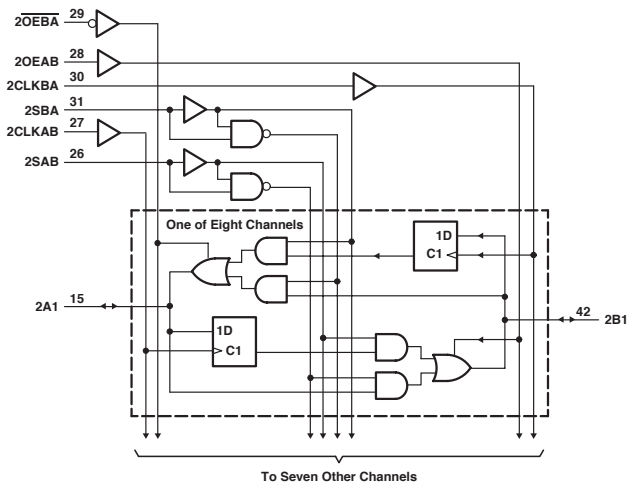
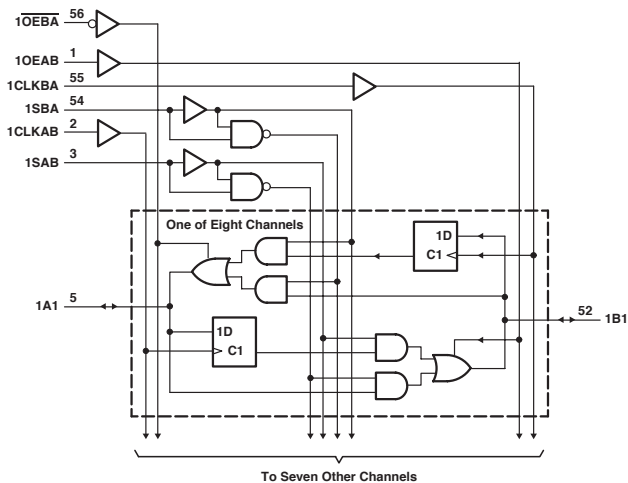
PARAMETER	MAX or MIN	ACT	UNIT
I _{CC}	MAX	0.08	mA
I _{DH}	MAX	-24	mA
I _{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT
f _{max}			MIN	90
t _w Pulse duration	CLKAB or CLKBA high or low		MIN	5.5
t _{su} Setup time	A before CLKAB ' or B before CLKBA '		MIN	5.3
t _h Hold time	A after CLKAB ' or B after CLKBA '		MIN	1
t _{PLH}	A or B	B or A	MAX	11.3
t _{PHL}				11.9
t _{PLH}	CLKAB or CLKBA	A or B	MAX	13.7
t _{PHL}				13.6
t _{PLH}	SAB or SBA	A or B	MAX	17.3
t _{PHL}				17.8
t _{PZH}	OEBA	A	MAX	12.3
t _{PZL}				13.9
t _{PHZ}	OEBA	A	MAX	10.6
t _{PLZ}				10.8
t _{PZH}	OEAB	B	MAX	11.9
t _{PZL}				13.5
t _{PHZ}	OEAB	B	MAX	11.4
t _{PLZ}				11.6

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

INPUTS						DATA I/O†		OPERATION OR FUNCTION
OEAB	OEBA	CLKAB	CLKBA	SAB	SBA	A1 THRU AB	B1 THRU B8	
L	H	H or L	H or L	X	X	Input	Input	Isolation
L	H	↑	↑	X	X	Input	Input	Store A and B data
X	H	↑	↑	X	X	Input	Unspecified ‡	Store A, hold B
H	H	↑	↑	X‡	X	Input	Output	Store A in both registers
L	X	H or L	↑	X	X	Unspecified ‡	Input	Hold A, store B
L	L	↑	↑	X	X‡	Output	Input	Store B in both registers
L	L	X	X	X	L	Output	Input	Real-time B data to A bus
L	L	X	H or L	X	H	Output	Input	Store B data to A bus
H	H	X	X	L	X	Input	Output	Real-time A data to B bus
H	H	H or L	X	H	X	Input	Output	Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus and stored B data A bus

† The data output functions may be enabled or disabled by a variety of level combinations at the OEAB or OEBA inputs. Data input functions are always enabled; i.e., data at the bus pins is stored on every low-to-high transition of the clock inputs.

‡ Select control = L; clocks can occur simultaneously.

§ Select control = H; clocks must be staggered in order to load both registers.

RECOMMENDED OPERATING CONDITIONS

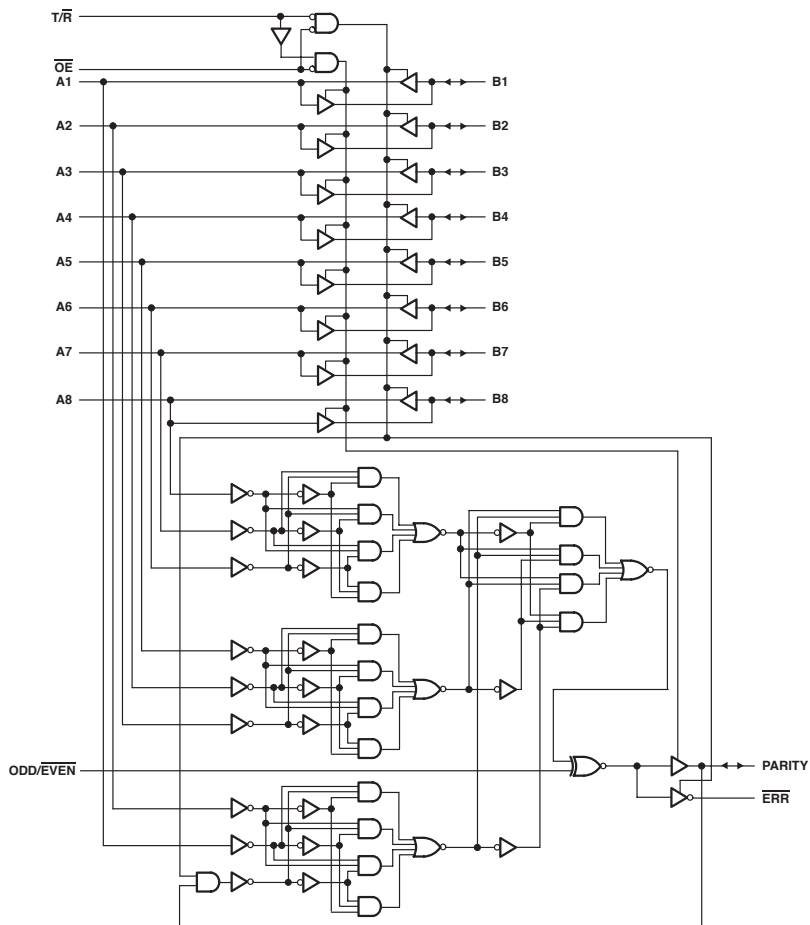
PARAMETER	MAX or MIN	ABT	LVTH 3V	AC	ACT	LVCH 3V	UNIT
I _{CC}	MAX	32	5	0.08	0.08	0.02	mA
I _{QH}	MAX	-32	-32	-24	-24	-24	mA
I _{OL}	MAX	64	64	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVTH 3V	AC	ACT	LVCH 3V
f _{max}			MIN	125	150	95	90	150
t _w Pulse duration	CLKAB or CLKBA high or low		MIN	4.3	3.3	5	5.5	3.3
t _{su} Setup time	A before CLKAB * or B before CLKBA *, high		MIN	3	1.2	4.5	4.5	3
	A before CLKAB * or B before CLKBA *, low		MIN	3	2	4.5	4.5	3
t _h Hold time	A after CLKAB * or B after CLKBA *, high		MIN	0	0.5	0	1	0.2
	A after CLKAB * or B after CLKBA *, low		MIN	0	0.5	0	1	0.2
t _{PLH}	CLKAB or CLKBA	A or B	MAX	4.9	4.2	12.2	12.3	6.4
				4.7	4.2	12.3	12.3	6.4
t _{PHL}	A or B	B or A	MAX	3.9	3.4	9.9	10.5	6.3
				4.6	3.4	10.2	11.6	6.3
t _{PLH}	SAB or SBA	A or B	MAX	5	4.5	13.8	16	7.4
				5	4.5	13.8	16.9	7.4
t _{PZH}	OEBA	A	MAX	5	4.3	10.7	11.7	6.3
				5.3	4.3	13.2	13.4	6.3
t _{PHZ}	OEBA	A	MAX	4.9	5.6	8.8	9.5	6.2
				4	5.4	8.7	9.2	6.2
t _{PZH}	OEAB	B	MAX	4.2	4.2	10.5	10.8	6.3
				4.6	4.2	13	12.4	6.3
t _{PHZ}	OEAB	B	MAX	5.9	5.5	8	10.5	6.2
				5.2	5.5	7.8	9.9	6.2

UNIT f_{max}: MHz other: ns

Logic Diagram



FUNCTION TABLE
(each 8-bit section)

NUMBER OF A OR B INPUTS THAT ARE HIGH	INPUTS			INPUT/OUTPUT PARITY	OUTPUTS	
	\overline{OE}	T/R	ODD/EVEN		ERR	OUTPUT MODE
0, 2, 4, 6, 8	L	H	H	H	Z	Transmit
	L	H	L	L	Z	Transmit
	L	L	H	H	H	Receive
	L	L	H	L	L	Receive
	L	L	L	L	H	Receive
1, 3, 5, 7	L	H	H	L	Z	Transmit
	L	H	L	H	Z	Transmit
	L	L	H	H	L	Receive
	L	L	H	L	H	Receive
	L	L	L	H	H	Receive
	L	L	L	L	L	Receive
Don't care	H	X	X	Z	Z	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	UNIT
I _{CC}	MAX	36	0.08	mA
I _{OH}	MAX	-32	-24	mA
I _{OL}	MAX	64	24	mA

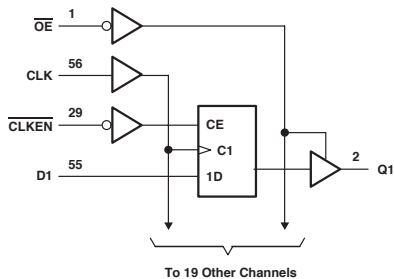
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT
t _{PLH}	A or B	B or A	MAX	4.1	10.7
				4.3	10.6
t _{PLH}	A or B	PARITY	MAX	6.7	14.3
				6.1	14.3
t _{PHL}	ODD / EVEN	PARITY, \overline{ERR}	MAX	6.7	13.7
				6.1	14.1
t _{PLH}	B	\overline{ERR}	MAX	6.7	14.6
				6.1	14.7
t _{PHL}	PARITY	\overline{ERR}	MAX	6.7	13.8
				6.1	14.2
t _{PZH}	\overline{OE}	A or B	MAX	5.6	11.3
				6	13
t _{PHZ}	\overline{OE}	A or B	MAX	5.4	11.2
				4.3	10.5
t _{PZH}	\overline{OE}	PARITY, \overline{ERR}	MAX	5.6	11.3
				6	13
t _{PHZ}	\overline{OE}	PARITY, \overline{ERR}	MAX	5.4	11.2
				4.3	10.5

UNIT: ns

20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each flip-flop)

INPUTS				OUTPUT
OE	CLKEN	CLK	D	Q
L	H	X	H	Q _O
L	L	↑	H	H
L	L	↑	L	L
L	L	L	X	Q _O
H	X	X	X	Z

RECOMMENDED OPERATING CONDITIONS

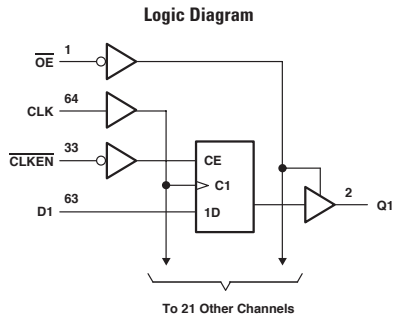
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH}	MAX	-24	mA
I _{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f _{max}			MIN	150
t _w Pulse duration	CLK high or low		MIN	3.3
t _{su} Setup time	Data before CLK *		MIN	3.1
	CLKEN before CLK *		MIN	2.7
t _h Hold time	Data after CLK *		MIN	0
	CLKEN after CLK *		MIN	0
t _{PLH}	CLK	Q	MAX	4.3
t _{PHL}				4.3
t _{PZH}	OE	Q	MAX	4.8
t _{PZL}				4.8
t _{PHZ}	OE	Q	MAX	4.4
t _{PLZ}				4.4

UNIT f_{max} : MHz other : ns

22-BIT FLIP-FLOP WITH 3-STATE OUTPUTS



FUNCTION TABLE
(each flip-flop)

INPUTS				OUTPUT Q
OE	CLKEN	CLK	D	
L	H	X	X	Q ₀
L	L	↑	H	H
L	L	↑	L	L
L	L	L or H	X	Q ₀
H	X	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	AVC 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH}	MAX	-12	mA
I _{OL}	MAX	12	mA

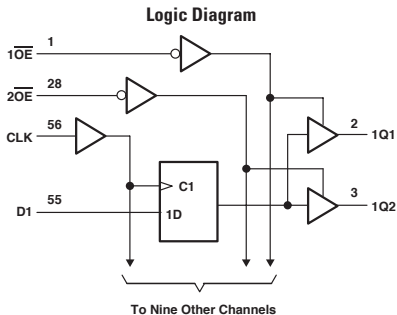
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	AVC 3V
t _{max}			MIN	150
t _w Pulse duration	CLK high or low		MIN	2.8
t _{su} Setup time	Data before CLK		MIN	2.5
	CLKEN before CLK		MIN	1.4
t _h Hold time	Data after CLK		MIN	0
	CLKEN after CLK		MIN	1.2
t _{PLH}	CLK	Q	MAX	2.6
t _{PHL}				2.6
t _{PZH}	OE	Q	MAX	4.3
t _{PZL}				4.3
t _{PHZ}	OE	Q	MAX	3.4
t _{PLZ}				3.4

UNIT f_{max} : MHz other : ns

16820

10-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH DUAL OUTPUTS



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
\overline{OE}_n †	CLK	D	Q_n †
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

† $n = 1, 2$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

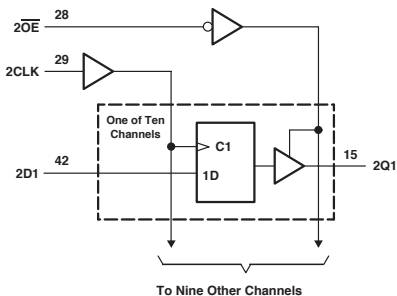
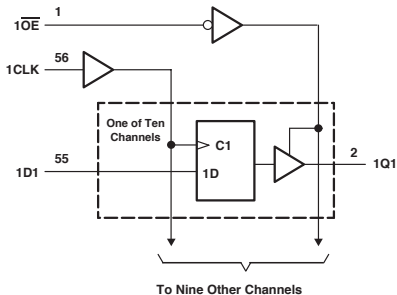
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f_{max}			MIN	150
t_w Pulse duration	CLK high or low		MIN	3.3
t_{su} Setup time	Data before CLK *		MIN	1.4
t_h Hold time	Data after CLK *		MIN	1
t_{PLH}	CLK	Q	MAX	4.8
t_{PHL}				4.8
t_{PZH}	\overline{OE}	Q	MAX	5
t_{PZL}				5
t_{PHZ}	\overline{OE}	Q	MAX	4.5
t_{PLZ}				4.5

UNIT f_{max} : MHz other : ns

16821

20-BIT BUS INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V	UNIT
I _{CC}	MAX	89	5	0.08	0.04	mA
I _{OH}	MAX	-32	-32	-24	-24	mA
I _{OL}	MAX	64	64	24	24	mA

SWITCHING CHARACTERISTICS

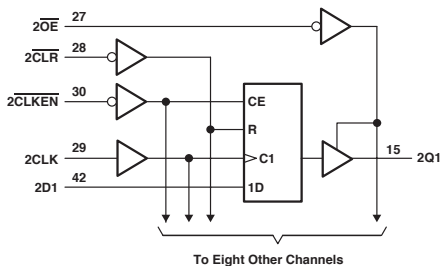
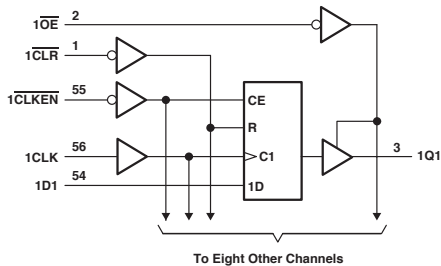
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V
f _{max}			MIN	150	150	70	150
t _w Pulse duration	CLK high or low		MIN	3.3	1.5	7	3.3
t _{su} Setup time	Data before CLK *, low		MIN	1.8	1.5	7.5	3.4
	Data before CLK *, high		MIN	1.8	1.5	7.5	3.4
t _h Hold time	Data after CLK *, high		MIN	1.3	1	0.5	0
	Data after CLK *, low		MIN	1.3	1	0.5	0
t _{PLH}	CLK	Q	MAX	6.1	3.5	13.4	4.5
				5.4	3.5	14	4.5
t _{PZH}	OE	Q	MAX	5.7	4.1	11.9	5.1
				5.6	3.6	14.7	5.1
t _{PHZ}	OE	Q	MAX	6.5	4.8	10.7	4.6
				7.1	4.8	10	4.6

UNIT f_{max}: MHz other: ns

16823

18-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH DUAL OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 9-bit flip-flop)

INPUTS					OUTPUT
OE	CLR	CLKEN	CLK	D	Q
L	L	X	X	X	L
L	H	L	↑	H	L
L	H	L	↑	L	L
L	H	L	L	X	Q ₀
L	H	H	X	X	Q ₀
H	X	X	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ABTH	AC	ACT	ALVCH 3V	UNIT
I _{CC}	MAX	80	80	0.08	0.08	0.04	mA
I _{OH}	MAX	-32	-32	-24	-24	-24	mA
I _{OL}	MAX	64	64	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	AC	ACT	ALVCH 3V
f _{max}			MIN	150	150	115	90	150
t _w Pulse duration	CLR low		MIN	3.3	3.3	3.3	3.3	3.3
	CLK high or low		MIN	3.3	3.3	4.4	5.5	3.3
t _{su} Setup time	CLR inactive		MIN	1.6	1.6	0.6	0.5	0.8
	Data high before CLK *		MIN	1.7	1.7	5	7	1
	Data low before CLK *		MIN	1.7	1.7	5	7	1.3
	CLKEN low before CLK *		MIN	2.8	2.8	4.2	3.5	1.5
t _h Hold time	Data high after CLK *		MIN	1.2	1.2	1.3	0.5	0.8
	Data low after CLK *		MIN	1.2	1.2	1.3	0.5	0.5
	CLKEN low after CLK *		MIN	0.6	0.6	1.4	2.5	0.4
TP _{LH}	CLK	Q	MAX	6.8	6.8	12	12.1	4.5
TP _{HL}				6	6	12.7	12.9	4.5
IP _{LH}				-	-	-	-	4.6
IP _{HL}	CLR	Q	MAX	6.1	6.7	11	12.5	4.6
DP _{ZH}	OE	Q	MAX	4.9	4.9	9.7	10.7	4.8
DP _{ZL}				5.5	5.5	11.8	12.8	4.8
IP _{HZ}				6.1	6.1	9.3	10.3	4.5
IP _{LZ}	OE	Q	MAX	8.7	8.7	8.6	9.4	4.5

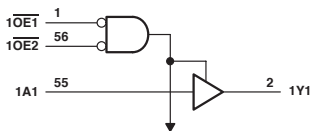
UNIT f_{max} : MHz other : ns

■ : OBSOLETE or NOT RECOMMENDED NEW DESIGNS

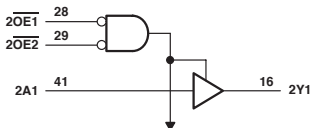
16825

18-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram



To Eight Other Channels



To Eight Other Channels

FUNCTION TABLE
(each 9-bit section)

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	ALVCH 3V	UNIT
I _{CC}	MAX	32	0.08	0.04	mA
I _{OH}	MAX	-32	-24	-24	mA
I _{OL}	MAX	64	24	24	mA

SWITCHING CHARACTERISTICS

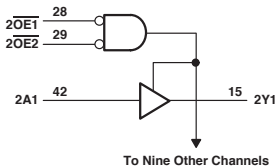
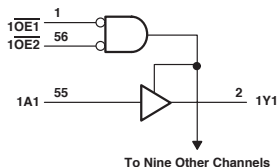
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	ALVCH 3V
t _{PLH}	A	Y	MAX	3.9	10.5	3.4
				4.4	10.3	3.4
t _{PZH}	\overline{OE}	Y	MAX	6.1	11	4.7
				6	13.2	4.7
t _{PHZ}	\overline{OE}	Y	MAX	6.9	11.5	4.5
				6.6	10.6	4.5

UNIT: ns

16827

20-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 10-bit section)

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

RECOMMENDED OPERATING CONDITIONS

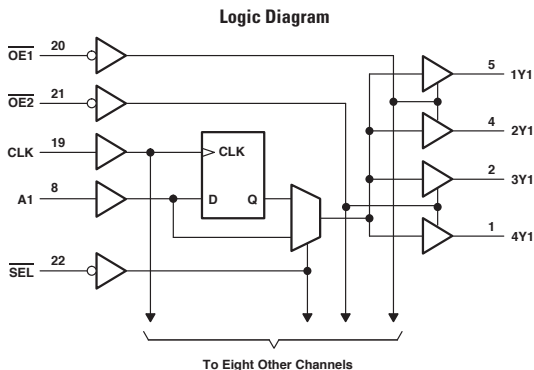
PARAMETER	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V	AVC	UNIT
I _{CC}	MAX	32	6	0.08	0.04	0.04	mA
I _{OH}	MAX	-32	-32	-24	-24	-12	mA
I _{OL}	MAX	64	64	24	24	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVTH 3V	ACT	ALVCH 3V	AVC
t _{PLH}	A	Y	MAX	3.4	3	11	3.4	1.7
				4.2	2.8	10.8	3.4	1.7
t _{PHL}	\overline{OE}	Y	MAX	5.6	3.9	11.7	4.7	5.1
				5.5	3.4	14	4.7	5.1
t _{PHZ}	\overline{OE}	Y	MAX	6.6	5.8	12.4	4.5	4.7
				6.1	4.6	11.5	4.5	4.7

UNIT: ns

1-TO-4 ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS



FUNCTION TABLE

INPUTS				OUTPUT
OE	SEL	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

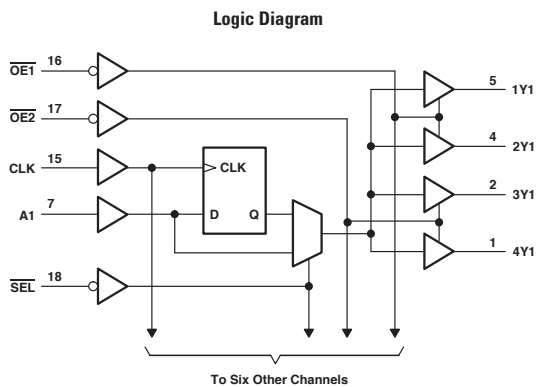
RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{DH}	MAX	-24	mA
I _{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f _{max}			MIN	150
t _w Pulse duration	CLK high or low		MIN	3.3
t _{su} Setup time	A data before CLK '↑'		MIN	1.6
t _h Hold time	A data after CLK '↓'		MIN	1.1
t _{PLH}	A	Y	MAX	3.6
t _{PHL}				3.6
t _{PLH}	CLK	Y	MAX	3.9
t _{PHL}				3.9
t _{PLH}	SEL	Y	MAX	4.4
t _{PHL}				4.4
t _{PZH}	OE	Y	MAX	4.3
t _{PZL}				4.3
t _{PHZ}	OE	Y	MAX	4.5
t _{PLZ}				4.5

UNIT f_{max} : MHz other : ns



FUNCTION TABLE

INPUTS				OUTPUT
OE	SEL	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH}	MAX	-24	mA
I _{OL}	MAX	24	mA

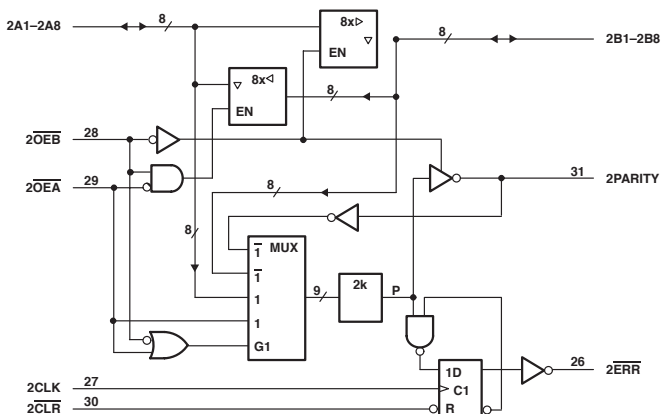
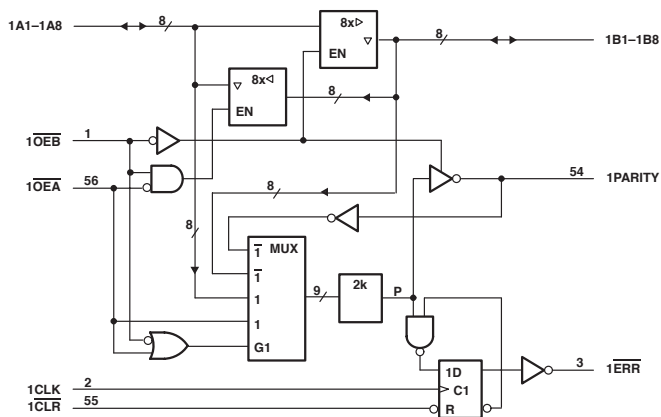
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
t _{max}			MIN	150
t _w Pulse duration	CLK high or low		MIN	3.3
t _{su} Setup time	A data before CLK *		MIN	1.6
t _h Hold time	A data after CLK *		MIN	1.1
t _{PLH}	A	Y	MAX	3.6
t _{PHL}				3.6
t _{PLH}	CLK	Y	MAX	3.9
t _{PHL}				3.9
t _{PLH}	$\overline{\text{SEL}}$	Y	MAX	4.4
t _{PHL}				4.4
t _{PZH}	$\overline{\text{OE}}$	Y	MAX	4.3
t _{PZL}				4.3
t _{PHZ}	$\overline{\text{OE}}$	Y	MAX	4.5
t _{PLZ}				4.5

 UNIT f_{max} : MHz other : ns

DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

Logic Diagram



FUNCTION TABLE

INPUTS						OUTPUT AND I/O				FUNCTION
OEB	OEA	CLR	CLK	A Σ OF H	Bi† Σ OF H	A	B	PARITY	ERR‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	↑	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
X	X	L	X	X	X	X	NA	NA	H	Check error flag register
H	H	L	↑	No ↑ No ↑ Odd Even	X	Z	Z	Z	NC H H L	Isolation§
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care

† Summation of high-level inputs includes PARITY along with Bi inputs. ‡ Output states shown when ERR was previously high.

§ In this mode, ERR (when clocked) shows inverted parity of the A bus.

ERROE-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT PRE-STATE	OUTPUT ERR	FUNCTION
CLR	CLK	POINT P	ERR _{n-1} †	ERR	
H	↑	H	H	H	Sample
H	↑	X	L	L	
H	↑	L	X	L	
L	X	X	X	H	Clear

† State of ERR before any changes at CLR, CLK, or point P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	UNIT
I _{CC}	MAX	36	0.08	mA
I _{OH}	MAX	-32	-24	mA
I _{OL}	MAX	64	24	mA

SWITCHING CHARACTERISTICS

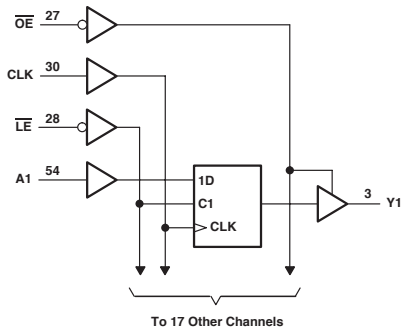
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT
t _w Pulse duration	CLK high or low		MIN	3	4
	CLR low			-	-
t _{su} Setup time	A data before CLK *, A port		MIN	4.5	-
	A data before CLK *, CLR			1	1.5
	A data before CLK *, OEA			5	-
t _h Hold time	A data after CLK *, A port or OEA		MIN	0	0
t _{PLH}	A or B	B or A	MAX	4.1	10.4
t _{PHL}				4.3	10.7
t _{PLH}	A	PARITY	MAX	6.7	13.5
t _{PHL}				6.1	13.8
t _{PZH}	OEB or OEA	A or B	MAX	5.6	11.2
t _{PZL}				6	13
t _{PHZ}	OEB or OEA	A or B	MAX	5.4	10.8
t _{PLZ}				4.3	10.1
t _{PLH}	CLK, CLR	ERR	MAX	4.6	15.8
t _{PHL}				3.9	11.6
t _{PLH}	OEB	PARITY	MAX	6.7	-
t _{PHL}				6.1	-
t _{PLH}	OEA	PARITY	MAX	6.7	13.2
t _{PHL}				6.1	13.6
t _{PZH}	OEB	PARITY	MAX	5.7	9.5
t _{PZL}				6.5	10.7
t _{PHZ}	OEB	PARITY	MAX	4.7	10.2
t _{PLZ}				4.1	9.7
t _{PZH}	OEA	PARITY	MAX	5.7	-
t _{PZL}				6.5	-
t _{PHZ}	OEA	PARITY	MAX	4.7	-
t _{PLZ}				4.1	-

UNIT: ns

16834

16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE	LE	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Y _{0†}
L	H	L	X	Y _{0‡}

† Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes high.

‡ Output level before the indicated steady-state input conditions were established.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	AVC 3V	UNIT
I _{CC}	MAX	0.04	0.04	mA
I _{OH}	MAX	-24	-12	mA
I _{OL}	MAX	24	12	mA

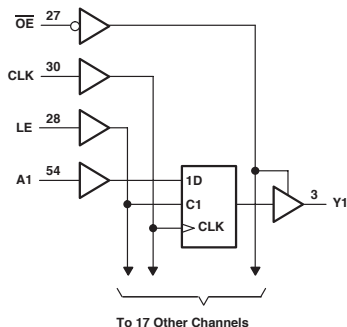
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	AVC 3V
f _{max}			MIN	150	150
t _w Pulse duration	LE low		MIN	3.3	3.3
	CLK high or low		MIN	3.3	3.3
t _{su} Setup time	Data before CLK *		MIN	1.7	0.7
	Data before LE *, CLK high		MIN	1.9	1
	Data before LE *, CLK low		MIN	1.5	1
t _h Hold time	A data after CLK *		MIN	0.7	0.9
	Data after LE *, CLK high		MIN	0.9	1.4
	Data after LE *, CLK low		MIN	0.9	1.3
t _{PLH}	A	Y	MAX	3.6	2.5
				3.6	2.5
t _{PLH}	LE	Y	MAX	4.9	4
				4.9	4
t _{PLH}	CLK	Y	MAX	4.6	3.1
				4.6	3.1
t _{PZL}	OE	Y	MAX	5	6.2
				5	6.2
t _{PHZ}	OE	Y	MAX	4.5	5.3
				4.5	5.3

UNIT f_{max} : MHz other : ns

3.3-V ABT 18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	H	X	Y ₀ †
L	L	L	X	Y ₀ ‡

† Output level before the indicated steady-state input conditions were established, provided that CLK was high before LE went low.

‡ Output level before the indicated steady-state input conditions were established.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	ALVC 3V	ALVCH 3V	AVC 3V	UNIT
I _{CC}	MAX	5	0.04	0.04	0.04	mA
I _{OH}	MAX	-32	-24	-24	-12	mA
I _{OL}	MAX	64	24	24	12	mA

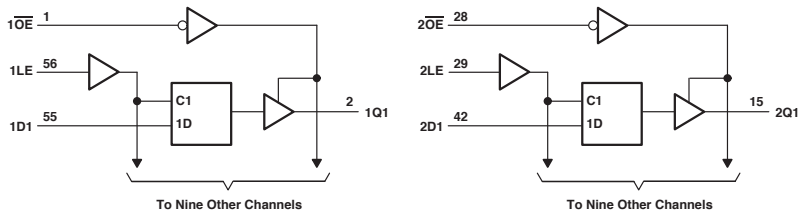
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVC 3V	ALVCH 3V	AVC 3V
f _{max}			MIN	150	150	150	150
t _w Pulse duration	LE low		MIN	3.3	3.3	3.3	3.3
	CLK high or low		MIN	3.3	3.3	3.3	3.3
t _{su} Setup time	Data before CLK *		MIN	2.1	1.7	1.7	0.7
	Data before LE , , CLK high		MIN	2.3	1.5	1.5	0.8
	Data before LE , , CLK low		MIN	1.5	1	1	0.5
t _h Hold time	A data after CLK *		MIN	1	0.7	0.7	1.3
	Data after LE , , CLK high		MIN	0.8	1.4	1.4	1.6
	Data after LE , , CLK low		MIN	0.8	1.4	1.4	1.4
t _{PLH}	A	Y	MAX	3.7	3.6	3.6	2.5
				3.7	3.6	3.6	2.5
t _{PHL}	LE	Y	MAX	5.1	4.2	4.2	3.8
				5.1	4.2	4.2	3.8
t _{PLH}	CLK	Y	MAX	5.1	4.5	4.5	3.1
				5.1	4.5	4.5	3.1
t _{PZH}	OE	Y	MAX	4.6	4.6	4.6	6.2
				4.6	4.6	4.6	6.2
t _{PHZ}	OE	Y	MAX	5.8	3.9	3.9	5.3
				5.8	3.9	3.9	5.3

UNIT f_{max}: MHz other: ns

20-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 10-bit latch)

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	ALVCH 3V	UNIT
I _{CC}	MAX	89	0.08	0.04	mA
I _{OH}	MAX	-32	-24	-24	mA
I _{OL}	MAX	64	24	24	mA

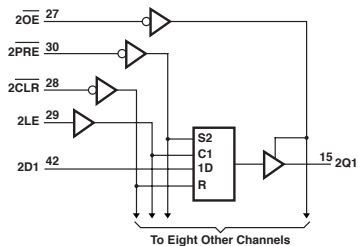
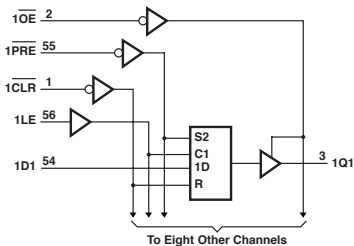
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	ALVCH 3V
t _w Pulse duration	LE high or low		MIN	4	4	3.3
t _{su} Setup time	Data before LE ,		MIN	1	1.5	1.1
t _h Hold time	Data after LE , , high		MIN	2	3	1.1
	Data after LE , , low		MIN	2	4.5	1.1
t _{PLH}	D	Q	MAX	5	11.8	3.9
t _{PHL}				5.1	12.2	3.9
t _{PLH}	LE	Q	MAX	5	12.7	4.3
t _{PHL}				5	12.7	4.3
t _{PZL}	OE	Q	MAX	5.7	11.3	4.9
t _{PZL}				5.6	13.7	4.9
t _{PHZ}	OE	Q	MAX	6.5	10.2	4.1
t _{PLZ}				7.1	9.6	4.1

UNIT: ns

18-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 9-bit latch)

INPUTS					OUTPUT
PRE	CLR	OE	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q ₀
X	X	H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I _{CC}	MAX	85	mA
I _{OH}	MAX	-32	mA
I _{OL}	MAX	64	mA

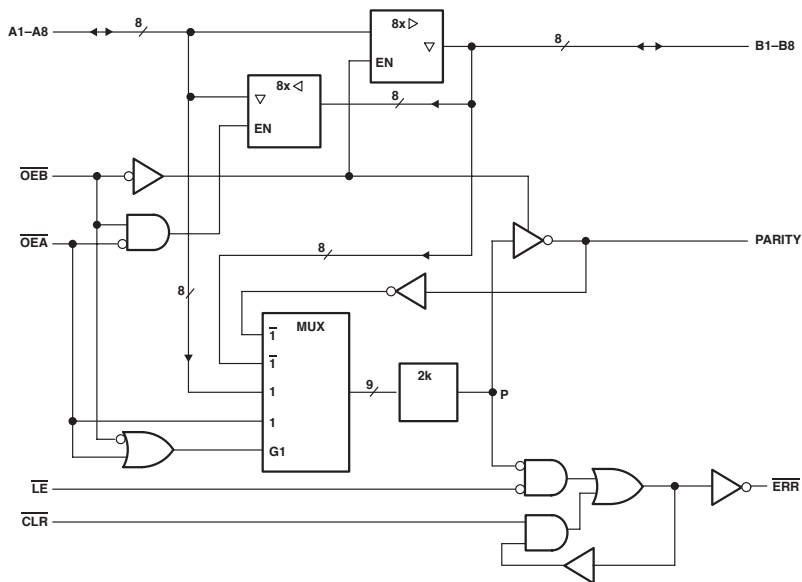
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	
t _w Pulse duration	CLR low		MIN	3.3	
				PRE low	3.3
				LE high	3.3
t _{su} Setup time	Data before LE , high		MIN	0.9	
				Data before LE , low	0.6
t _h Hold time	Data after LE , high		MIN	1.7	
				Data after LE , low	1.8
t _{PLH}	D	Q	MAX	4.8	
t _{PHL}				4.8	
t _{PLH}	LE	Q	MAX	5.9	
t _{PHL}				5.3	
t _{PLH}	PRE	Q	MAX	6.1	
t _{PHL}				5	
t _{PLH}	CLR	Q	MAX	5.4	
t _{PHL}				6	
t _{PZH}	OE	Q	MAX	5.4	
t _{PZL}				5.8	
t _{PHZ}	OE	Q	MAX	6.3	
t _{PLZ}				5.2	

UNIT: ns

DUAL 8-BIT TO 9-BIT PARITY BUS TRANSCEIVERS

Logic Diagram



FUNCTION TABLE

INPUTS						OUTPUT AND I/Os				FUNCTION
OEB	OEA	CLR	LE	Ai Σ OF H	Bi† Σ OF H	A	B	PARITY	ERR‡	
L	H	X	X	Odd Even	NA	NA	A	L H	NA	A data to B bus and generate parity
H	L	H	L	NA	Odd Even	B	NA	NA	H L	B data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	NC	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error flag register
H	H	X	X	L L Odd X L H Even	X	Z	Z	Z	NC H H L	Isolation§ (parity check)
L	L	X	X	Odd Even	NA	NA	A	H L	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care

† Summation of high-level inputs includes PARITY along with Bi inputs.

‡ Output states shown assume ERR was previously high.

§ In this mode, ERR (when clocked) shows inverted parity of the A bus.

ERROR-FLAG FUNCTION TABLE

INPUTS		INTERNAL TO DEVICE	OUTPUT	OUTPUT ERR	FUNCTION
CLR	LE	POINT P	ERR _{n-1} †	ERR	
L	L	L H	X	L H	Pass
H	L	X H	L H	L H	Sample
L	H	X	X	H	Clear
H	H	X	L H	L H	Store

† State of ERR before changes at CLR, LE, or point P

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I _{CC}	MAX	40	mA
I _{OH}	MAX	-32	mA
I _{OL}	MAX	64	mA

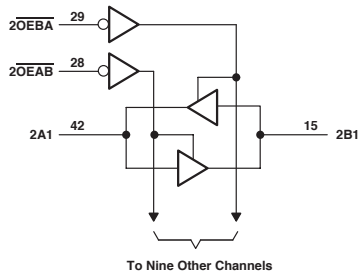
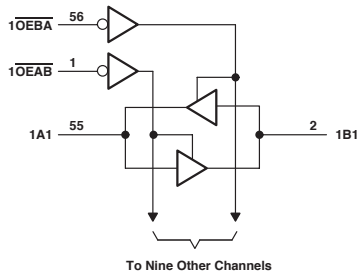
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t _w Pulse duration	\overline{LE} high or low		MIN	8.5
	\overline{CLR} low			4
t _{su} Setup time	A, B and PARITY before \overline{LE} ,		MIN	10
	\overline{CLR} before \overline{LE} ,			0
t _h Hold time	A, B and PARITY after \overline{LE} ,		MIN	0
	\overline{CLR} after \overline{LE} ,			0
t _{PLH}	A or B	B or A	MAX	4.1
t _{PHL}				4.3
t _{PLH}	A or \overline{OE}	PARITY	MAX	7.1
t _{PHL}				7.2
t _{PLH}	\overline{CLR}	\overline{ERR}	MAX	5.7
t _{PZH}	\overline{OE}	A or B	MAX	5.6
t _{PZL}				6
t _{PHZ}	\overline{OE}	A or B	MAX	5.4
t _{PLZ}				4.3
t _{PZH}	\overline{OE}	PARITY	MAX	5.7
t _{PZL}				6.5
t _{PHZ}	\overline{OE}	PARITY	MAX	4.7
t _{PLZ}				4.1
t _{PLH}	\overline{LE}	\overline{ERR}	MAX	4.8
t _{PHL}				4.9
t _{PLH}	A, B or PARITY	\overline{ERR}	MAX	7.2
t _{PHL}				7.4

UNIT: ns

20-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram

FUNCTION TABLE
(each 10-bit section)

INPUTS		OPERATION
OEBA	OEBA	
L	L	Latch A and B (A = B)
L	H	A to B
H	L	B to A
H	H	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ACT	UNIT
I_{CC}	MAX	0.08	mA
I_{OH}	MAX	-24	mA
I_{OL}	MAX	24	mA

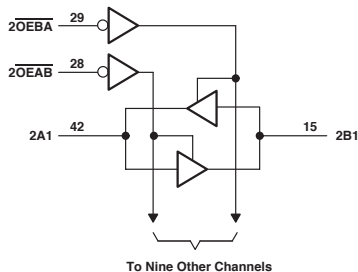
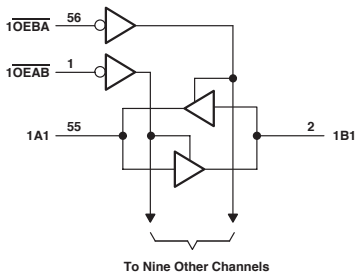
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ACT
t_{PLH}	A or B	B or A	MAX	10.4
t_{PHL}				11.1
t_{PZH}	\overline{OEBA} or \overline{OEAB}	A or B	MAX	10
t_{PZL}				12.7
t_{PHZ}	\overline{OEBA} or \overline{OEAB}	A or B	MAX	10.7
t_{PLZ}				10

UNIT: ns

18-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 9-bit section)

INPUTS		OPERATION
OEAB	OEBA	
H	L	B data to A bus
L	H	A data to B bus
H	H	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ACT	ALVCH 3V	UNIT
I _{CC}	MAX	32	0.08	0.04	mA
I _{DH}	MAX	-32	-24	-24	mA
I _{OL}	MAX	64	24	24	mA

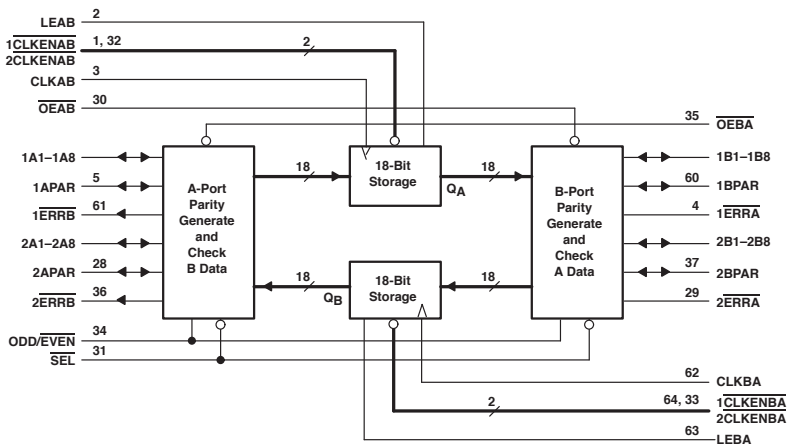
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ACT	ALVCH 3V
t _{PLH}	A or B	B or A	MAX	3.5	11.1	3.4
t _{PHL}				3.9	11.8	3.4
t _{PZH}	OEBA or OEAB	A or B	MAX	5.4	10.6	4.7
t _{PZL}				4.8	13.6	4.7
t _{PHZ}	OEBA or OEAB	A or B	MAX	6	11.6	4.2
t _{PLZ}				5	11	4.2

UNIT: ns

18-BIT UNIVERSAL BUS TRANSCEIVER WITH PARITY GENERATORS/CHECKERS

Block Diagram



FUNCTION TABLE

INPUTS				OUTPUT	
CLKENAB	OEAB	LEAB	CLKAB	A	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ₀ †
L	L	L	↑	L	L
L	L	L	↑	H	H
L	L	L	L	X	B ₀ ‡
L	L	L	L	H	X
L	L	L	L	H	X

† Output level before the indicated steady-state input conditions were established

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low

PARITY-ENABLE FUNCTION TABLE

INPUTS			OPERATION OR FUNCTION	
SEL	OEBA	OEAB		
L	H	L	Parity is checked on port A and is generated on port B.	
L	L	H	Parity is checked on port B and is generated on port A.	
L	H	H	Parity is checked on port B and port A.	
L	L	L	Parity is generated on port A and B if device is in FF mode.	
H	L	L	Parity functions are disabled; device acts as a standard 18-bit registered transceiver.	
H	L	H	Q _A data to B, Q _B data to A	
H	H	L	Q _B data to A	
H	H	H	Q _A data to B	
			Isolation	

PARITY FUNCTION TABLE

INPUTS					OUTPUTS						
SEL	OEBA	OEAB	ODD/EVEN	Σ OF INPUTS A1-A8 = H	Σ OF INPUTS B1-B8 = H	APAR	BPAR	APAR ERRR	BPAR ERRB		
L	H	L	L	0, 2, 4, 6, 8	N/A	L	N/A	N/A	H	L	Z
L	H	L	L	1, 3, 5, 7	N/A	L	N/A	N/A	L	H	Z
L	H	L	L	0, 2, 4, 6, 8	N/A	H	N/A	N/A	L	L	Z
L	H	L	L	1, 3, 5, 7	N/A	H	N/A	N/A	H	H	Z
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	L	L	Z	N/A	H
L	L	H	L	N/A	1, 3, 5, 7	N/A	L	L	H	Z	N/A
L	L	H	L	N/A	0, 2, 4, 6, 8	N/A	H	L	L	Z	N/A
L	L	H	L	N/A	1, 3, 5, 7	N/A	H	L	H	Z	N/A
L	H	L	H	0, 2, 4, 6, 8	N/A	L	N/A	N/A	H	L	Z
L	H	L	H	1, 3, 5, 7	N/A	L	N/A	N/A	L	H	Z
L	H	L	H	0, 2, 4, 6, 8	N/A	H	N/A	N/A	H	H	Z
L	H	L	H	1, 3, 5, 7	N/A	H	N/A	N/A	L	L	Z
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	L	L	Z	H	Z
L	L	H	H	N/A	1, 3, 5, 7	N/A	L	L	Z	L	Z
L	L	H	H	N/A	0, 2, 4, 6, 8	N/A	H	L	Z	N/A	H
L	L	H	H	N/A	1, 3, 5, 7	N/A	H	L	Z	H	Z
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	L	L	Z	H	Z	H
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	L	L	Z	L	Z	L
L	H	H	L	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	H	Z	H
L	H	H	L	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	L	Z	H
L	H	H	H	0, 2, 4, 6, 8	0, 2, 4, 6, 8	H	H	Z	H	Z	H
L	H	H	H	1, 3, 5, 7	1, 3, 5, 7	H	H	Z	L	Z	L
L	L	L	L	N/A	N/A	N/A	N/A	PE†	Z	PE†	Z
L	L	L	H	N/A	N/A	N/A	N/A	PO‡	Z	PO‡	Z

† Parity output is set to the level so that the specific bus side is set to even parity.

‡ Parity output is set to the level so that the specific bus side is set to odd parity.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVCH 3V	ALVCH 3V	UNIT
I _{CC}	MAX	0.02	0.04	mA
I _{OH}	MAX	-24	-24	mA
I _{OL}	MAX	24	24	mA

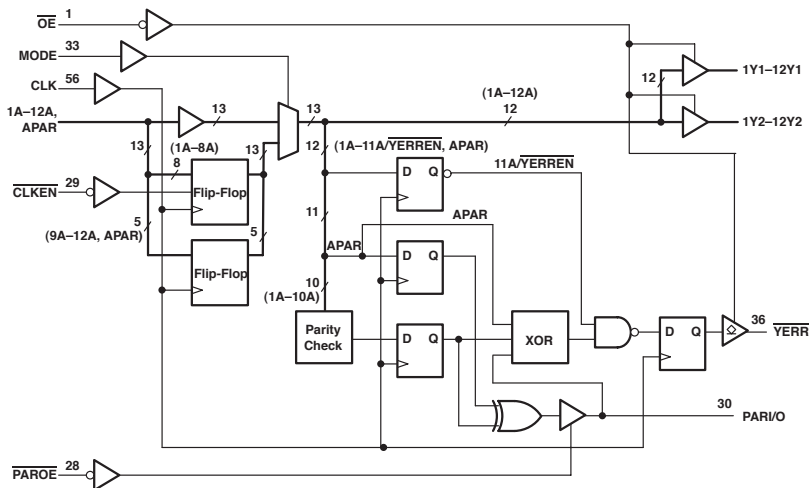
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVCH 3V	ALVCH 3V
f _{max}			MIN	125	125
t _w Pulse duration	CLK ' '		MIN	3	3
	LE high		MIN	3	3
t _{su} Setup time	A, APAR or B, BPAR before CLK ' '		MIN	2.5	1.7
	CLKEN before CLK ' '		MIN	2.5	1.7
	A, APAR or B, BPAR before LE ,		MIN	2	1.2
t _h Hold time	A, APAR or B, BPAR after CLK ' '		MIN	1.3	0.5
	CLKEN after CLK ' '		MIN	1.5	0.7
	A, APAR or B, BPAR after LE ,		MIN	1.7	0.9
I _{PLH}	A or B	B or A	MAX	5.4	4.4
				5.4	4.4
I _{PHL}	A or B	BPAR or APAR	MAX	7.7	6.7
				7.7	6.7
I _{PLH}	APAR or BPAR	BPAR or APAR	MAX	5.7	4.7
				5.7	4.7
I _{PHL}	APAR or BPAR	ERRA or ERBB	MAX	8.5	7.5
				8.5	7.5
I _{PLH}	ODD / EVEN	ERRA or ERBB	MAX	7.8	6.8
				7.8	6.8
I _{PHL}	ODD / EVEN	BPAR or APAR	MAX	7.5	6.5
				7.5	6.5
I _{PLH}	SEL	BPAR or APAR	MAX	6.1	5.1
				6.1	5.1
I _{PLH}	CLKAB or CLKBA	A or B	MAX	6.1	5.1
				6.1	5.1
I _{PHL}	CLKAB or CLKBA	BPAR or APAR parity feedthrough	MAX	6.6	5.6
				6.6	5.6
I _{PLH}	CLKAB or CLKBA	BPAR or APAR parity generated	MAX	8.7	7.7
				8.7	7.7
I _{PHL}	CLKAB or CLKBA	ERRA or ERBB	MAX	8.9	7.9
				8.9	7.9
I _{PLH}	LEAB or LEBA	A or B	MAX	5.8	4.8
				5.8	4.8
I _{PHL}	LEAB or LEBA	BPAR or APAR parity feedthrough	MAX	6.3	5.3
				6.3	5.3
I _{PLH}	LEAB or LEBA	BPAR or APAR parity generated	MAX	8.4	7.4
				8.4	7.4
I _{PHL}	LEAB or LEBA	ERRA or ERBB	MAX	8.5	7.5
				8.5	7.5
I _{PZH}	OEAB or OEBA	B, BPAR or A, APAR	MAX	6.3	5.3
				6.3	5.3
I _{PHZ}	OEAB or OEBA	B, BPAR or A, APAR	MAX	5.9	4.9
				5.9	4.9
I _{PZH}	OEAB or OEBA	ERRA or ERBB	MAX	5.9	4.9
				5.9	4.9
I _{PHZ}	OEAB or OEBA	ERRA or ERBB	MAX	6.7	5.7
				6.7	5.7
I _{PZH}	SEL	ERRA or ERBB	MAX	6.5	5.5
				6.5	5.5
I _{PHZ}	SEL	ERRA or ERBB	MAX	5.9	4.9
				5.9	4.9

UNIT f_{max}: MHz other: ns

3.3-V 12-BIT UNIVERSAL BUS DRIVER WITH PARITY CHECKER AND DUAL 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUTS		
OE	MODE	CLKEN	CLK	A	$1Y_{n1} - 8Y_{n1}†$	$9Y_{n1} - 12Y_{n1}†$
L	L	L	↑	H	H	H
L	L	L	↑	L	L	L
L	L	H	↑	H	Y_0	H
L	L	H	↑	L	Y_0	L
L	H	X	X	H	H	H
L	H	X	X	L	L	L
H	X	X	X	X	Z	Z

† $T_n = 1, 2$

PAR/O FUNCTION†

INPUTS			OUTPUT
PAROE	Σ OF INPUTS $1A - 10A = H$	APAR	PAR/O
L	0, 2, 4, 6, 8, 10	L	L
L	1, 3, 5, 7, 9	L	H
L	0, 2, 4, 6, 8, 10	H	H
L	1, 3, 5, 7, 9	H	L
H	X	X	Z

† This table applies to the first device of a cascaded pair of ALVCH16903 devices.

PARITY FUNCTION

INPUTS						OUTPUT
OE	PAROE†	$11A/YERREN§$	PAR/O	Σ OF INPUTS $1A - 10A = H$	APAR	YERR
L	H	L	L	0, 2, 4, 6, 8, 10	L	H
L	H	L	L	1, 3, 5, 7, 9	L	L
L	H	L	L	0, 2, 4, 6, 8, 10	H	H
L	H	L	L	1, 3, 5, 7, 9	H	L
L	H	L	H	0, 2, 4, 6, 8, 10	L	L
L	H	L	H	1, 3, 5, 7, 9	L	H
L	H	L	H	0, 2, 4, 6, 8, 10	H	H
L	H	L	H	1, 3, 5, 7, 9	H	L
H	X	X	X	X	X	H
L	X	H	X	X	X	H

† When used as a single device, PAROE must be tied high.

§ Valid after appropriate number of clock pulses have set internal register.

RECOMMENDED OPERATING CONDITIONS

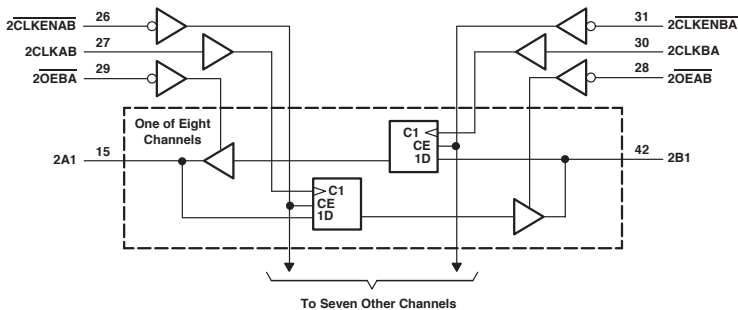
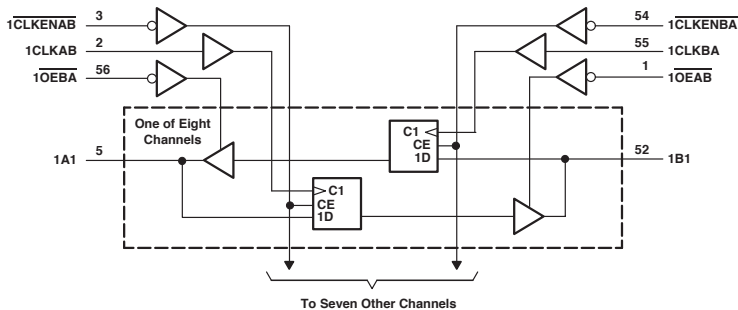
PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH}	MAX	-24	mA
I _{OL}	MAX	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	
f _{max}			MIN	125	
t _w Pulse duration	CLK ' "		MIN	3	
t _{su} Setup time	1A-12A before CLK ' ", resister mode		MIN	1.45	
	1A-10A before CLK ' ", buffer mode		MIN	4.4	
	APAR before CLK ' ", resister mode		MIN	1.3	
	APAR before CLK ' ", buffer mode		MIN	3.1	
	PARI/O before CLK ' ", both mode		MIN	1.7	
	11A/YERREN before CLK ' ", buffer mode		MIN	1.6	
	CLKEN before CLK ' ", resister mode		MIN	2.2	
t _h Hold time	1A-12A after CLK ' ", resister mode		MIN	0.55	
	1A-10A after CLK ' ", buffer mode		MIN	0.25	
	APAR after CLK ' ", resister mode		MIN	0.7	
	APAR after CLK ' ", buffer mode		MIN	0.25	
	PARI/O before CLK ' ", resister mode		MIN	0.4	
	PARI/O before CLK ' ", buffer mode		MIN	0.5	
	11A/YERREN after CLK ' ", buffer mode		MIN	0.4	
	CLKEN after CLK ' ", resister mode		MIN	0.4	
t _{PLH} t _{PHL}	Buffer mode	A	Y	MAX	3.8
					3.8
t _{PLH} t _{PHL}	Both mode	CLK	YERR	MAX	4.4
					4.4
t _{PLH} t _{PHL}	Both mode	CLK	PARI / O	MAX	6.6
					6.6
t _{PLH} t _{PHL}	Both mode	MODE	Y	MAX	4.9
					4.9
t _{PLH} t _{PHL}	Resister mode	CLK	Y	MAX	4.8
					4.6
t _{PZH} t _{PZL}	Both mode	OE	Y	MAX	5.4
					5.4
t _{PZH} t _{PZL}	Both mode	PAROE	PARI / O	MAX	4.8
					4.8
t _{PHZ} t _{PLZ}	Both mode	OE	Y	MAX	5
					5
t _{PHZ} t _{PLZ}	Both mode	PAROE	PARI / O	MAX	3.8
					3.8
t _{PLH} t _{PHL}	Both mode	OE	YERR	MAX	4
					4.2

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
CLKENAB	CLKAB	OEAB	A	B
H	X	L	X	B ₀ †
X	L	L	X	B ₀ †
L	†	L	L	L
L	†	L	H	H
H	X	H	X	Z

† A-to-B data flow is shown; B-to-A data flow is similar but uses CLKENBA, CLKBA, and OEBA.

‡ Level of B before the indicated steady-state input conditions were established.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	AC	LVTH 3V	LVCH 3V	ALVCH 3V	UNIT
I _{CC}	MAX	35	0.08	5	0.02	0.04	mA
I _{OH}	MAX	-32	-24	-32	-24	-24	mA
I _{OL}	MAX	64	24	64	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	AC	LVTH 3V	LVCH 3V	ALVCH 3V
f _{max}			MIN	150	75	150	150	150
t _w Pulse duration	CLKEN high		MIN	-	-	-	-	3.3
	CLK high or low			3.3	6.7	3.3	3.3	3.3
t _{su} Setup time	Data before CLK		MIN	3.5	5	1.7	2.8	1.5
	CLKEN before CLK			3	6.5	2	1.4	1
t _h Hold time	Data after CLK		MIN	1	1	0.8	0.5	0.8
	CLKEN after CLK			1	0	0.4	1.9	1.1
t _{PLH}	CLK	A or B	MAX	4.3	11.8	4.4	6.6	3.9
t _{PHL}				4.5	11.7	4.4	6.6	3.9
t _{PZH}	OEBA or OEAB	A or B	MAX	4.6	11.2	4.9	6.6	4.4
t _{PZL}				6	13	4.9	6.6	4.4
t _{PHZ}	OEBA or OEAB	A or B	MAX	5.5	9.4	6.2	6.7	4
t _{PLZ}				4.2	8.7	5.3	6.7	4

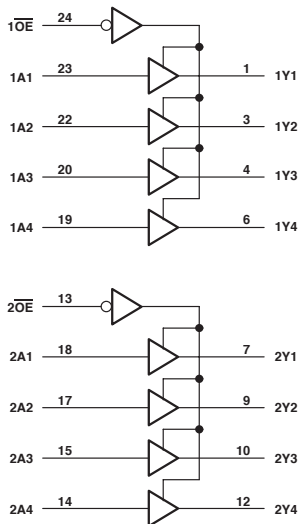
UNIT f_{max}: MHz other: ns

25244

25-Ω OCTAL BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- High Output Drive Current
- Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs

Logic Diagram



FUNCTION TABLE
(each buffer/driver)

INPUTS		OUTPUT
OE	A	Y
L	H	H
L	L	L
H	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	SN64 BCT	UNIT
I_{CC}	MAX	119	119	mA
I_{OH}	MAX	-80	-80	mA
I_{OL}	MAX	188	188	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	SN64 BCT
t_{PLH}	A	Y	MAX	5.5	5.5
t_{PHL}				6	6.3
t_{PZH}	\overline{OE}	Y	MAX	9.3	9.7
t_{PZL}				10.2	10.4
t_{PHZ}	\overline{OE}	Y	MAX	6.3	6.5
t_{PLZ}				8.4	9.5

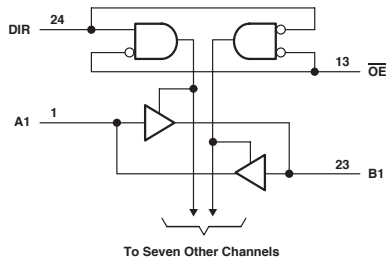
UNIT: ns

25245

25-Ω OCTAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- High Output Drive Current
- Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs

Logic Diagram



FUNCTION TABLE

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	ABTH	UNIT
I_{CC}	MAX	125	20	mA
I_{OH} (A port)	MAX	-80	-80	mA
I_{OH} (B port)	MAX	-3	-32	mA
I_{OL} (A port)	MAX	188	188	mA
I_{OL} (B port)	MAX	24	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT	ABTH
t_{PLH}	A	B	MAX	5.7	3.9
t_{PHL}				7.2	4.3
t_{PLH}	B	A	MAX	5.5	3.9
t_{PHL}				6.2	4.3
t_{PZH}	\overline{OE}	A	MAX	9.6	6.5
t_{PZL}				10.3	6.8
t_{PHZ}	\overline{OE}	A	MAX	6.2	7.2
t_{PLZ}				8.3	6.4
t_{PZH}	\overline{OE}	B	MAX	8.9	6.5
t_{PZL}				9.7	6.8
t_{PHZ}	\overline{OE}	B	MAX	6.9	7.2
t_{PLZ}				7.5	6.4

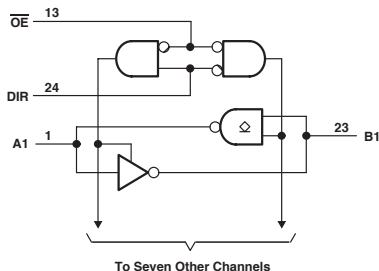
UNIT: ns

25642

25-Ω OCTAL BUS TRANSCEIVER

- High Output Drive Current
- Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs

Logic Diagram



FUNCTION TABLE

INPUTS		OPERATION
OE	DIR	
L	L	\bar{B} data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
I_{CC}	MAX	125	mA
I_{OH} (B port)	MAX	-3	mA
I_{OL} (A port)	MAX	188	mA
I_{OL} (B port)	MAX	24	mA
V_{OH} (A port)	MAX	5.5	V

SWITCHING CHARACTERISTICS

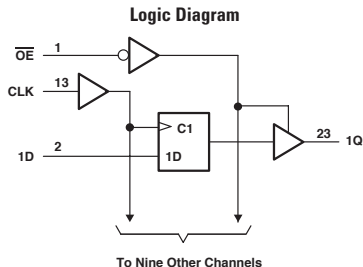
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
t_{PLH}	A	B	MAX	6.2
t_{PHL}				4
t_{PLH}	B	A	MAX	6.3
t_{PHL}				5.9
t_{PLH}	\overline{OE}	A	MAX	11.6
t_{PHL}				11.3
t_{PZH}	\overline{OE}	B	MAX	9.1
t_{PZL}				9.8
t_{PHZ}	\overline{OE}	B	MAX	7.3
t_{PLZ}				7.3

UNIT: ns

29821

10-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Outputs
- Data Flow-Through Pinout



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
I _{CC}	MAX	115	35	mA
I _{OH}	MAX	-24	-24	mA
I _{OL}	MAX	48	48	mA

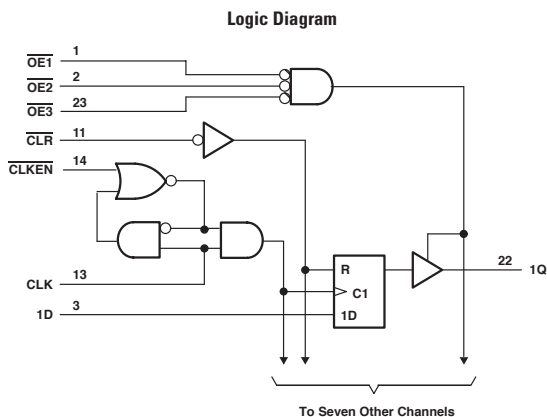
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
f _{max}				-	125
t _w Pulse duration	CLK high or low		MIN	7	7
t _{su} Setup time	Data before CLK ' "		MIN	4	7
t _h Hold time	Data after CLK ' "		MIN	2	1
t _{PLH}	CLK	Q	MAX	10	12
t _{PHL}				10	10
t _{PZH}	OE	Q	MAX	14	12
t _{PZL}				14	13
t _{PHZ}	OE	Q	MAX	14	8
t _{PLZ}				12	8

UNIT f_{max} : MHz other : ns

8-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- 3-State Outputs
- Data Flow-Through Pinout



FUNCTION TABLE

INPUTS					D	OUTPUT Q
OE†	CLR	CLKEN	CLK	D		
L	L	X	X	X	L	
L	H	L	↑	H	H	
L	H	L	↑	L	L	
L	H	H	H or L	X	Q ₀	
H	X	X	X	X	Z	

† OE = H if any of the output-enable inputs is high.
OE = L if all of the output-enable inputs are low.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	SN74 BCT	UNIT
I _{CC}	MAX	40	mA
I _{OH}	MAX	-24	mA
I _{OL}	MAX	48	mA

SWITCHING CHARACTERISTICS

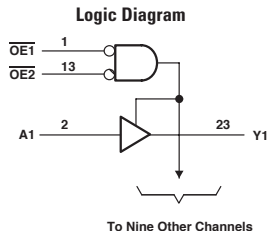
PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
f _{max}			MIN	125
t _w Pulse duration	CLK low		MIN	4
	CLK high or low		MIN	4
t _{su} Setup time	Before CLK ↑, data high		MIN	6
	Before CLK ↑, data low		MIN	3.5
	CLR		MIN	1
	CLKEN before CLK ↑		MIN	8
t _h Hold time	After CLK ↑, data high		MIN	1.5
	After CLK ↑, data low		MIN	0
	CLKEN after CLK ↑		MIN	0.5
t _{PLH}	CLK	Q	MAX	9
			8.4	
t _{PHL}	CLR	Q	MAX	9.5
t _{PZH}	OE	Q	MAX	10.3
			10.2	
t _{PHZ}	OE	Q	MAX	9
			8.2	

UNIT f_{max}: MHz other: ns

29827

10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

- pnp Inputs Reduce dc Loading
- 3-State Outputs
- Data Flow-Through Pinout



FUNCTION TABLE

INPUT			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
L	X	X	Z
H	H	X	Z

$t_{\text{tr}} = 1,2$

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
I_{CC}	MAX	40	40	mA
I_{OH}	MAX	-24	-24	mA
I_{OL}	MAX	48	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
t_{PLH}	A	Y	MAX	7	5.5
t_{PHL}				7.5	7.5
t_{PZH}	$\overline{\text{OE}}$	Y	MAX	15	9.1
t_{PZL}				15	12.8
t_{PHZ}	$\overline{\text{OE}}$	Y	MAX	17	8.8
t_{PLZ}				12	8.4

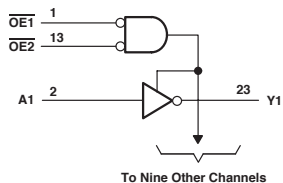
UNIT: ns

29828

10-BIT BUFFERS AND BUS DRIVERS WITH 3-STATE OUTPUTS

- pnp Inputs Reduce dc Loading
- 3-State Outputs
- Data Flow-Through Pinout

Logic Diagram



RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	UNIT
I_{CC}	MAX	40	mA
I_{DH}	MAX	-24	mA
I_{OL}	MAX	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS
t_{PLH}	A	Y	MAX	7
t_{PHL}				7.5
t_{PZH}	\overline{OE}	Y	MAX	15
t_{PZL}				15
t_{PHZ}	\overline{OE}	Y	MAX	17
t_{PLZ}				12

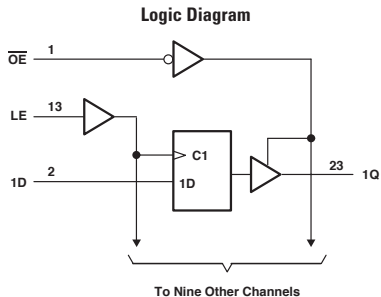
UNIT: ns

NOTICE : ALS IS NOT RECOMMENDED FOR NEW DESIGNS

29841

10-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Outputs
- Data Flow-Through Pinout



FUNCTION TABLE

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
I _{CC}	MAX	85	35	mA
I _{OH}	MAX	-24	-24	mA
I _{OL}	MAX	48	48	mA

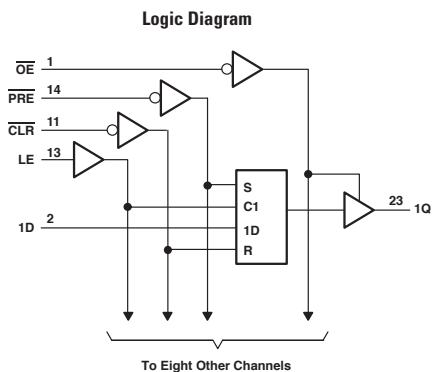
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
t _w Pulse duration	LE high or low		MIN	6	4
t _{su} Setup time	Data before LE ,		MIN	2.5	2
t _h Hold time	Data after LE , , high		MIN	4.5	1.5
	Data after LE , , low		MIN	4.5	3.5
t _{PLH}	D	Q	MAX	9.5	7.5
t _{PHL}				9.5	8.6
t _{PLH}	LE	Q	MAX	12	8.6
t _{PHL}				12	8.1
t _{PZH}	OE	Q	MAX	14	9.2
t _{PZL}				14	12.8
t _{PHZ}	OE	Q	MAX	15	6.9
t _{PLZ}				12	6.9

UNIT: ns

9-BIT BUS INTERFACE D-TYPE LATCHES WITH 3-STATE OUTPUTS

- 3-State Outputs
- Data Flow-Through Pinout



FUNCTION TABLE

INPUTS					OUTPUT
PRE	CLR	OE	LE	D	Q
L	X	L	X	X	H
H	L	L	X	X	L
H	H	L	H	L	L
H	H	L	H	H	H
H	H	L	L	X	Q ₀
X	X	H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

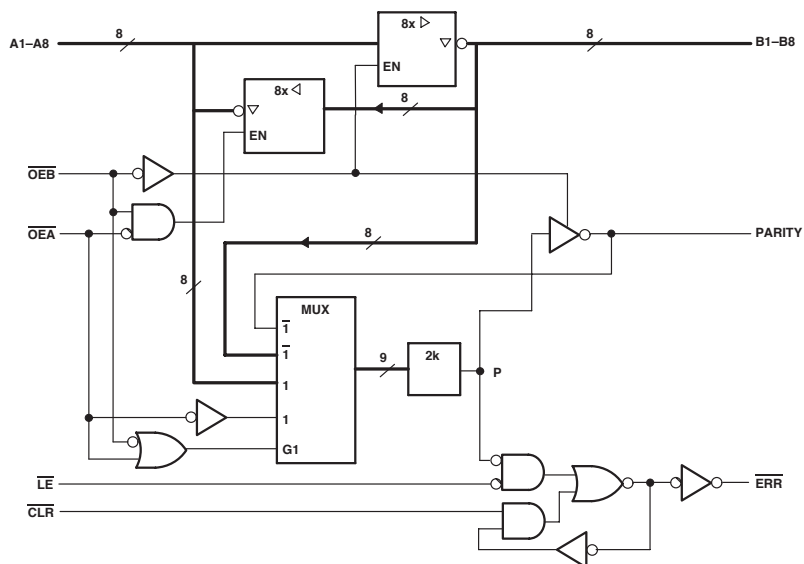
PARAMETER	MAX or MIN	SN74 BCT	UNIT
I _{CC}	MAX	35	mA
I _{OH}	MAX	-24	mA
I _{OL}	MAX	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	SN74 BCT
t _w Pulse duration	$\overline{\text{PRE}}$ low		MIN	7
	$\overline{\text{CLR}}$ low			5
	LE high			4
t _{su} Setup time	Data before LE , high or low		MIN	1.5
	$\overline{\text{PRE}}$ or CLR inactive			2
t _h Hold time	Data after LE , high or low		MIN	3.5
t _{PLH}	$\overline{\text{D}}$	Q	MAX	8
t _{PHL}				9
t _{PLH}	LE	Q	MAX	10
t _{PHL}				10
t _{PLH}	$\overline{\text{PRE}}$	Q	MAX	12
t _{PHL}				12
t _{PLH}	$\overline{\text{CLR}}$	Q	MAX	12
t _{PHL}				12
t _{PZH}	$\overline{\text{OE}}$	Q	MAX	15
t _{PZL}				15
t _{PHZ}	$\overline{\text{OE}}$	Q	MAX	8
t _{PLZ}				8

UNIT: ns

Logic Diagram



FUNCTION TABLE

INPUTS						OUTPUT AND I/O				OPERATION
OEB	OEA	CLR	LE	Ai Σ of Hs Σ of Ls	Bi† Σ of Ls	A	B	PARITY	ERR‡	
L	H	X	X	Odd Even	NA	NA	\bar{A}	H L	NA	\bar{A} data to B bus and generate parity
H	L	X	L	NA	Odd Even	\bar{B}	NA	NA	H L	\bar{B} data to A bus and check parity
H	L	H	H	NA	X	X	NA	NA	N-1	Store error flag
X	X	L	H	X	X	X	NA	NA	H	Clear error-flag register
H	H	X	H	X	X	Z	Z	Z	NC	Isolation§
			L	H					H	
			X	L					H	
L	L	X	X	Odd Even	NA	NA	\bar{A}	L H	NA	A data to B bus and generate inverted parity

NA = not applicable, NC = no change, X = don't care

† Summation of high-level inputs includes PARITY along with Bi inputs.

‡ Output states Shown assume ERR was previously high.

§ In this mode, ERR, when enabled, shows inverted parity of the A bus.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
I _{CC}	MAX	100	80	mA
I _{OH}	MAX	-24	-24	mA
I _{OL}	MAX	48	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
t _w Pulse duration	\bar{LE} high		MIN	10	-
	\bar{LE} low		MIN	10	10
	CLR low		MIN	10	10
t _{su} Setup time	Before \bar{LE} , Bi and PARITY		MIN	10	18
	Before \bar{LE} , CLR high		MIN	15	-
t _h Hold time	Bi and PARITY after \bar{LE}		MIN	3	8
t _{PLH}	A or B	B or A	MAX	8	8
t _{PHL}				8	8
t _{PLH}	A	PARITY	MAX	15	15
t _{PHL}				18	15
t _{PZH}	\bar{OEA} or \bar{OEB}	A or B	MAX	17	17
t _{PZL}				17	19
t _{PHZ}	\bar{OEA} or \bar{OEB}	A or B	MAX	15	15
t _{PLZ}				8	17
t _{PHL}	\bar{LE}	\bar{ERR}	MAX	12	9
t _{PLH}	CLR	ERR	MAX	12	15
t _{PLH}	\bar{OEA}	PARITY	MAX	17	15
t _{PHL}				19	16
t _{PLH}	Bi / PARITY	\bar{ERR}	MAX	20	20
t _{PHL}				20	15

UNIT: ns

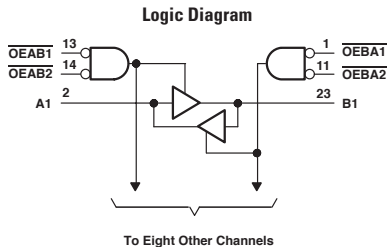
29863

9-BIT BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- True Outputs

FUNCTION TABLE

INPUTS				OPERATION
$\overline{OEAB1}$	$\overline{OEAB2}$	$\overline{OEBA1}$	$\overline{OEBA2}$	
L	L	L	L	Latch A and B
L	L	H	X	A to B
L	L	X	H	A to B
H	X	L	L	B to A
X	H	L	L	B to A
H	X	H	X	Isolation
H	X	X	H	
X	H	X	H	
X	H	H	X	



RECOMMENDED OPERATING CONDITIONS

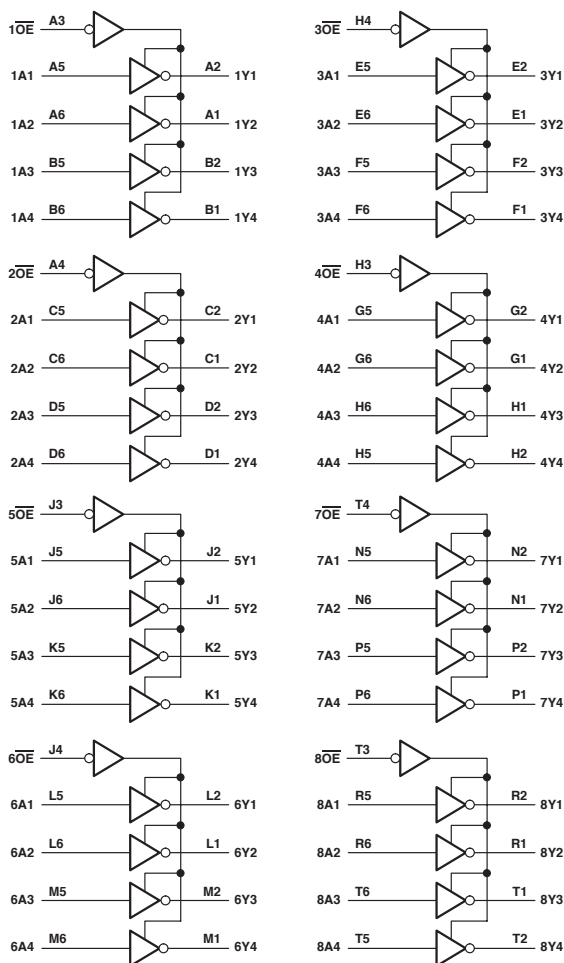
PARAMETER	MAX or MIN	ALS	SN74 BCT	UNIT
I_{CC}	MAX	65	45	mA
I_{OH}	MAX	-24	-24	mA
I_{OL}	MAX	48	48	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALS	SN74 BCT
t_{PLH}	A or B	B or A	MAX	8	5
t_{PHL}				8	7.5
t_{PZH}	\overline{OEAB} or \overline{OEBA}	A or B	MAX	15	8.4
t_{PZL}				15	12.6
t_{PHZ}	\overline{OEAB} or \overline{OEBA}	A or B	MAX	17	8.8
t_{PLZ}				12	8.1

UNIT: ns

Logic Diagram



FUNCTION TABLE

(each 4bit buffer/driver)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	L
L	L	H
H	X	Z

RECOMMENDED OPERATING CONDITIONS

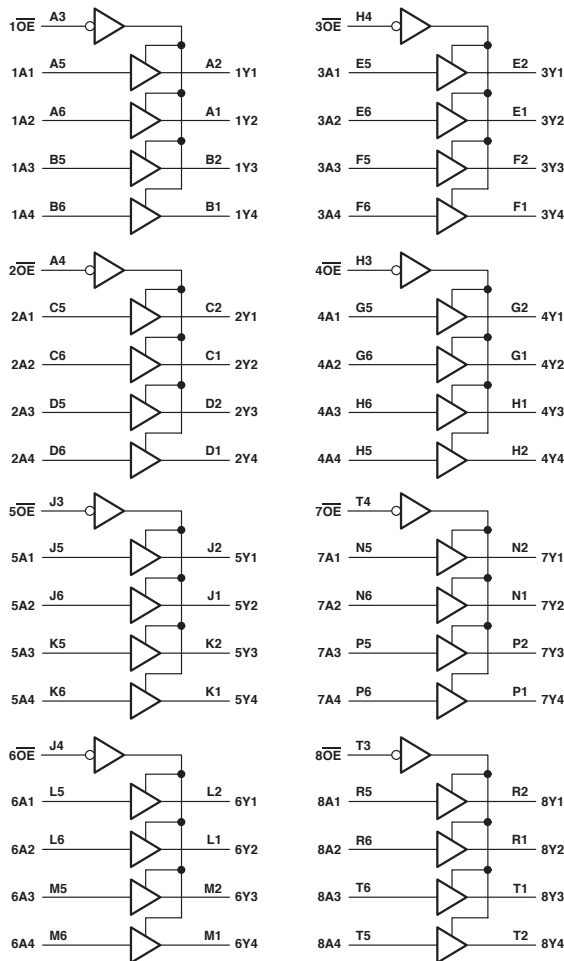
PARAMETER	MAX or MIN	LVT	UNIT
I_{CC}	MAX	10	mA
I_{OH}	MAX	-32	mA
I_{OL}	MAX	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT
t_{PLH}	A	Y	MAX	3.5
t_{PHL}			MAX	3.5
t_{PZH}	\overline{OE}	Y	MAX	4
t_{PZL}			MAX	4.4
t_{PHZ}	\overline{OE}	Y	MAX	4.5
t_{PLZ}			MAX	4.2

UNIT:ns

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT Y
\overline{OE}	A	
L	H	H
L	L	L
H	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVT 3V	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	ALVCH 3V	UNIT
I_{CC}	MAX	10	10	5	0.02	0.02	0.04	mA
I_{OH}	MAX	-32	-32	-32	-24	-24	-24	mA
I_{OL}	MAX	64	64	64	24	24	24	mA

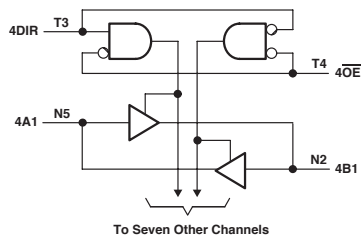
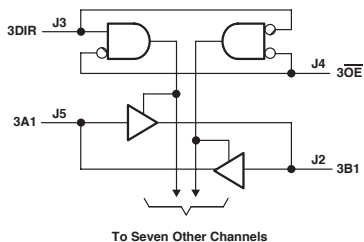
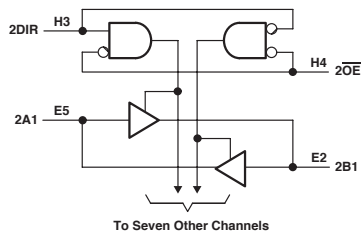
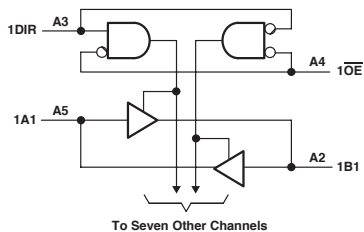
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT 3V	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	ALVCH 3V
t_{PLH}	A	Y	MAX	3.2	3.2	2.4	4.1	4.1	3
t_{PHL}				3.2	3.2	2.5	4.1	4.1	3
t_{PZH}	\overline{OE}	Y	MAX	4	4	3.8	4.6	4.6	4.4
t_{PZL}				4	4	2.9	4.6	4.6	4.4
t_{PHZ}	\overline{OE}	Y	MAX	4.5	4.5	4.2	5.8	5.8	4.1
t_{PLZ}				4.2	4.2	3.6	5.8	5.8	4.1

UNIT: ns

36-BIT BUS TRANSCEIVER WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each 9-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

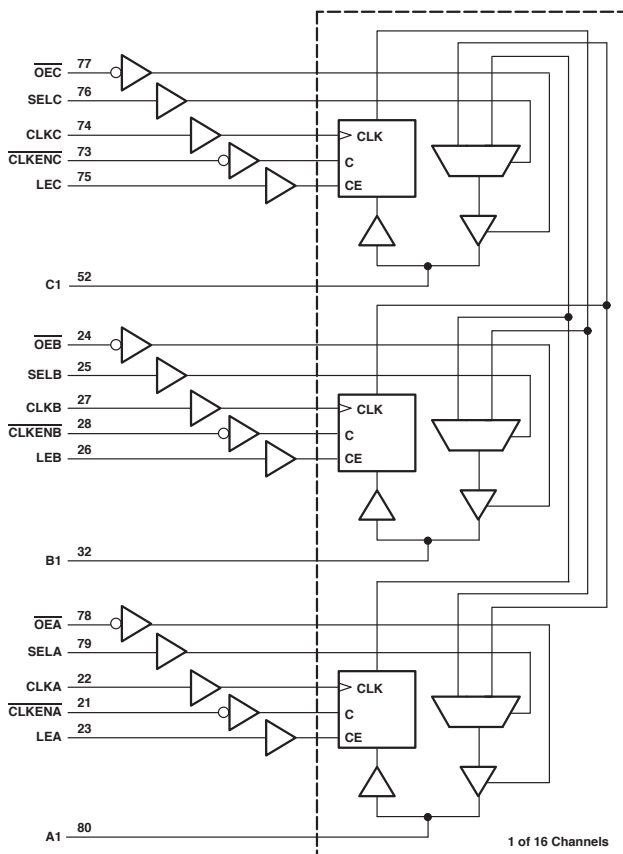
PARAMETER	MAX or MIN	ABTH	LVTH 3V	LVC 3V	LVCH 3V	ALVCH 3V	UNIT
I_{CC}	MAX	20	10	0.04	0.02	0.04	mA
I_{OH}	MAX	-32	-32	-24	-24	-24	mA
I_{OL}	MAX	64	64	24	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH	LVTH 3V	LVC 3V	LVCH 3V	ALVCH 3V
t_{PLH}	A or B	B or A	MAX	5	3.3	4	4	3
t_{PHL}				5.2	3.3	4	4	3
t_{PZH}	\overline{OE}	B or A	MAX	7.3	4.5	5.5	5.5	4.4
t_{PZL}				8.1	4.6	5.5	5.5	4.4
t_{PHZ}	\overline{OE}	B or A	MAX	6.5	5.1	6.6	6.6	4.1
t_{PLZ}				6.9	5.1	6.6	6.6	4.1

UNIT: ns

Logic Diagram



**FUNCTION TABLE
STORAGE†**

INPUTS				OUTPUT
CLKENA	CLKA	LEA	A	
H	X	L	X	Q ₀ ‡
L	†	L	L	L
L	†	L	H	H
X	H	L	X	Q ₀ ‡
X	L	L	X	Q ₀ ‡
X	X	H	L	L
X	X	H	H	H

† A-port register shown. B and C ports are similar but use CLKENB, CLKENG, CLKB, CLKC, LEB, and LEC.

‡ Output level before the indicated steady-state input conditions were established.

A-PORT OUTPUT

INPUTS		OUTPUT A
OEA	SELA	
H	X	Z
L	H	Output of C register
L	L	Output of B register

B-PORT OUTPUT

INPUTS		OUTPUT B
OEB	SELB	
H	X	Z
L	H	Output of A register
L	L	Output of C register

C-PORT OUTPUT

INPUTS		OUTPUT C
OEC	SELC	
H	X	Z
L	H	Output of B register
L	L	Output of A register

RECOMMENDED OPERATING CONDITIONS

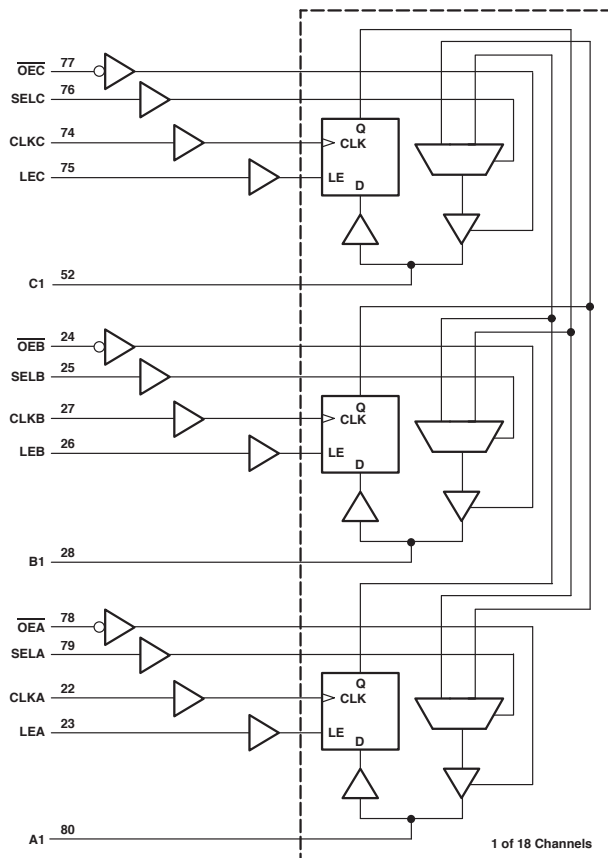
PARAMETER	MAX or MIN	ABTH	UNIT
I _{CC}	MAX	40	mA
I _{DH}	MAX	-32	mA
I _{OL}	MAX	64	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
f _{max}			MIN	150
t _w Pulse duration	LE high		MIN	3.3
	CLK high or low		MIN	3.3
t _{su} Setup time	A, B, or C before CLK *		MIN	2.4
	A or B before LE ,		MIN	2.1
t _h Hold time	CLKEN* before CLK *		MIN	3.2
	A, B, or C after CLK *		MIN	1.4
	A or B after LE ,		MIN	2.1
	CLKEN* after CLK *		MIN	1.1
t _{PLH}	A, B, or C	C, B, or A	MAX	6.1
t _{PHL}			6.6	
t _{PLH}	SEL	A, B, or C	MAX	6.5
t _{PHL}			6.5	
t _{PLH}	LE	A, B, or C	MAX	7.5
t _{PHL}			6.7	
t _{PZH}	\overline{OE}	A, B, or C	MAX	6.4
t _{PZL}			6.8	
t _{PHZ}	\overline{OE}	A, B, or C	MAX	6
t _{PLZ}			6.1	

UNIT f_{max} : MHz other : ns

Logic Diagram



**FUNCTION TABLE
STORAGE†**

INPUTS			OUTPUT
CLKA	LEA	A	
↑	L	L	L
↑	L	H	H
H	L	X	Q ₀ ‡
L	L	X	Q ₀ ‡
X	H	L	L
X	H	H	H

† A-port register shown. B and C ports are similar but use CLKB, CLKC, LEB, and LEC.

‡ Output level before the indicated steady-state input conditions were established.

A-PORT OUTPUT

INPUTS		OUTPUT A
OEA	SELA	
H	X	Z
L	H	Output of A register
L	L	Output of B register

B-PORT OUTPUT

INPUTS		OUTPUT B
OEB	SELB	
H	X	Z
L	H	Output of A register
L	L	Output of C register

C-PORT OUTPUT

INPUTS		OUTPUT C
OEC	SELC	
H	X	Z
L	H	Output of B register
L	L	Output of A register

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABTH	UNIT
I _{CC}	MAX	45	mA
I _{OH}	MAX	-32	mA
I _{OL}	MAX	64	mA

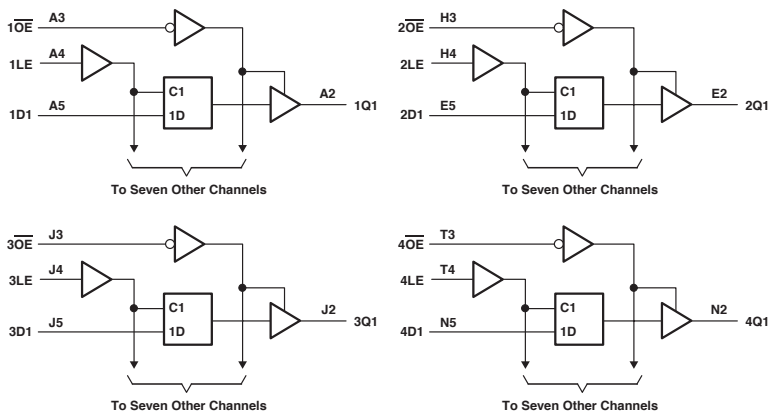
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
f _{max}			MIN	150
t _w Pulse duration	LE high		MIN	3.3
	CLK high or low		MIN	3.3
t _{su} Setup time	A, B, or C before CLK *		MIN	2.4
	A, B, or C before LE *		MIN	2.1
t _h Hold time	A, B, or C after CLK *		MIN	1.4
	A, B, or C after LE *		MIN	2.1
t _{PLH}	A, B, or C	C, B, or A	MAX	6.1
t _{PHL}				6.6
t _{PLH}	SEL	A, B, or C	MAX	6.5
t _{PHL}			6.5	
t _{PLH}	LE	A, B, or C	MAX	7.5
t _{PHL}			6.9	
t _{PLH}	CLK	A, B, or C	MAX	7.4
t _{PHL}			6.7	
t _{PHZ}	\overline{OE}	A, B, or C	MAX	6.8
t _{PZL}			7.1	
t _{PHZ}	\overline{OE}	A, B, or C	MAX	6.2
t _{PLZ}			6	

UNIT f_{max} : MHz other : ns

32-BIT TRANSPARENT D-TYPE LATCH WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	ALVTH 3V	LVCH 3V	UNIT
I _{CC}	MAX	10	5	0.02	mA
I _{OH}	MAX	-32	-32	-24	mA
I _{OL}	MAX	64	64	24	mA

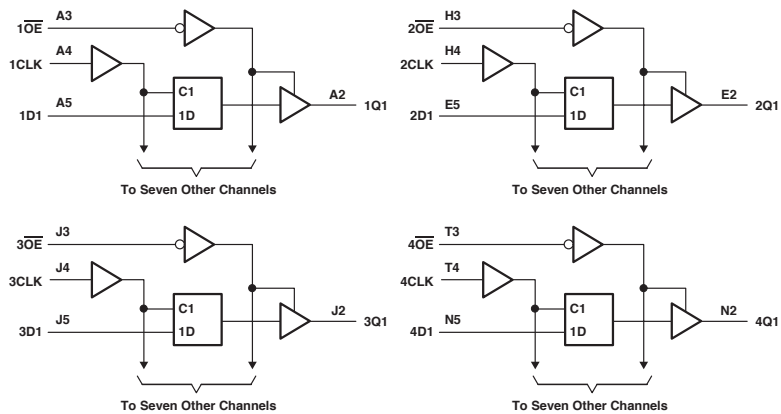
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVTH 3V	LVCH 3V
t _w Pulse duration, LE high or low			MIN	3	1.5	3.3
t _{su} Setup time	Data before LE , data high		MIN	1	1.4	1.7
	Data before LE , data low		MIN	1	0.9	1.7
t _h Hold time	Data after LE , data high		MIN	1	0.9	1.2
	Data after LE , data low		MIN	1	1.4	1.2
t _{PLH}	D	Q	MAX	3.8	3.1	4.2
t _{PHL}				3.6	3.3	4.2
t _{PLH}	LE	Q	MAX	4.3	3.3	4.6
t _{PHL}				4	3.5	4.6
t _{PZH}	\overline{OE}	Q	MAX	4.3	4	4.7
t _{PZL}				4.3	3.4	4.7
t _{PHZ}	\overline{OE}	Q	MAX	5	4.9	5.9
t _{PLZ}				4.7	4.5	5.9

UNIT: ns

32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
OE	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	H or L	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

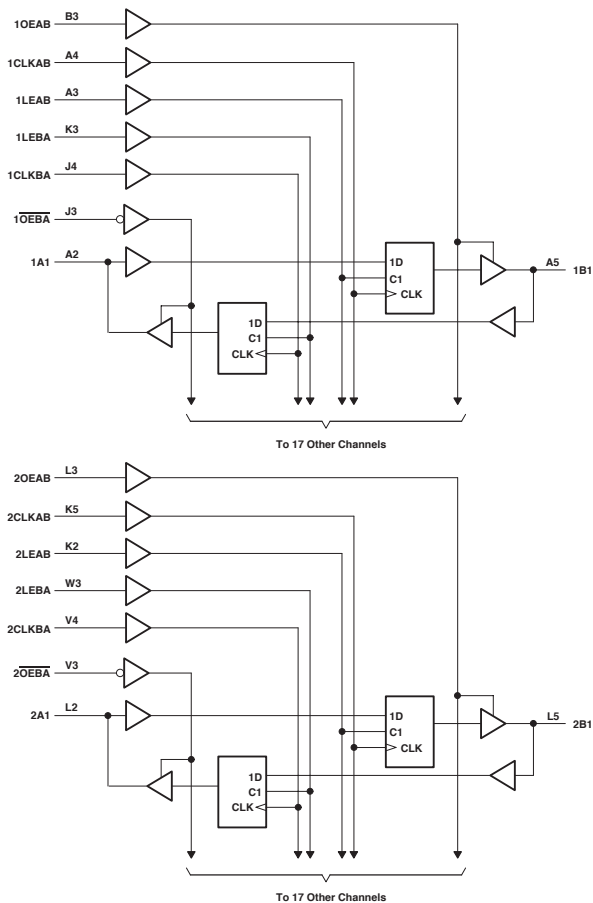
PARAMETER	MAX or MIN	LVTH 3V	ALVTH 3V	LVCH 3V	ALVCH 3V	UNIT
I _{CC}	MAX	10	5	0.02	0.04	mA
I _{OH}	MAX	-32	-32	-24	-24	mA
I _{OL}	MAX	64	64	24	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVTH 3V	LVCH 3V	ALVCH 3V
f _{max}				160	250	150	150
t _w Pulse duration, CLK high or low			MIN	3	1.5	3.3	3.3
t _{su} Setup time	Data before CLK ↑, data high		MIN	1.8	1	1.9	1.9
	Data before CLK ↑, data low		MIN	1.8	1.5	1.9	1.9
t _h Hold time	Data after CLK ↑, data high		MIN	0.8	0.5	1.1	0.5
	Data after CLK ↑, data low		MIN	0.8	1	1.1	0.5
t _{PLH}	CLK	Q	MAX	4.5	3.2	4.5	4.2
t _{PHL}				4	3.2	4.5	4.2
t _{PZH}	OE	Q	MAX	4.5	3.8	4.6	4.8
t _{PZL}				4.4	3.3	4.6	4.8
t _{PHZ}	OE	Q	MAX	5	4.6	5.5	4.3
t _{PLZ}				4.6	4.2	5.5	4.3

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE†

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	L
H	L	†	L	L
H	L	†	H	H
H	L	H	X	B ₀ †
H	L	L	X	B ₀ §

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

RECOMMENDED OPERATING CONDITIONS

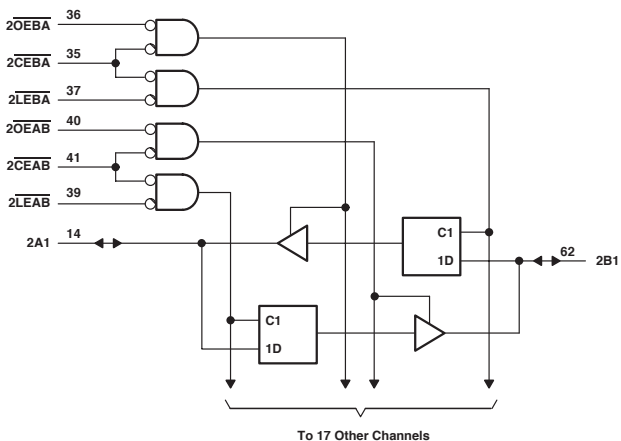
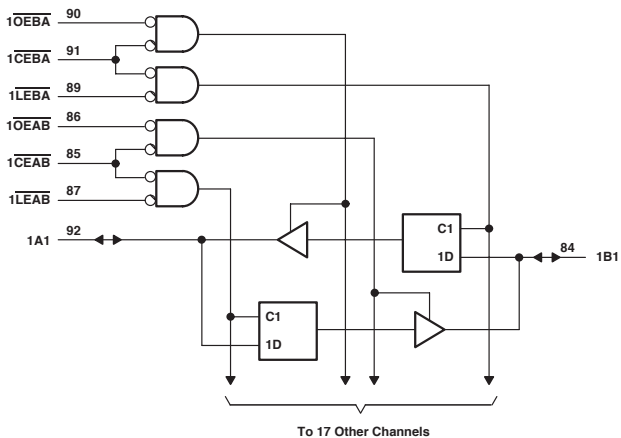
PARAMETER	MAX or MIN	ABTH	ALVCH 3V	UNIT
I _{CC}	MAX	90	0.02	mA
I _{QH}	MAX	-32	-24	mA
I _{OL}	MAX	64	24	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH	ALVCH 3V
f _{max}			MIN	150	150
t _w Pulse duration	LEAB or LEBA high		MIN	3.3	3.3
	CLKAB or CLKBA high or low		MIN	3.3	3.3
t _{su} Setup time	A before CLKAB *		MIN	3.5	1.7
	B before CLKBA *		MIN	3.5	1.7
	A before LEAB , or LEBA , CLK high		MIN	1.6	1.5
	A before LEAB , or LEBA , CLK low		MIN	1.6	1
t _h Hold time	A after CLKAB * or B after CLKBA *		MIN	0	0.7
	A after LEAB , or B after LEBA ,		MIN	1.6	1.4
t _{PLH}	A or B	B or A	MAX	4.8	3.9
t _{PHL}				5.4	3.9
t _{PZH}	LEAB or LEBA	B or A	MAX	5.3	4.6
t _{PZL}				5.5	4.6
t _{PHZ}	CLKAB or CLKBA	B or A	MAX	5.3	4.9
t _{PLZ}				5.4	4.9
t _{PZH}	OEAB	B	MAX	5.6	4.6
t _{PZL}				6	4.6
t _{PHZ}	OEAB	B	MAX	5.9	5
t _{PLZ}				5.6	5
t _{PZH}	OEBA	A	MAX	5.6	5
t _{PZL}				6	5
t _{PHZ}	OEBA	A	MAX	5.9	4.2
t _{PLZ}				5.6	4.2

UNIT f_{max} : MHz other : ns

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
CEAB	LEAB	OEAB	A	Y
H	X	X	X	Z
X	X	H	X	Z
L	H	L	X	B_0^\ddagger
L	L	L	L	L
L	L	L	H	H

† A-to-B data flow is shown; B-to-A flow conditions is the same that it uses CEBA, LEBA, and OEBA.
 ‡ Output level before the indicated steady-state input conditions were established.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABTH	UNIT
Icc	MAX	20	mA
Ioh	MAX	-32	mA
Iol	MAX	64	mA

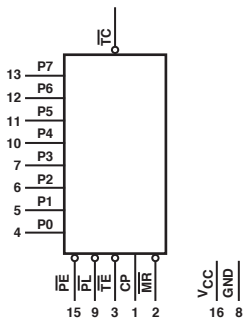
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
t _w Pulse duration, \overline{LEAB} or \overline{LEBA} low			MIN	3.3
t _{su} Setup time	Data before \overline{LEAB} ' or \overline{LEBA} '		MIN	2.1
	Data before \overline{CEAB} ' or \overline{CEBA} '		MIN	1.7
t _h Hold time	Data after \overline{LEAB} ' or \overline{LEBA} '		MIN	0.6
	Data after \overline{CEAB} ' or \overline{CEBA} '		MIN	0.9
t _{PLH}	A or B	B or A	MAX	5.9
t _{PHL}				5.7
t _{PLH}	\overline{LE}	A or B	MAX	7.5
t _{PHL}				6.6
t _{PZH}	\overline{CE}	A or B	MAX	8
t _{PZL}				8.8
t _{PHZ}	\overline{CE}	A or B	MAX	7.1
t _{PLZ}				7.5
t _{PZH}	\overline{OE}	A or B	MAX	7.3
t _{PZL}				8.1
t _{PHZ}	\overline{OE}	A or B	MAX	6.5
t _{PLZ}				6.9

UNIT: ns

8-STAGE SYNCHRONOUS DOWN COUNTERS

Logic Diagram



FUNCTION TABLE

CONTROL INPUTS				PRESET MODE	ACTION
MR	PL	PE	TE		
L	X	X	L	Synchronous	Inhibit Counter Count Down
X	H	X	L	Asynchronously	Preset On Next Positive Clock Transition
X	X	L	L		Preset Asynchronously
H	L	H	L		Clear to Maximum Count

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	CD74 HC	CD74 HCT	UNIT
I_{CC}	MAX	0.16	0.16	mA
I_{OH}	MAX	-4	-4	mA
I_{OL}	MAX	4	4	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	CD74 HC	CD74 HCT
t_w	CP	\overline{TC}	MIN	50	53
	\overline{PL}			38	63
	MR			38	53
t_{su}	P to CP	\overline{TC}	MIN	30	36
	\overline{PE} to CP			22	30
	\overline{TE} to CP			45	60
t_h	P to CP	\overline{TC}	MIN	5	5
	\overline{TE} to CP			0	0
	\overline{PE} to CP			2	2
t_{PLH}	CP	\overline{TC} (Async Preset)	MAX	90	90
t_{PHL}				90	90
t_{PLH}	CP	\overline{TC} (Sync Preset)	MAX	90	95
t_{PHL}				90	95
t_{PLH}	\overline{TE}	\overline{TC}	MAX	60	75
t_{PHL}				60	75
t_{PLH}	\overline{PL}	\overline{TC}	MAX	83	102
t_{PHL}				83	102
t_{PLH}	MR	\overline{TC}	MAX	83	83
t_{PHL}				83	83

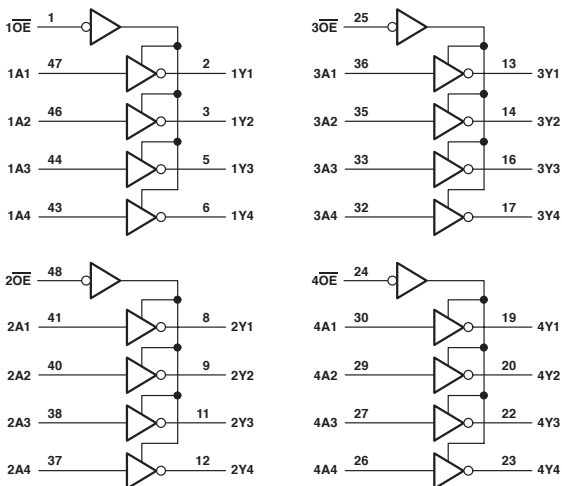
UNIT:ns

162240

3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74LVT162240, SN74LVTH162240: Output Ports Have Equivalent 22-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
OE	A	Y
L	H	L
L	L	H
H	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVT 3V	LVTH 3V	UNIT
I _{CC}	MAX	5	5	mA
I _{OH}	MAX	-12	-12	mA
I _{OL}	MAX	12	12	mA

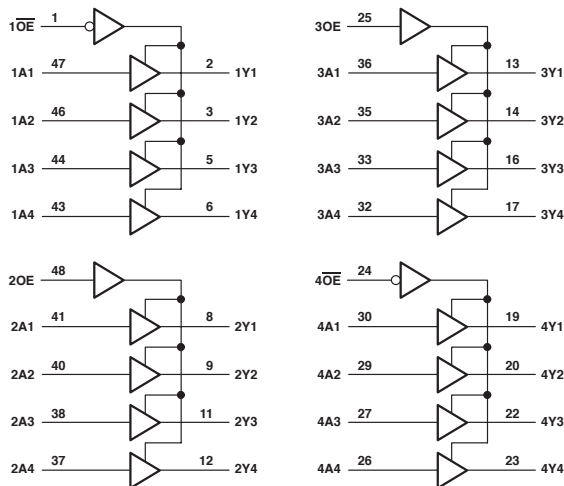
SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVT 3V	LVTH 3V
t _{PLH}	A	Y	MAX	4	4
t _{PHL}				4	4
t _{PZH}	OE	Y	MAX	4.8	4.8
t _{PZL}				4.7	4.7
t _{PHZ}	OE	Y	MAX	4.7	4.7
t _{PLZ}				4.5	4.5

UNIT: ns

3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUT
1OE, 4OE	1A, 4A		1Y, 4Y
L	H		H
L	L		L
H	X		Z

INPUTS			OUTPUT
2OE, 3OE	2A, 3A		2Y, 3Y
H	H		H
H	L		L
L	X		Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	UNIT
I _{CC}	MAX	5	mA
I _{OH}	MAX	-12	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

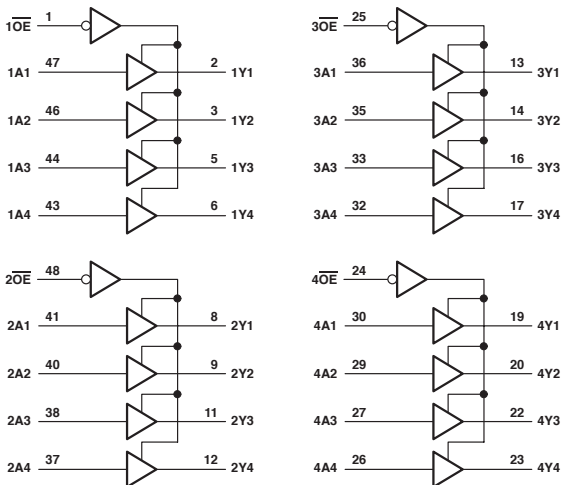
PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V
t _{PLH}	A	Y	MAX	4.1
t _{PHL}				4.1
t _{PZH}	$\overline{0E}$ or $0E$	Y	MAX	4.9
t _{PZL}				4.8
t _{PHZ}	$\overline{0E}$ or $0E$	Y	MAX	5.3
t _{PHZ}				4.9

UNIT: ns

16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74ABT162244: Output Ports Have Equivalent 25- Ω Series Resistors
- SN74LVT162244A, LVTH162244: Output Ports Have Equivalent 22- Ω Series Resistors
- SN74ALVTH162244: Output Ports Have Equivalent 30- Ω Series Resistors
- SN74LVC162244A: Output Ports Have Equivalent 26- Ω Series Resistors
- SN74LVCH162244A: Output Ports Have Equivalent 26- Ω Series Resistors
- SN74ALVCH162244: Output Ports Have Equivalent 26- Ω Series Resistors

Logic Diagram

FUNCTION TABLE
(each 4-bit buffer)

INPUTS		OUTPUT
\overline{OE}	A	Y
L	H	H
L	L	L
H	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	ALVCH 3V	UNIT
I_{CC}	MAX	30	5	5	5	0.02	0.02	0.04	mA
I_{OH}	MAX	-12	-12	-12	-12	-12	-12	-12	mA
I_{OL}	MAX	12	12	12	12	12	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	LVT 3V	LVTH 3V	ALVTH 3V	LVC 3V	LVCH 3V	ALVCH 3V
t_{PLH}	A	Y	MAX	3.9	4	4	3.3	4.4	4.4	4.2
t_{PHL}				4.8	3.6	3.6	3.3	4.4	4.4	4.2
t_{PZH}	\overline{OE}	Y	MAX	5.4	5.1	5.1	4.9	5.5	5.5	5.6
t_{PZL}				5.1	4.5	4.5	3.3	5.5	5.5	5.6
t_{PHZ}	\overline{OE}	Y	MAX	4.6	5	5	4.9	6.3	6.3	5.5
t_{PLZ}				4.5	5	5	4.3	6.3	6.3	5.5

UNIT: ns

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
OE	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALVTH 3V	LVCR 3V	UNIT
I _{CC}	MAX	32	32	5	5	5	0.02	mA
I _{OH} (A port)	MAX	-12	-12	-12	-12	-12	-12	mA
I _{OH} (B port)	MAX	-32	-32	-32	-32	-32	-12	mA
I _{OL} (A port)	MAX	12	12	12	12	12	12	mA
I _{OL} (B port)	MAX	64	64	64	64	64	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ABTH	LVT 3V	LVTH 3V	ALVTH 3V	LVC 3V
t _{PLH}	A	B	MAX	3.9	3.9	3.3	3.3	3.1	7.5
				4.2	4.2	3.3	3.3	3	7.5
t _{PHL}	B	A	MAX	4.6	4.6	4	4	3.7	7.5
				5.1	5.1	3.4	3.4	3.4	7.5
t _{PZH}	\overline{OE}	B	MAX	6.3	6.3	4.6	4.6	3.8	9
				6.4	6.4	4.6	4.6	3.4	9
t _{PHZ}	\overline{OE}	B	MAX	6.3	6.3	5.2	5.2	4.7	7.5
				5.2	5.2	5.1	5.1	4.8	7.5
t _{PZH}	\overline{OE}	A	MAX	7.1	7.1	5.3	5.3	4.7	9
				7	7	5.1	5.1	3.9	9
t _{PHZ}	\overline{OE}	A	MAX	6.6	6.6	5.6	5.6	5	7.5
				5.7	5.7	5.5	5.5	4.9	7.5

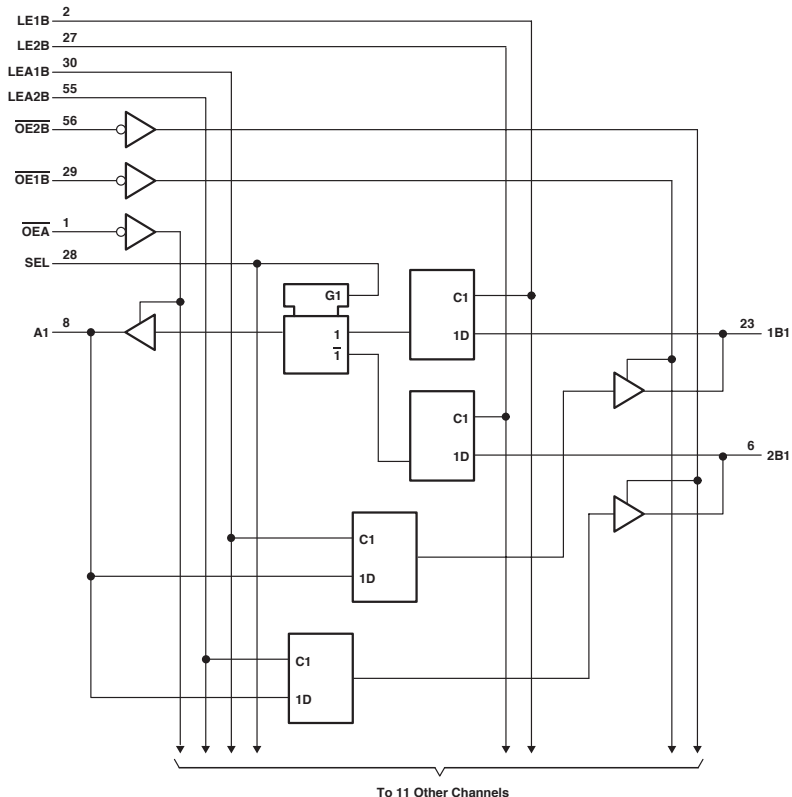
UNIT: ns

162260

12-BIT TO 24-BIT MULTIPLEXED D-TYPE LATCH WITH 3-STATE OUTPUTS

- SN74ABTH162260: B-Port Outputs Have Equivalent 25-Ω Series Resistors
- SN74ALVCH162260: B-Port Outputs Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
B TO A ($\overline{OE} = H$)

INPUTS						OUTPUT A
1B	2B	SEL	LE1B	LE2B	OEA	
H	X	H	H	X	L	H
L	X	H	H	X	L	L
X	X	H	L	X	L	A ₀
X	H	L	X	H	L	H
X	L	L	X	H	L	L
X	X	L	X	L	L	A ₀
X	X	X	X	X	H	Z

A TO B ($\overline{OE} = H$)

INPUTS					OUTPUTS	
A	LEA1B	LEA2B	OE1B	OE2B	1B	2B
H	H	H	L	L	H	H
L	H	H	L	L	L	L
H	H	L	L	L	H	2B ₀
L	H	L	L	L	L	2B ₀
H	L	H	L	L	1B ₀	H
X	L	L	L	L	1B ₀	L
X	L	L	L	L	1B ₀	2B ₀
X	X	X	H	H	Z	Z
X	X	X	L	H	Active	Z
X	X	X	H	L	Z	Active
X	X	X	L	L	Active	Active

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABTH	ALVCH 3V	UNIT
I _{cc}	MAX	63	0.04	mA
I _{OH} (A port)	MAX	-32	-24	mA
I _{OH} (B port)	MAX	-32	-12	mA
I _{OL} (A port)	MAX	64	24	mA
I _{OL} (B port)	MAX	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH	ALVCH 3V	
f _{max}				-	150	
t _w Pulse duration, LE1B, LE2B, LEA1B, or LEA2B high			MIN	3.3	3.3	
t _{su} Setup time, data before LE1B, LE2B, LEA1B, or LEA2B ,			MIN	1.5	1.1	
t _h Hold time, data after LE1B, LE2B, LEA1B, or LEA2B ,			MIN	1	1.5	
t _{PLH}	A	B	MAX	6.1	4.9	
				7.1	4.9	
t _{PHL}	B	A	MAX	6	4.3	
				6.2	4.3	
t _{PLH}	LE	A	MAX	6.3	4.4	
				5.8	4.4	
t _{PHL}	LE	B	MAX	6.1	5	
				7.1	5	
t _{PLH}	SEL (1B)	A	MAX	5.6	5.6	
	SEL (2B)			6.3	5.6	
t _{PHL}	SEL (1B)			MAX	5	5.6
	SEL (2B)				6.2	5.6
t _{PZH}	\overline{OE}	A	MAX	6.3	5.4	
				6.5	5.4	
t _{PZL}	\overline{OE}	B	MAX	6.3	6	
				8.2	6	
t _{PHZ}	\overline{OE}	A	MAX	6.7	4.6	
				5.2	4.6	
t _{PLZ}	\overline{OE}	B	MAX	7.5	5.1	
				6.2	5.1	

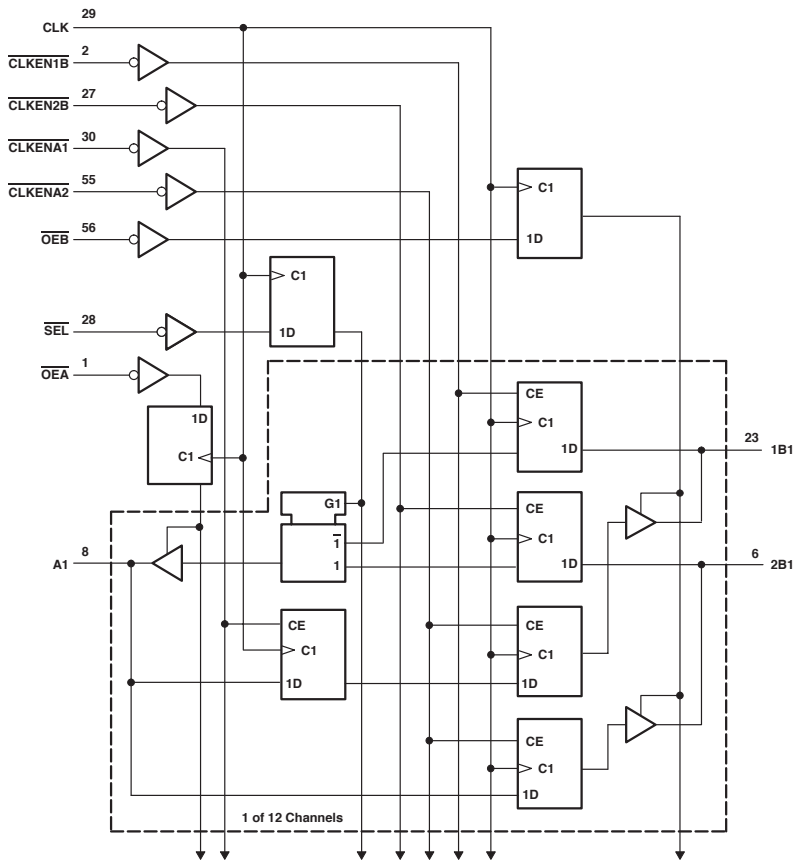
 UNIT f_{max} : MHz other : ns

162268

12-BIT TO 24-BIT REGISTERED BUS EXCHANGER WITH 3-STATE OUTPUTS

- SN74ALVCH162268: B-Port Outputs Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	OE \bar{A}	OE \bar{B}	A	1B, 2B
↑	H	H	Z	Z
↑	H	L	Z	Active
↑	L	H	Active	Z
↑	L	L	Active	Active

A-TO-B STORAGE ($\overline{OE\bar{B}} = L$)

INPUTS			OUTPUTS		
CLKENA1	CLKENA2	CLK	A	1B	2B
H	H	X	X	1B \dagger	2B \dagger
L	X	↑	L	L \dagger	X
L	X	↑	H	H \dagger	X
X	L	↑	L	X	L
X	L	↑	H	X	H

† Two CLK edges are needed to propagate data.

‡ Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE ($OE\bar{A} = L$)

INPUTS					OUTPUT	
CLKEN1B	CLKEN2B	CLK	SEL	1B	2B	A
H	X	X	H	X	X	A \dagger
X	H	X	L	X	X	A \dagger
L	X	↑	H	H	X	L
L	X	↑	H	L	X	H
X	L	↑	L	X	L	L
X	L	↑	L	X	H	H

† Output level before the indicated steady-state input conditions were established

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH} (A port)	MAX	-24	mA
I _{OH} (B port)	MAX	-12	mA
I _{OL} (A port)	MAX	24	mA
I _{OL} (B port)	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f _{max}			MIN	150
t _w	Pulse duration, CLK high or low		MIN	3.3
t _{su}	Setup time	A data before CLK ' 0	MIN	3.4
		B data before CLK ' 0	MIN	1
		SEL before CLK ' 0	MIN	1.3
		CLKENAT or CLKENA2 before CLK ' 0	MIN	2.8
		CLKENBT or CLKENB2 before CLK ' 0	MIN	2.5
		OE before CLK ' 0	MIN	3.2
t _h	Hold time	A data after CLK ' 0	MIN	0.2
		B data after CLK ' 0	MIN	1.3
		SEL after CLK ' 0	MIN	1
		CLKENAT or CLKENA2 after CLK ' 0	MIN	0.4
		CLKENBT or CLKENB2 after CLK ' 0	MIN	0.5
		OE after CLK ' 0	MIN	0.2
t _{pd}	CLK	B	MAX	5.4
		A (1B)		4.8
		A (2B)		4.8
		A (SEL)		5.8
t _{en}	CLK	B	MAX	6.1
		A		5.1
t _{fs}	CLK	B	MAX	5.9
		A		5

UNIT f_{max} : MHz other : ns

FUNCTION TABLE

A-TO-B STORAGE ($\overline{OE} = L$, DIR = H)

INPUTS			OUTPUTS	
SEL	CLK	A	1B	2B
H	X	X	1B \uparrow	2B \uparrow
L	X	L	L \uparrow	X
L	L	H	H \uparrow	X

\uparrow Output level before indicated steady-state input conditions were established

\ddagger Two CLK edges are needed to propagate the data.

B-TO-A STORAGE ($\overline{OE} = L$, DIR = L)

INPUTS				OUTPUT
CLK	SEL	1B	2B	A
\uparrow	H	X	L	L \S
\uparrow	H	X	H	H \S
\uparrow	L	L	X	L
\uparrow	L	H	X	H

\S Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

C-TO-D STORAGE ($\overline{OE} = L$)

INPUTS			OUTPUT	
SEL	CLK	C	1D	2D
H	X	X	1D \uparrow	2D \uparrow
L	\uparrow	L	L \uparrow	L
L	\uparrow	H	H \uparrow	H

\uparrow Output level before indicated steady-state input conditions were established

\ddagger Two CLK edges are needed to propagate the data.

OUTPUT ENABLE

INPUTS			OUTPUT		
CLK	\overline{OE}	DIR	A	1B, 2B	1D, 2D
\uparrow	H	X	Z	Z	Z
\uparrow	L	H	Z	Active	Active
\uparrow	L	L	Active	Z	Active

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCHG 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH} (A to B)	MAX	8	mA
I _{OH} (B to A)	MAX	6	mA
I _{OL} (A to B)	MAX	8	mA
I _{OL} (B to A)	MAX	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCHG 3V
t _{max}			MIN	160
t _w	Pulse duration, CLK high or low		MIN	2.3
t _{su}	Setup time	A data before CLK, high or low	MIN	1.4
		B data before CLK, high or low	MIN	2
		C data before CLK, high or low	MIN	1.3
		DIR before CLK, high or low	MIN	2
		SEL before CLK, high or low	MIN	2
t _h	Hold time	A data after CLK, high or low	MIN	0.3
		B data after CLK, high or low	MIN	0.3
		C data after CLK, high or low	MIN	0.3
		DIR after CLK, high or low	MIN	0.3
		SEL after CLK, high or low	MIN	0.3
t _{pd}	Propagation delay	CLK	A	5
			B	7.4
			D	7.2
t _{en}	Enable time	CLK	A	6.2
			B	9.4
		\overline{OE}	A	6
			B	9.5
			D	7.9
t _{dis}	Disable time	CLK	A	6.4
			B	7.8
		\overline{OE}	A	5
			B	7.6
			D	6.7

UNIT f_{max} : MHz other : ns

FUNCTION TABLE
**A-TO-B STORAGE
(OE = L, DIR = H)**

INPUTS			OUTPUTS	
SEL	CLK	A	1B	2B
H	X	X	1B ₀ †	2B ₀ †
L	↑	L	L‡	L
L	↑	H	H‡	H

† Output level before indicated steady-state input conditions were established

‡ Two CLK edges are needed to propagate the data.

**B-TO-A STORAGE
(OE = L, DIR = L)**

INPUTS				OUTPUT
CLK	SEL	1B	2B	A
↑	H	X	L	L‡
↑	H	X	H	H‡
↑	L	L	X	L
↑	L	H	X	H

§ Two CLK edges are needed to propagate the data. The data is loaded in the first register when SEL is low and propagates to the second register when SEL is high.

OUTPUT ENABLE

INPUTS			OUTPUTS	
CLK	OE	DIR	A	1B, 2B
↑	H	X	Z	Z
↑	L	H	Z	Active
↑	L	L	Active	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCHG 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH} (A to B)	MAX	8	mA
I _{OH} (B to A)	MAX	8	mA
I _{OL} (A to B)	MAX	8	mA
I _{OL} (B to A)	MAX	6	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCHG 3V
f _{max}			MIN	160
t _w Pulse duration, CLK high or low			MIN	2.3
t _{su} Setup time		A data before CLK	MIN	1.5
		B data before CLK	MIN	2
		DIR before CLK	MIN	2
		SEL before CLK	MIN	2
t _h Hold time		A data after CLK	MIN	0.3
		B data after CLK	MIN	0.3
		DIR after CLK	MIN	0.3
		SEL after CLK	MIN	0.3
t _{pd}	CLK	A	MAX	5
		B		7.4
t _{en}	CLK	A	MAX	6.3
		B		9.4
	OE	A	MAX	6
		B		9.5
t _{dis}	CLK	A	MAX	6.4
		B		7.8
	OE	A	MAX	5
		B		7.6

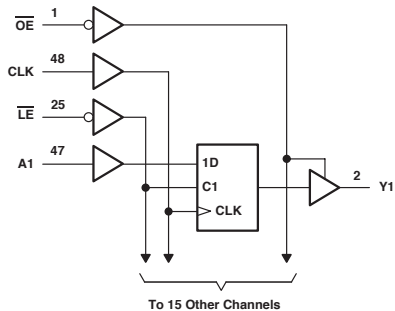
UNIT f_{max} : MHz other : ns

162334

16-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162334: Output Ports Have Equivalent 26- Ω Series Resistors
- SN74ALVCH162334: Output Port Has Equivalent 26- Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE	LE	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y ₀ †

† Output level before the indicated steady-state input conditions were established

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	0.04	mA
I _{OH}	MAX	-12	-12	mA
I _{OL}	MAX	12	12	mA

SWITCHING CHARACTERISTICS

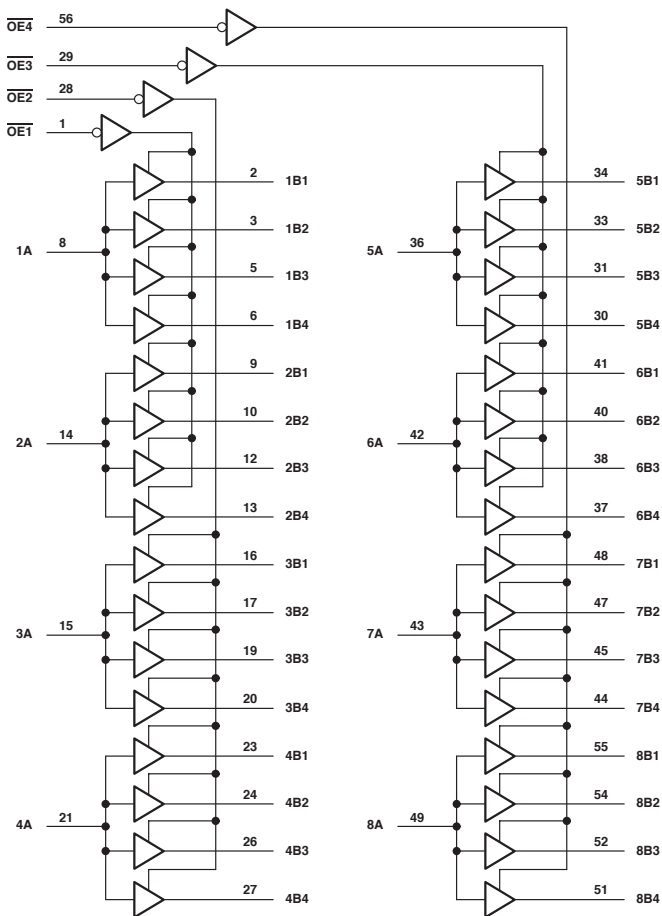
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V
t _{max}			MIN	150	150
t _w Pulse duration	LE low			3.3	3.3
	CLK high or low		MIN	3.3	3.3
t _{su} Setup time	Data before CLK *		MIN	1.5	1.5
	Data before LE * CLK high		MIN	1.3	1.3
	Data before LE * CLK low		MIN	1.2	1.2
t _h Hold time	Data after CLK *		MIN	0.9	0.9
	Data after LE * CLK high		MIN	1.1	1.1
	Data after LE * CLK low		MIN	1.1	1.1
t _{pd}	A	Y	MAX	3.9	3.9
	LE		5	5	
	CLK		MAX	4.9	4.9
t _{en}	OE	Y		5.4	5.4
t _{dis}	OE	Y	MAX	5	5

UNIT f_{max} : MHz other : ns

1-BIT TO 4-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVCH162344: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS		OUTPUT
OE	A	Bn
L	H	H
L	L	L
H	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH}	MAX	-12	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
t _{PLH}	A	B	MAX	4.4
t _{PHL}				4.4
t _{PZH}	OE	B	MAX	5.7
t _{PZL}				5.7
t _{PHZ}	OE	B	MAX	4.5
t _{PLZ}				4.5

UNIT: ns

162373

3.3-V ABT 16-BIT TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

- SN74LVTH162373: Output Ports Have Equivalent 22-Ω Series Resistors

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

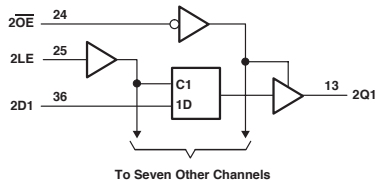
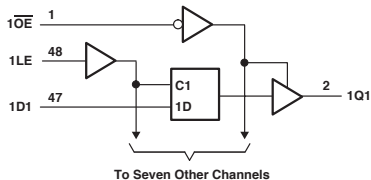
PARAMETER	MAX or MIN	LVTH 3V	UNIT
I _{CC}	MAX	5	mA
I _{OH}	MAX	-12	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V
t _w Pulse duration, LE high or low			MIN	3
t _{su} Setup time	Data before LE , , data high		MIN	1
	Data before LE , , data low		MIN	1
t _h Hold time	Data after LE , , data high		MIN	1
	Data after LE , , data low		MIN	1
t _{PLH}	D	Q	MAX	4.6
t _{PHL}				4
t _{PLH}	LE	Q	MAX	5.1
t _{PHL}				4.6
t _{PZH}	OE	Q	MAX	5.4
t _{PZL}				4.9
t _{PHZ}	OE	Q	MAX	5.4
t _{PLZ}				5.1

UNIT: ns

Logic Diagram



162374

3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

- SN74LVTH162374: Output Ports Have Equivalent 22- Ω Series Resistors
- SN74ALVCH162374: Output Ports Have Equivalent 26- Ω Series Resistors

FUNCTION TABLE
(each flip-flop)

INPUTS			OUTPUT
OE	CLK	D	Q
L	\uparrow	H	H
L	\uparrow	L	L
L	L	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

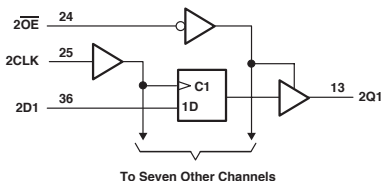
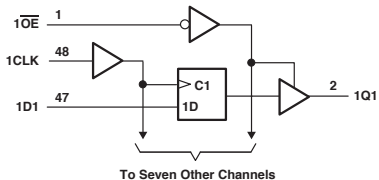
PARAMETER	MAX or MIN	LVTH 3V	ALVCH 3V	UNIT
I _{CC}	MAX	5	0.04	mA
I _{DH}	MAX	-12	-12	mA
I _{OL}	MAX	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V	ALVCH 3V
f _{max}				160	150
t _w Pulse duration, CLK high or low			MIN	3	3.3
t _{su} Setup time		Data before CLK \uparrow , data high	MIN	1.8	1.9
		Data before CLK \uparrow , data low	MIN	1.8	1.9
t _h Hold time		Data after CLK \downarrow , data high	MIN	0.8	0.5
		Data after CLK \downarrow , data low	MIN	0.8	0.5
t _{PLH}	CLK	Q	MAX	5.3	4.6
t _{PHL}				4.9	4.6
t _{PZH}	OE	Q	MAX	5.6	5.2
t _{PZL}				4.9	5.2
t _{PHZ}	OE	Q	MAX	5.4	4.5
t _{PLZ}				5	4.5

UNIT f_{max} : MHz other : ns

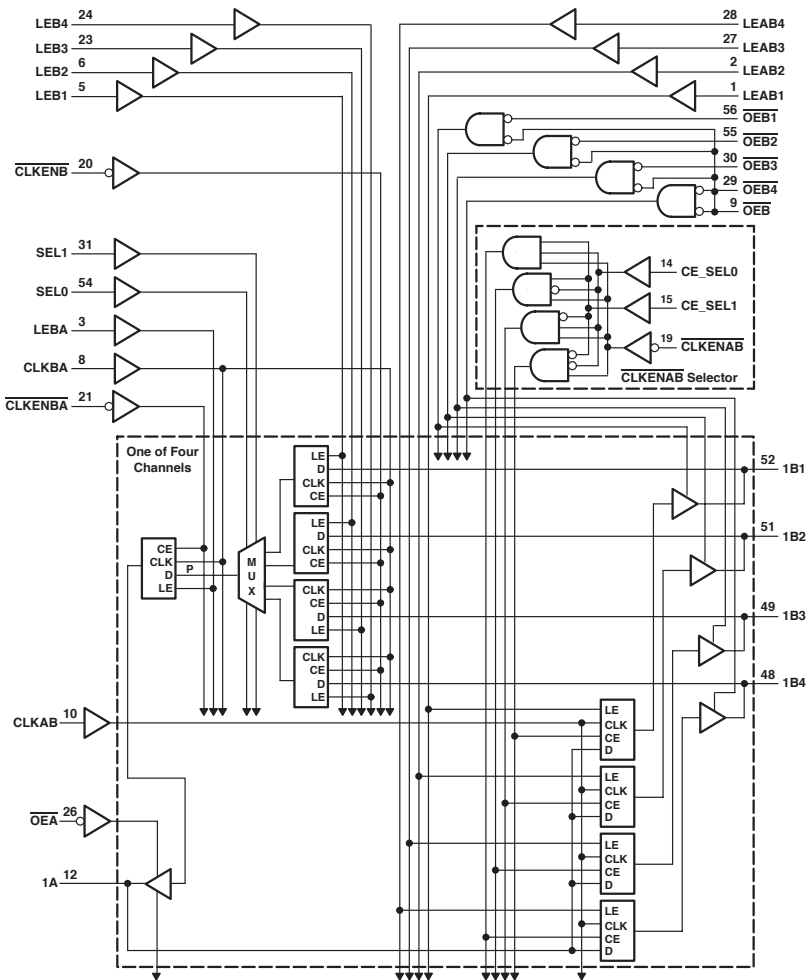
Logic Diagram



4-TO-1 MULTIPLEXED/DEMULTIPLEXED REGISTERED TRANSCIEVERS WITH 3-STATE OUTPUTS

- SN74ABTH162460: B-Port Outputs Have Equivalent 25-Ω Series Resistors

Logic Diagram



FUNCTION TABLE
A-TO-B OUTPUT ENABLE

INPUTS		OUTPUT
OEB	OEBn	Bn
H	H	Z
H	L	Z
L	H	Z
L	L	Active

†n = 1, 2, 3, 4

A-TO-B STORAGE
 (assuming OEB = L, OEBn = L)

INPUTS								OUTPUTS					
CLKENAB	CE	SEL1	CE	SEL0	CLKAB	LEAB1	LEAB2	LEAB3	LEAB4	B1	B2	B3	B4
X	X	X	X	X	H or L	H	L	L	L	A	A ₀	A ₀	A ₀
X	X	X	X	X	H or L	H	L	L	L	A	A	A	A ₀
L	X	X	X	L	L	L	L	L	L	A ₀	A ₀	A ₀	A ₀
L	L	L	L	H	†	L	L	L	L	A	A ₀	A ₀	A ₀
L	L	L	H	†	L	L	L	L	L	A ₀	A	A ₀	A ₀
L	H	L	†	L	L	L	L	L	L	A ₀	A ₀	A	A ₀
L	H	H	†	L	L	L	L	L	L	A ₀	A ₀	A ₀	A ₀
H	X	X	X	†	L	L	L	L	L	A ₀	A ₀	A ₀	A ₀

B-TO-A STORAGE

(after point P)

INPUTS								P
CLKENB	CLKBA	LEB1	LEB2	LEB3	LEB4	SEL1	SEL0	
X	X	H	L	L	L	L	L	B1
X	X	L	H	L	L	L	H	B2
X	X	L	L	H	L	H	L	B3
X	X	L	L	L	H	H	H	B4
L	†	L	L	L	L	L	L	B1
						L	H	B2
						H	L	B3
						H	H	B4
L	L	L	L	L	L	L	L	B1†
						L	H	B2†
						H	L	B3†
						H	H	B4†

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE

(after point P)

INPUTS							OUTPUT
CLKENBA	CLKBA	LEBA	OEA	B			A
X	X	X	H	X			X
X	X	H	L	L			L
X	X	H	L	H			H
H	X	L	L	X			A ₀ †
L	†	L	L	L			L
L	†	L	L	H			H
L	L	L	L	X			A ₀ †

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABTH	UNIT
I _{CC}	MAX	32	mA
I _{OH} (A port)	MAX	-32	mA
I _{OH} (B port)	MAX	-12	mA
I _{OL} (A port)	MAX	64	mA
I _{OL} (B port)	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER		MAX or MIN	ABTH	
f _{max}		MIN	160	
t _w Pulse duration	CLKAB high or low	MIN	3.8	
	CLKBA high or low	MIN	4.5	
	LEAB1, 2, 3 or 4 high	MIN	2.8	
	LEBA high	MIN	2.8	
	LEB1, 2, 3 or 4 high	MIN	3	
t _{su} Setup time	Before CLKAB	A bus	MIN	2.5
		CE_SEL0/1	MIN	3.2
		CLKENAB	MIN	3.2
	Before LEAB1, 2, 3, or 4, A bus	B bus	MIN	3.8
		CLKENB	MIN	2.3
		CLKENBA	MIN	2.5
	Before CLKBA	LEB1, 2, 3 or 4	MIN	4.3
		SEL0/1	MIN	4.5
		Before LEB1, 2, 3, or 4, B bus	MIN	3.2
	Before CLKBA	B bus	MIN	4
		LEB1, 2, 3 or 4	MIN	4.4
		SEL0/1	MIN	4.3
t _h Hold time	after CLKAB	A bus	MIN	0.5
		CE_SEL0/1	MIN	1.1
		CLKENAB	MIN	0.5
	after LEAB1, 2, 3, or 4, A bus	B bus	MIN	1.2
		B bus	MIN	1.3
		CLKENB	MIN	1
	after CLKBA	CLKENBA	MIN	1
		SEL0/1	MIN	0
		Before LEB1, 2, 3, or 4, B bus	MIN	1.5
	after CLKBA	B bus	MIN	0.4
		SEL0/1	MIN	0.1

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABTH
IP _{LH}				6.5
IP _{HL}	B	A	MAX	6.5
IP _{ZH}	0EA	A	MAX	5.6
IP _{ZL}				5.5
IP _{HZ}	0EA	A	MAX	5.9
IP _{LZ}				6.5
IP _{LH}	A	B	MAX	6.2
IP _{HL}				6.5
IP _{ZH}	0EB	B	MAX	6.8
IP _{ZL}				6.3
IP _{HZ}	0EB	B	MAX	6.2
IP _{LZ}				5.8
IP _{ZH}	0EB1, 2, 3, 4	B	MAX	6.6
IP _{ZL}				6.2
IP _{HZ}	0EB1, 2, 3, 4	B	MAX	5.3
IP _{LZ}				4.9
IP _{LH}	CLKBA	A	MAX	7.4
IP _{HL}				7.7
IP _{LH}	CLKAB	B	MAX	6.5
IP _{HL}				6.5
IP _{LH}	LEBA	A	MAX	5.8
IP _{HL}				5.8
IP _{LH}	LEAB1, 2, 3, 4	B	MAX	6.2
IP _{HL}				6.2
IP _{LH}	LEBA1, 2, 3, 4	A	MAX	7.2
IP _{HL}				6.8
IP _{LH}	SEL	A	MAX	7.5
IP _{HL}				6.9

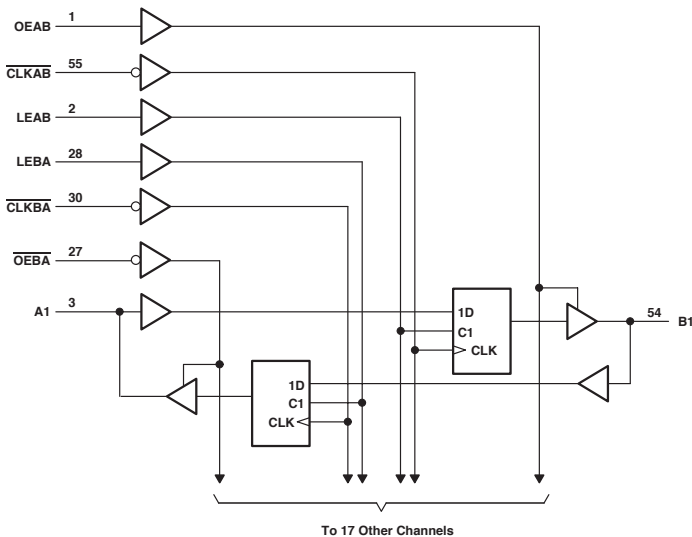
UNIT: ns

162500

18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

- SN74ABT162500: B-Port Outputs Have Equivalent 25-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OEAB	LEAB	CLKAB	A	B
L	X	X	X	Z
H	H	X	L	L
H	H	X	H	H
H	L	↓	L	L
H	L	↓	H	H
H	L	H	X	B ₀ †
H	L	L	X	B ₀ ‡

† Output level before the indicated steady-state input conditions were established.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I _{CC}	MAX	36	mA
I _{OH} (A port)	MAX	-32	mA
I _{OH} (B port)	MAX	-12	mA
I _{OL} (A port)	MAX	64	mA
I _{OL} (B port)	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
f _{max}			MIN	150
t _w Pulse duration	LEAB or LEBA high		MIN	2.5
	CLKAB or CLKBA high or low		MIN	3
t _{su} Setup time	A before CLKAB ,		MIN	3.3
	B before CLKBA ,		MIN	3.3
	A before LEAB , or LEBA , CLK high		MIN	1
	A before LEAB , or LEBA , CLK low		MIN	2.5
t _h Hold time	A after CLKAB , or B after CLKBA ,		MIN	0
	A after LEAB , or B after LEBA ,		MIN	2
t _{PLH}	A or B	B or A	MAX	4.8
t _{PHL}				5.7
t _{PZH}	LEAB or LEBA	B or A	MAX	5.6
t _{PZL}				5.9
t _{PHZ}	CLKAB or CLKBA	B or A	MAX	5.9
t _{PLZ}				6
t _{PZH}	OEAB	B	MAX	5.3
t _{PZL}				5.4
t _{PHZ}	OEAB	B	MAX	6.5
t _{PLZ}				5.8
t _{PZH}	OEBA	A	MAX	5.3
t _{PZL}				5.4
t _{PHZ}	OEBA	A	MAX	6.5
t _{PLZ}				5.8

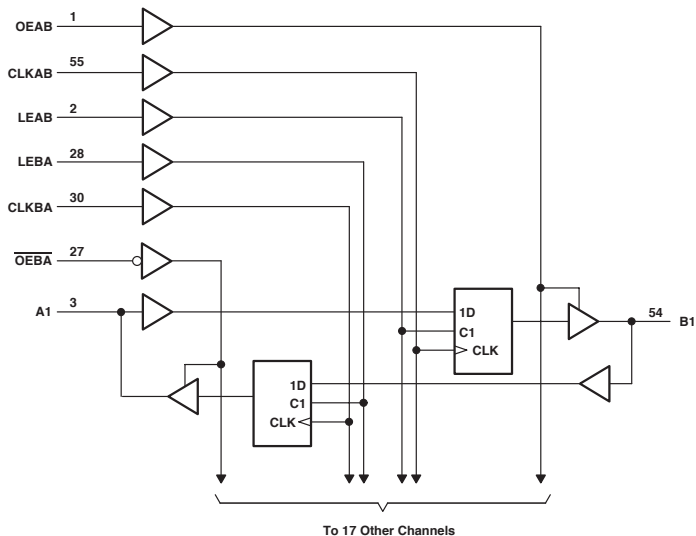
UNIT f_{max} : MHz other : ns

162501

18-BIT UNIVERSAL BUS TRANSCEIVERS WITH 3-STATE OUTPUTS

- SN74ABT162501: B-Port Outputs Have Equivalent 25- Ω Series Resistors

Logic Diagram



FUNCTION TABLE†

INPUTS					OUTPUT
OEAB	LEAB	CLKAB	A	Y	
L	X	X	X	Z	
H	H	X	L	L	
H	H	X	H	H	
H	L	†	L	L	
H	L	†	H	H	
H	L	H	X	B ₀ ‡	
H	L	L	X	B ₀ §	

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, and CLKBA.

‡ Output level before the indicated steady-state input conditions were established, provided that CLKAB was high before LEAB went low.

§ Output level before the indicated steady-state input conditions were established.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I _{CC}	MAX	36	mA
I _{OH} (A port)	MAX	-32	mA
I _{OH} (B port)	MAX	-12	mA
I _{OL} (A port)	MAX	64	mA
I _{OL} (B port)	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
f _{max}			MIN	150
t _w Pulse duration	LEAB or LEBA high		MIN	3
	CLKAB or CLKBA high or low		MIN	3.3
t _{su} Setup time	A before CLKAB *		MIN	4.3
	B before CLKBA *		MIN	4.3
	A before LEAB , or LEBA , CLK high		MIN	2.5
	A before LEAB , or LEBA , CLK low		MIN	1
t _h Hold time	A after CLKAB * or B after CLKBA *		MIN	0
	A after LEAB , or B after LEBA ,		MIN	2
t _{PLH}	A or B	B or A	MAX	4.8
t _{PHL}				5.7
t _{PZH}	LEAB or LEBA	B or A	MAX	5.6
t _{PZL}				5.9
t _{PHZ}	CLKAB or CLKBA	B or A	MAX	5.5
t _{PLZ}				5.3
t _{PZH}	OEAB	B	MAX	5.3
t _{PZL}				5.4
t _{PHZ}	OEAB	B	MAX	6.5
t _{PLZ}				5.8
t _{PZH}	OEBA	A	MAX	5.3
t _{PZL}				5.4
t _{PHZ}	OEBA	A	MAX	6.5
t _{PLZ}				5.8

UNIT f_{max} : MHz other : ns

FUNCTION TABLE
A-TO-B STORAGE(OEAB=L)

INPUTS			OUTPUT
CLKNAB	OLKAB	A	B
H	X	X	Bo†
L	†	L	L
L	†	H	H

† Output level before the indicated steady-state input conditions were established

B-TO-A STORAGE (OEBA = L)

INPUTS					OUTPUT
CLKENBA	CLK2BA	CLK1BA	SEL	B	A
H	X	X	X	X	Ag†
L	†	X	H	L	L
L	†	X	H	H	H
L	†	†	L	L	L‡
L	†	†	L	H	H‡

† Output level before the indicated steady-state input conditions were established

‡ Three CLK1BA edges and one CLK2BA edge are needed to propagate data from B to A when SEL is low.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
Icc	MAX	0.04	mA
Ioh(A port)	MAX	-24	mA
Ioh(B port)	MAX	-12	mA
Iol(A port)	MAX	24	mA
Iol(B port)	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
fmax			MIN	150
tw	Pulse duration, CLK high or low		MIN	3
tsu	Setup time	A data before CLKAB *	MIN	1.3
		B data before CLK2BA *	MIN	1.7
		B data before CLK1BA *	MIN	1.1
		SEL before CLK2BA *	MIN	3.3
		CLKENAB before CLKAB *	MIN	1.6
		CLKENBA before CLK1BA *	MIN	2.1
		CLKENBA before CLK2BA *	MIN	2.2
th	Hold time	A data after CLKAB *	MIN	0.9
		B data after CLK2BA *	MIN	0.6
		B data after CLK1BA *	MIN	1
		SEL after CLK2BA *	MIN	0.1
		CLKENAB after CLKAB *	MIN	0.3
		CLKENBA after CLK1BA *	MIN	0.1
		CLKENBA after CLK2BA *	MIN	0
tpd	CLKAB	B	MAX	4.7
	CLK2BA	A		4.2
ten	OEBA	A	MAX	5.1
	OEAB	B		5.7
tdis	OEBA	A	MAX	4.9
	OEAB	B		4.9

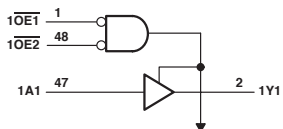
UNIT fmax : MHz other : ns

162541

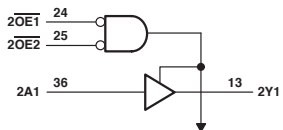
3.3-V ABT 16-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74LVTH162541: Output Ports Have Equivalent 22-Ω Series Resistors

Logic Diagram



To Seven Other Channels



To Seven Other Channels

FUNCTION TABLE
(each 8-bit section)

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	UNIT
I _{CC}	MAX	5	mA
I _{OH}	MAX	-12	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V
t _{PLH}	A	Y	MAX	4.1
t _{PHL}				4.1
t _{PZH}	\overline{OE}	Y	MAX	5
t _{PZL}				4.8
t _{PHZ}	\overline{OE}	Y	MAX	5.9
t _{PLZ}				5.4

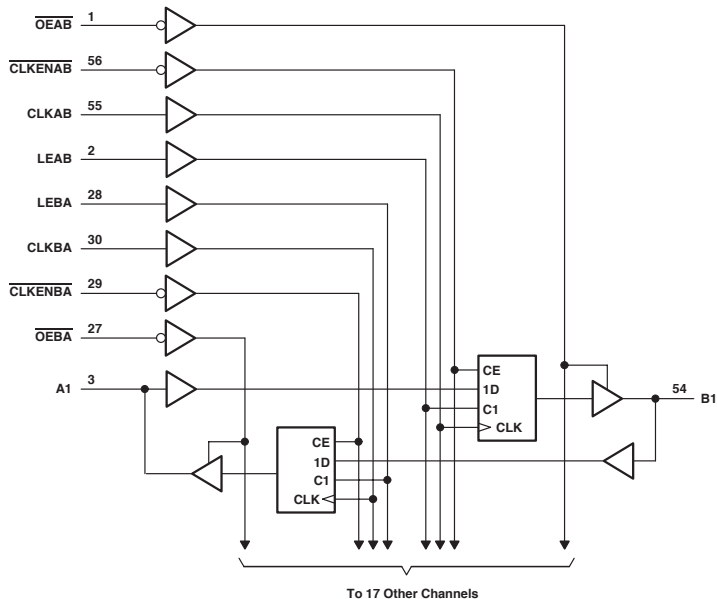
UNIT: ns

162601

18-BIT UNIVERSAL BUS TRANSCEIVER WITH 3-STATE OUTPUTS

- SN74ABT162601: B-Port Outputs Have Equivalent 25- Ω Series Resistors
- SN74ALVCH162601: B-Port Outputs Have Equivalent 26- Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT
CLKENAB	OEAB	LEAB	CLKAB	\bar{A}	B
X	H	X	X	X	Z
X	L	H	X	L	L
X	L	H	X	H	H
H	L	L	X	X	B ₀ ‡
H	L	L	X	X	B ₀ ‡
L	L	L	†	L	L
L	L	L	†	H	H
L	L	L	L	X	B ₀ ‡
L	L	L	H	X	B ₀ §

† A-to-B data flow is shown; B-to-A flow is similar but uses OEBA, LEBA, CLKBA, and CLKENBA.

‡ Output level before the indicated steady-state input conditions were established.

§ Output level before the indicated steady-state input conditions were established, provided that CLKAB was low before LEAB went low.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVCH 3V	UNIT
I _{CC}	MAX	36	0.04	mA
I _{OH} (A port)	MAX	-32	-24	mA
I _{OH} (B port)	MAX	-12	-12	mA
I _{OL} (A port)	MAX	64	24	mA
I _{OL} (B port)	MAX	12	12	mA

SWITCHING CHARACTERISTICS

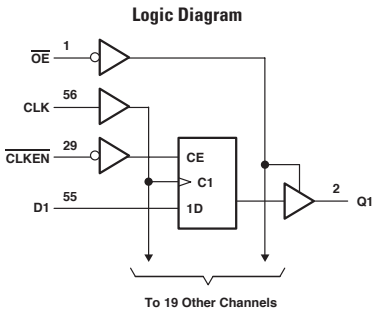
PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVCH 3V
t _{max}			MIN	150	150
t _w Pulse duration	LEAB or LEBA high		MIN	2.5	3.3
	CLKAB or CLKBA high or low		MIN	3	3.3
t _{su} Setup time	Data before CLK *		MIN	4.3	2.1
	A before LEAB , or B before LEBA , , CLK high		MIN	2.5	1.6
	A before LEAB , or B before LEBA , , CLK low		MIN	1	1.1
	CLKEN before *		MIN	2.7	1.7
t _h Hold time	Data after CLK *		MIN	0	0.8
	A after LEAB , or B after LEBA , , CLK high		MIN	0.5	1.4
	A after LEAB , or B after LEBA , , CLK low		MIN	0.5	1.7
	CLKEN after *		MIN	0	0.6
t _{PLH}	A	B	MAX	4.8	4.5
t _{PHL}				5.7	4.5
t _{PLH}	B	A	MAX	4	4.1
t _{PHL}				4.9	4.1
t _{PLH}	LEBA	A	MAX	5	4.7
t _{PHL}				5	4.7
t _{PLH}	LEAB	B	MAX	5.6	5.1
t _{PHL}				5.9	5.1
t _{PLH}	CLKBA	A	MAX	5.3	5
t _{PHL}				5	5
t _{PLH}	CLKAB	B	MAX	5.5	5.5
t _{PHL}				5.3	5.5
t _{PZH}	\overline{OEBA}	A	MAX	5.1	5.2
t _{PZL}				5.4	5.2
t _{PZH}	\overline{OEAB}	B	MAX	6.1	5.7
t _{PZL}				5.7	5.7
t _{PHZ}	\overline{OEBA}	A	MAX	6.2	4.4
t _{PLZ}				5.4	4.4
t _{PHZ}	\overline{OEAB}	B	MAX	5.4	4.8
t _{PLZ}				5.2	4.8

UNIT f_{max}: MHz other: ns

162721

3.3-V 20-BIT FLIP-FLOP WITH 3-STATE OUTPUTS

- SN74ALVCH162721: Output Ports Have Equivalent 26-Ω Series Resistors



FUNCTION TABLE
(each flip-flop)

INPUTS				OUTPUT Q
OE	CLKEN	CLK	D	
L	H	X	X	Q ₀
L	L	↑	H	H
L	L	↑	L	L
L	L	L or H	X	Q ₀
H	X	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH}	MAX	-12	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

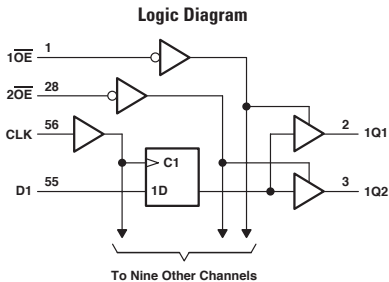
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f _{max}			MIN	150
t _w Pulse duration	CLK high or low		MIN	3.3
t _{su} Setup time	Data before CLK *		MIN	3.1
	CLKEN before CLK *		MIN	2.7
t _h Hold time	Data after CLK *		MIN	0
	CLKEN after CLK *		MIN	0
t _{PLH}	CLK	Q	MAX	5.3
t _{PHL}				5.3
t _{PZH}	OE	Q	MAX	5.8
t _{PZL}				5.8
t _{PHZ}	OE	Q	MAX	5
t _{PLZ}				5

UNIT f_{max} : MHz other : ns

162820

3.3-V 10-BIT FLIP-FLOP WITH DUAL OUTPUTS AND 3-STATE OUTPUTS

- SN74ALVCH162820: Output Ports Have Equivalent 26-Ω Series Resistors



FUNCTION TABLE
(each flip flop)

INPUT			OUTPUT
OE _n	CLK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q ₀
H	X	X	Z

t_n = 1,2

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH}	MAX	-12	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

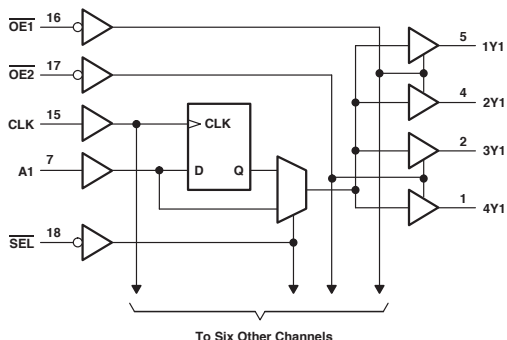
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f _{max}			MIN	150
t _w Pulse duration	CLK high or low			3.3
t _{su} Setup time	Data before CLK *		MIN	1.4
t _h Hold time	Data after CLK *		MIN	1
t _{PLH}	CLK	Q	MAX	5.4
t _{PHL}				5.4
t _{PZH}	OE	Q	MAX	5.6
t _{PZL}				5.6
t _{PHZ}	OE	Q	MAX	5
t _{PLZ}				5

UNIT f_{max} : MHz other : ns

18-BIT BUS-INTERFACE FLIP-FLOPS WITH 3-STATE OUTPUTS

- SN74ABT162823A: Output Ports Have Equivalent 25-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS					OUTPUT Q
OE	CLR	CLENK	CLK	D	
L	L	X	X	X	L
L	H	L	↑	H	H
L	H	L	↑	L	L
L	H	L	L	X	Q ₀
L	H	H	X	X	Q ₀
H	X	X	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I _{CC}	MAX	80	mA
I _{OH}	MAX	-12	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
f _{max}			MIN	150
t _w Pulse duration	CLR low		MIN	3.3
	CLK high or low		MIN	3.3
t _{su} Setup time	CLR inactive		MIN	1.6
	Data before CLK '↑'		MIN	2
	CLENK' low before CLK '↑'		MIN	2.8
t _h Hold time	Data after CLK '↑'		MIN	1.2
	CLENK low after CLK '↑'		MIN	0.6
TP _{LH}	CLK	Q	MAX	7.5
TP _{LH}			6.7	
TP _{LH}	CLR	Q	MAX	7
TP _{ZH}	OE	Q	MAX	5.9
TP _{ZL}			7	
TP _{HZ}	OE	Q	MAX	6.6
TP _{LZ}			9	

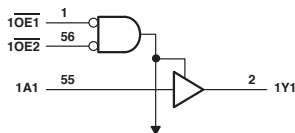
UNIT f_{max}: MHz other: ns

162825

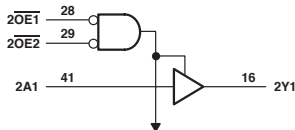
18-BIT BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74ABT162825: Output Ports Have Equivalent 25-Ω Series Resistors

Logic Diagram



To Eight Other Channels



To Eight Other Channels

FUNCTION TABLE

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	UNIT
I _{CC}	MAX	32	mA
I _{OH}	MAX	-12	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT
t _{PLH}	A	Y	MAX	3.9
t _{PHL}				4.7
t _{PZH}	OE	Y	MAX	6.9
t _{PZL}				6.3
t _{PHZ}	OE	Y	MAX	6.6
t _{PLZ}				6.3

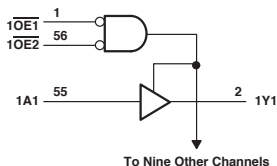
UNIT: ns

162827

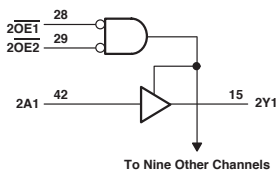
20-BIT BUS BUFFERS/DRIVERS WITH 3-STATE OUTPUTS

- SN74ABT162827A: Output Ports Have Equivalent 25-Ω Series Resistors
- SN74ALVTH162827: Output Ports Have Equivalent 30-Ω Series Resistors
- SN74ALVCH162827: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



To Nine Other Channels



To Nine Other Channels

FUNCTION TABLE (each flip flop)

INPUTS			OUTPUT
OE1	OE2	A	Y
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

Tn = 1,2

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V	UNIT
I _{CC}	MAX	32	5.5	0.04	mA
I _{OH}	MAX	-12	-12	-12	mA
I _{OL}	MAX	12	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVTH 3V	ALVCH 3V
t _{PLH}	A	Y	MAX	3.9	3.9	3.8
				4.7	3.7	3.8
t _{PZH}	OE	Y	MAX	6.9	5.6	5.1
				6.3	4.1	5.1
t _{PHZ}	OE	Y	MAX	6.6	6.3	4.7
				6.3	5.1	4.7

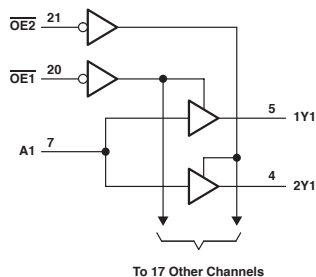
UNIT: ns

162830

1-BIT TO 2-BIT ADDRESS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVCH162830, SN74ALVCHS162830: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS			OUTPUTS	
OE1	OE2	A	1Yn	2Yn
L	H	H	H	Z
L	H	L	L	Z
H	L	H	Z	H
H	L	L	Z	L
L	L	H	H	H
L	L	L	L	L
H	H	X	Z	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	ALVCHS 3V	UNIT
I _{CC}	MAX	0.04	0.04	mA
I _{DH}	MAX	-12	-12	mA
I _{OL}	MAX	12	12	mA

SWITCHING CHARACTERISTICS

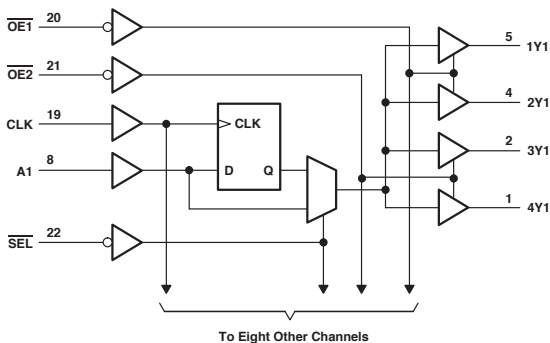
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V	ALVCHS 3V
t _{PLH}	A	Y	MAX	3.5	3.5
t _{PHL}				3.5	3.5
t _{PZH}	OE	Y	MAX	4.8	4.8
t _{PZL}				4.8	4.8
t _{PHZ}	OE	Y	MAX	5.2	5.2
t _{PLZ}				5.2	5.2

UNIT: ns

1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162831, SN74ALVCH162831: Output Ports Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE	SEL	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	UNIT
I_{CC}	MAX	0.04	0.04	mA
I_{OH}	MAX	-12	-12	mA
I_{OL}	MAX	12	12	mA

SWITCHING CHARACTERISTICS

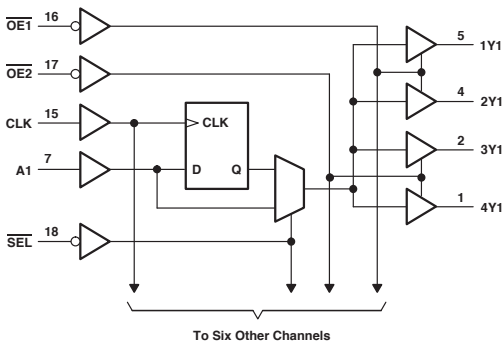
PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V
f_{max}			MIN	150	150
t_{w} Pulse duration	CLK high or low		MIN	3.3	3.3
t_{su} Setup time	A data before CLK *		MIN	1.6	1.6
t_h Hold time	A data after CLK *		MIN	1.1	1.1
t_{PLH}	A	Y	MAX	4.3	4.3
t_{PHL}	A	Y	MAX	4.3	4.3
t_{PLH}	CLK	Y	MAX	4.7	4.7
t_{PHL}	CLK	Y	MAX	4.7	4.7
t_{PLH}	SEL	Y	MAX	4.8	4.8
t_{PHL}	SEL	Y	MAX	4.8	4.8
t_{PZH}	OE	Y	MAX	5.1	5.1
t_{PZL}	OE	Y	MAX	5.1	5.1
t_{PHZ}	OE	Y	MAX	5.1	5.1
t_{PLZ}	OE	Y	MAX	5.1	5.1

UNIT f_{max} : MHz other: ns

1-BIT TO 4-BIT ADDRESS REGISTER/DRIVER WITH 3-STATE OUTPUTS

- SN74ALVCH162832: Output Ports Have Equivalent 26- Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE	SEL	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH}	MAX	-12	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVCH 3V
f _{max}			MIN	150
t _w Pulse duration	CLK high or low		MIN	3.3
t _{su} Setup time	A data before CLK *		MIN	1.6
t _h Hold time	A data after CLK *		MIN	1.1
DP _{LH}	A	Y	MAX	4.3
DP _{HL}	A	Y	MAX	4.3
DP _{LH}	CLK	Y	MAX	4.7
DP _{HL}	CLK	Y	MAX	4.7
DP _{LH}	SEL	Y	MAX	4.8
DP _{HL}	SEL	Y	MAX	4.8
DP _{ZH}	OE	Y	MAX	5.1
DP _{ZL}	OE	Y	MAX	5.1
DP _{HZ}	OE	Y	MAX	5.1
DP _{LZ}	OE	Y	MAX	5.1

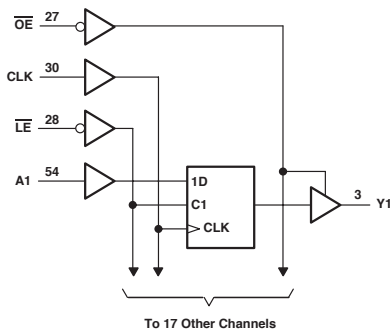
UNIT f_{max} : MHz other : ns

162834

18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162834: Outputs Have Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE	LE	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	H	X	Y ₀ †
L	H	L	X	Y ₀ ‡

† Output level before the indicated steady-state input conditions were established, provided that CLK is high before LE goes high
 ‡ Output level before the indicated steady-state input conditions were established

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	UNIT
I _{CC}	MAX	0.04	mA
I _{OH}	MAX	-12	mA
I _{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V
f _{max}			MIN	150
t _w Pulse duration	LE low		MIN	3.3
	CLK high or low		MIN	3.3
t _{su} Setup time	Data before CLK *		MIN	1.7
	Data before LE *, CLK high		MIN	1.9
	Data before LE *, CLK low		MIN	1.5
t _h Hold time	A data after CLK *		MIN	0.7
	Data after LE *, CLK high		MIN	0.9
	Data after LE *, CLK low		MIN	0.9
t _{PLH}	A	Y	MAX	4.2
t _{PHL}				4.2
t _{PLH}	LE	Y	MAX	5.8
t _{PHL}				5.8
t _{PLH}	CLK	Y	MAX	5.4
t _{PHL}				5.4
t _{PZH}	OE	Y	MAX	5.9
t _{PZL}				5.9
t _{PHZ}	OE	Y	MAX	5
t _{PLZ}				5

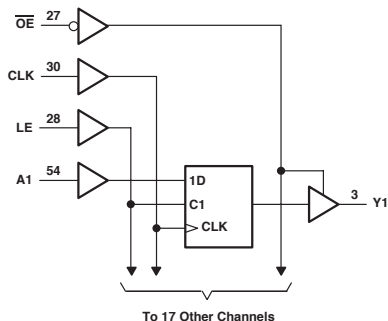
UNIT f_{max}: MHz other: ns

162835

18-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162835, SN74ALVCH162835: Output Port Has Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L or H	X	Y _{0†}

† Output level before the indicated steady-state input conditions were established

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	0.04	mA
I _{QH}	MAX	-12	-12	mA
I _{OL}	MAX	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V
t _{max}			MIN	150	150
t _w Pulse duration	LE low		MIN	3.3	3.3
	CLK high or low		MIN	3.3	3.3
t _{su} Setup time	Data before CLK *		MIN	1.7	1.7
	Data before LE , , CLK high		MIN	1.5	1.5
	Data before LE , , CLK low		MIN	1	1
t _h Hold time	A data after CLK *		MIN	0.7	0.7
	Data after LE , , CLK high		MIN	1.4	1.4
	Data after LE , , CLK low		MIN	1.4	1.4
t _{PLH}	A	Y	MAX	4.2	4.2
t _{PHL}	A	Y	MAX	4.2	4.2
t _{PLH}	LE	Y	MAX	5.1	5.1
t _{PHL}	LE	Y	MAX	5.1	5.1
t _{PLH}	CLK	Y	MAX	5.4	5.4
t _{PHL}	CLK	Y	MAX	5.4	5.4
t _{PZH}	OE	Y	MAX	5.5	5.5
t _{PZL}	OE	Y	MAX	5.5	5.5
t _{PHZ}	OE	Y	MAX	4.5	4.5
t _{PZL}	OE	Y	MAX	4.5	4.5

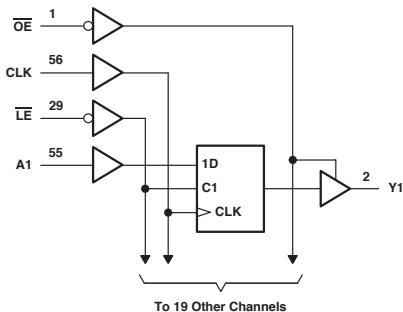
UNIT f_{max} : MHz other : ns

162836

20-BIT UNIVERSAL BUS DRIVER WITH 3-STATE OUTPUTS

- SN74ALVC162836, SN74ALVCH162836: Output Port Has Equivalent 26-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

INPUTS				OUTPUT
OE	LE	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L or H	X	Y ₀ †

† Output level before the indicated steady-state input conditions were established

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	ALVC 3V	ALVCH 3V	UNIT
I _{CC}	MAX	0.04	0.04	mA
I _{DH}	MAX	-12	-12	mA
I _{OL}	MAX	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC 3V	ALVCH 3V
f _{max}			MIN	150	150
t _w Pulse duration	LE low		MIN	3.3	3.3
	CLK high or low		MIN	3.3	3.3
t _{su} Setup time	Data before CLK *		MIN	1.5	1.5
	Data before LE, CLK high		MIN	1.3	1.3
	Data before LE, CLK low		MIN	1.2	1.2
t _h Hold time	A data after CLK *		MIN	0.9	0.9
	Data after LE, CLK high		MIN	1.1	1.1
	Data after LE, CLK low		MIN	1.1	1.1
t _{PLH}			MAX	4	4
t _{PHL}			MAX	4	4
t _{PLH}	LE	Y	MAX	5.1	5.1
t _{PHL}	LE	Y	MAX	5.1	5.1
t _{PLH}	CLK	Y	MAX	5	5
t _{PHL}	CLK	Y	MAX	5	5
t _{PZL}	OE	Y	MAX	5.5	5.5
t _{PZH}	OE	Y	MAX	5.5	5.5
t _{PLZ}	OE	Y	MAX	5.1	5.1
t _{PHZ}	OE	Y	MAX	5.1	5.1

UNIT f_{max} : MHz other : ns

162841

20-BIT BUS-INTERFACE D-TYPE LATCH WITH 3-STATE OUTPUTS

- SN74ABT162841: Output Ports Have Equivalent 25-Ω Series Resistors
- SN74ALVCH162841: Output Ports Have Equivalent 26-Ω Series Resistors

FUNCTION TABLE
(each 10-bit latch)

INPUTS			OUTPUT
OE	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q ₀
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

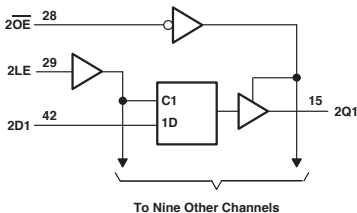
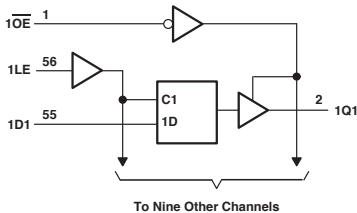
PARAMETER	MAX or MIN	ABT	ALVCH 3V	UNIT
I _{CC}	MAX	89	0.04	mA
I _{OH}	MAX	-12	-12	mA
I _{OL}	MAX	12	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ABT	ALVCH 3V
t _w Pulse duration	LE high or low		MIN	4	3.3
t _{su} Setup time	Data before LE		MIN	0.8	1.1
t _h Hold time	Data after LE		MIN	1.8	1.1
TP _{LH}	D	Q	MAX	5.2	4.3
TP _{HL}				6	4.3
TP _{LH}	LE	Q	MAX	5.4	4.7
TP _{HL}				5.8	4.7
TP _{ZH}	OE	Q	MAX	5.7	5.3
TP _{ZL}				6.5	5.3
TP _{HZ}	OE	Q	MAX	6.5	4.4
TP _{LZ}				7.1	4.4

UNIT: ns

Logic Diagram



164245

16-BIT TRANSCEIVER AND 3.3-V TO 5-V SHIFTER WITH 3-STATE OUTPUTS

- SN74ALVC164245:

A port has V_{CCA} , which is set to operate at 2.5 V and 3.3 V

B port has V_{CCB} , which is set to operate at 3.3 V and 5 V

- SN74AVCB164245, SN74AVCBH164245:

The A-port is designed to track V_{CCA} , V_{CCA} accepts any supply voltage from 1.4 V to 3.6 V

The B-port is designed to track V_{CCB} , V_{CCB} accepts any supply voltage from 1.4 V to 3.6 V

FUNCTION TABLE
(each 8-bit section)

INPUTS		OPERATION
\overline{OE}	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

RECOMMENDED OPERATING CONDITIONS

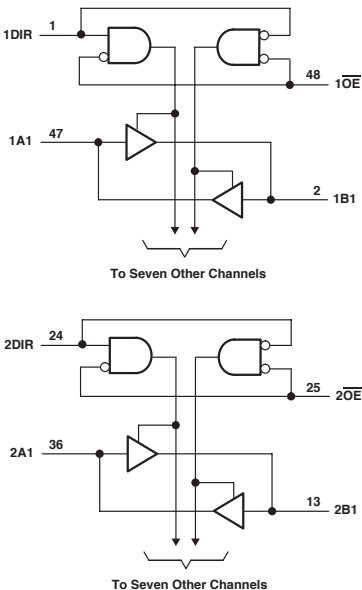
PARAMETER	MAX or MIN	ALVC	AVCB	AVCBH	UNIT
I_{CC} (5V)	MAX	0.04	-	-	mA
I_{CC} (3V)	MAX	0.02	0.04	0.04	mA
I_{OH} (5V)	MAX	-24	-	-	mA
I_{OL} (5V)	MAX	24	-	-	mA
I_{OH} (2.3V)	MAX	-12	-8	-8	mA
I_{OL} (2.3V)	MAX	12	8	8	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	ALVC		AVCB	AVCBH
				$V_{CCB}: 3V$ $V_{CCA}: 2.3V$	$V_{CCB}: 5V$ $V_{CCA}: 3V$	$V_{CCB}: 3V$ $V_{CCA}: 2.3V$	$V_{CCB}: 3V$ $V_{CCA}: 2.3V$
t_{PLH}	A	B	MAX	7.6	5.8	3.4	3.4
t_{PHL}				7.6	5.8	3.4	3.4
t_{PLH}	B	A	MAX	7.6	5.8	3.7	3.7
t_{PHL}				7.6	5.8	3.7	3.7
t_{PZL}	\overline{OE}	B	MAX	11.5	8.9	5.1	5.1
t_{PZH}				11.5	8.9	5.1	5.1
t_{PZL}	\overline{OE}	A	MAX	12.3	9.1	4.2	4.2
t_{PZH}				12.3	9.1	4.2	4.2
t_{PLZ}	\overline{OE}	B	MAX	10.5	9.5	3.3	3.3
t_{PHZ}				10.5	9.5	3.3	3.3
t_{PLZ}	\overline{OE}	A	MAX	9.3	8.6	3	3
t_{PHZ}				9.3	8.6	3	3

UNIT: ns

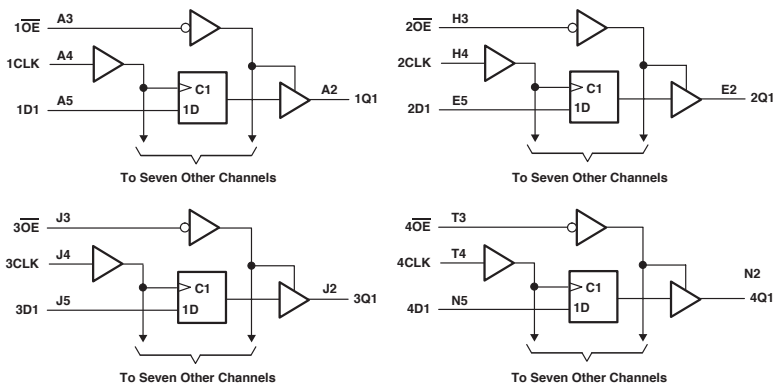
Logic Diagram



3.3-V ABT 32-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOP

- Output Ports Have Equivalent 22-Ω Series Resistors

Logic Diagram



FUNCTION TABLE

(each 8bit flip-flop)

INPUTS			OUTPUT
\overline{OE}	CLK	D	Q
L	1	H	H
L	1	L	L
L	H or L	X	Q_0
H	X	X	Z

RECOMMENDED OPERATING CONDITIONS

PARAMETER	MAX or MIN	LVTH 3V	UNIT
I_{CC}	MAX	10	mA
I_{OH}	MAX	-12	mA
I_{OL}	MAX	12	mA

SWITCHING CHARACTERISTICS

PARAMETER	INPUT	OUTPUT	MAX or MIN	LVTH 3V
f_{max}				160
t_w Pulse duration, CLK high or low			MIN	3
t_{su} Setup time	Data before CLK , data high		MIN	1.8
	Data before CLK , data low		MIN	1.8
t_h Hold time	Data after CLK , data high		MIN	0.8
	Data after CLK , data low		MIN	0.8
t_{PLH}	CLK	Q	MAX	5.3
t_{PHL}				4.9
t_{PZH}	\overline{OE}	Q	MAX	5.6
t_{PZL}				4.9
t_{PHZ}	\overline{OE}	Q	MAX	5.4
t_{PLZ}				5

UNIT f_{max} : MHz other : ns

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